A New Type of Single Board Computers for Detectors

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Systems using single board computers (SBCs) have hardware that cannot be easily configured for special applications. Upgrading the hardware is extremely costly and the hardware often requires expensive real time operating system (RTOS) licenses that also need to be updated periodically.

Proposed in this paper is a new type of SBCs – versatile, modular, reconfigurable and upgradeable ones that utilize a portable, high performance, standards-based real-time executive for which the source code is free – open source, and designed such that it makes them usable in a wide variety of applications including controllers and embedded controllers.

At Thomas Jefferson National Accelerator Facility, Versa Module Europa (VME) systems are used extensively and their usage is planned to be increased for the 12 GeV upgrade of the facility. Typically, VME SBCs running VxWorks RTOS as distributed input/output controllers (IOCs) are used as control systems. These IOCs function as experimental physics and industrial control system (EPICS) IOCs, whose EPICS core is composed of the IOC software and the channel access client and server.

The current VME controller implementation has drawbacks. For instance, controllers are a mixture of various models of SBCs and many of these controllers have dated technology that cannot be upgraded.

With the release of EPICS Base R3.14, which accepts RTOS other than VxWorks and the availability of new hardware, it is possible to resolve standardization and upgrade issues by designing a new type of SBCs, the conceptual design of which is described below.

The new SBC's board will consist of a 6U standard VME controller with expandable, flexible logic design based on field programmable gate arrays (FPGAs)[1] programmed with open source intellectual property (IP) cores[2]. The SBC will be able to fulfill multiple board roles by incorporating support for standard bus mezzanine multi-purpose cards such as analog to digital converters (ADCs) and digital to analog converters (DACs). The internal peripheral component interconnect (PCI) communication bus will be a versatile, multi-purpose FPGA based design. FPGA core logic will be used as a high performance embedded microcontroller.

State of the art advances in FPGA technology such as improvements in logic density, device speed and compiler tools will make the proposed SBC faster than many microprocessor-based SBCs or embedded controllers.

Since it would be prohibitively expensive to upgrade all parts of a control system at one time, the FPGA design will be such that improvements can be done via an IP core software update. Further, the system design will include the concept of layers or hierarchy, so that reprogramming a limited number of layers is sufficient to change a particular feature or to make a performance upgrade.

The ability to reprogram the FPGA provides a permanent path via software updates to implement new features, remotely if necessary, into an existing system after its fabrication and installation.

The SBC design will incorporate Joint Test Action Group (JTAG) interface which will make hardware functionality easily upgradeable. JTAG offers in system programming capability and can also be used for board level interconnection and functionality testing.

To minimize dependence on a sole manufacturer only products with multiple sources will be used. This approach avoids the severe impact of a manufacturer going out of business or dropping a product line.

The new SBC will be able to perform most current SBC applications. User defined options will be easily reconfigurable for specialized applications. Note, accelerator division's SBC upgrades will have no impact on physics division's hardware requirements.

For the planned feasability study the goal is to provide proof of principle – it is possible to have a solution using FPGAs and open source IP cores and RTOSes. The study should also make it possible to evaluate the performance of the FPGA design, the RTOS, and the application software as well as point out ways to provide more capability than available in current SBCs.
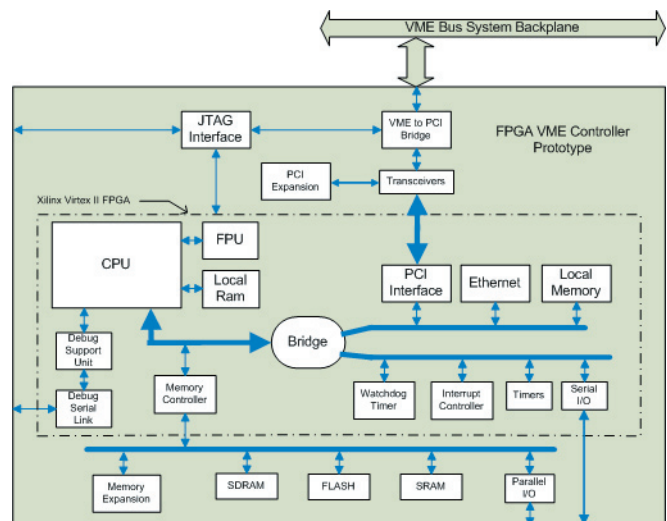

FIG. 1. prototype block diagram

Figure 1 shows the block diagram for the prototype SBC. The main component of the SBC is the scalable processor

architecture (SPARC) based central processing unit (CPU) IP cores – LEON2 processor, which is a synthesizable very high-level design language model of a 32-bit SPARC processor compliant with the Institute of Electrical and Electronic Engineers' SPARC V8 architecture. The RTOS used is real-time embedded system for multiprocessor systems , a portable high performance, standards-based real-time executive which is compatible with EPICS (release Base 3.14) IOC core and for which the source code is free. The complete source code is available under the GNU is Not Unix license, which allows free and unlimited use.

The LEON2 processor's FPGA IP core has several significant features such as a SPARC V8 compliant integer unit with a 5-stage pipeline, a separate instruction and data cache, SPARC V8 reference memory management unit, on-chip buses based on advanced microcontroller bus architecture, and 8/16/32-bits memory controller. LEON2 comes with peripherals such as universal asynchronous receiver-transmitters, timers, interrupt controller and input/output (IO) ports and a 32-bit Master/Target PCI Interface and a 10/100 Ethernet interface.

Upon successful completion of the study, a printed circuit board of the SBC will be designed. Upgrades for the final version of the SBC could include: VMEbus switched serial backplane capabilities with backward compatibility, ability to combine several current VME cards into a single IOC board, capability to support standard mezzanine cards PCI and industry pack IO, support via compact PCI, and PCI mezzanine card for VME physics, improvement of memory, communication and processor speed, and implementation of FPGA CPU and memory core on payload board so that it can be used as an embedded controller or as a core for other bus formats.

In conclusion, the proposed SBC design targets the requirements of many current SBC applications and provides a clear upgrade path to meet the needs of future experiments.

The proposed SBC will extend the life of VME systems given the capabilities of the FPGAs and the ease of implementing technology improvements.

Use of open source FPGA IP cores and RTOS will significantly reduce licensing and development costs[3]. The flexible design of the SBC will allow multiple use of the central FPGA CPU logic as a high-performance embedded controller.

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[1] The FPGAs' basic building blocks, IP cores, are software logic designs that can be tailored to fit the exact needs of the detectors. Current Jlab FPGA designs provide versatile VME bus data acquisition and control interfaces and also control and monitor numerous systems by interfacing sensors and instrumentation with ADCs, DACs, and time to digital converters.

[2] An IP core is a block of logic that is used in making application-specific integrated circuits and FPGAs.

[3] In the past FPGA and electronic design automation vendors charged anywhere from $5,000 to more than $350,000 for cores.