Test Procedures for the Test Stand of the CLAS Drift Chamber High Voltage System

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This paper presents the test procedures for the CAEN Test Stand (Cats), which is used for rapid testing, calibrating, and debugging of crates and modules of the SY527 CAEN power supply (Sycap) that provides high voltage for the CLAS drift chambers.

Cats [1] currently tests eight of the sixteen first article tests. Some tests are physical such as connector inspection. Some specifications are tested indirectly, such as the crate turn on/off. Cats uses a LabVIEW [2] GUI to display and test data from the mainframe and modules.

The voltage variation test, Fig. 1 shows the front panel (FP), ramps all twenty-four channels to the demand voltage, 1250 VDC, and checks whether the output voltage measured by the High Voltage Controller Module (HVCM) satisfies:

$$|V^{i}_{max} - V^{j}_{min}| < 1 \text{ VDC}; i, j \in [1,2,3 \ldots 24] \wedge i \neq j. \quad (1)$$

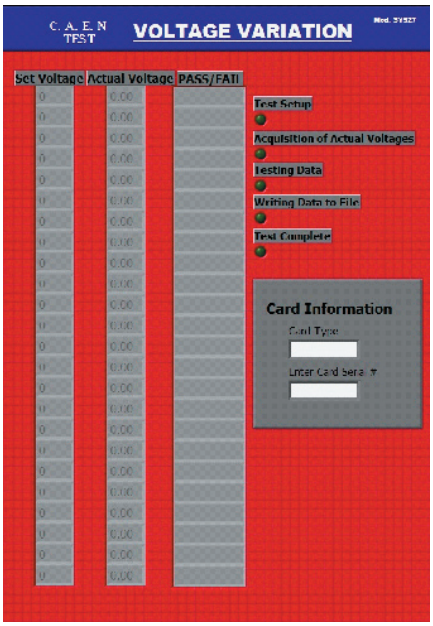
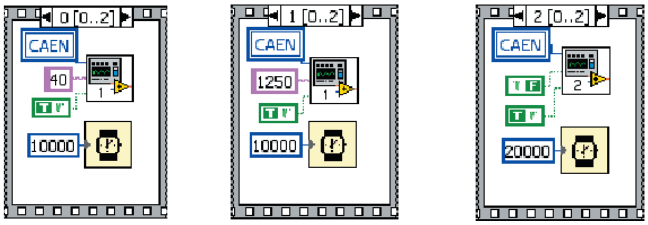


FIG. 1. Voltage variation FP

The three test setup functions, Fig. 2 from left to right, sets the current trip level to 40 μA, the voltage to 1250 VDC, and turns on all channels. Each of the three functions requires the serial port address at which the mainframe is connected (blue box labeled CAEN) and a Boolean (T/F) to accept or reject input. Additionally, the current function (Fig. 2a) needs the current level (pink box that contains the numerical value 40), the voltage function (Fig. 2b) needs the voltage level, 1250 VDC, and the power up function (Fig. 2c) needs another Boolean to confirm and initiate ramping of the channels. All functions include a delay in milliseconds (bottom numerical box) to allow the processes to complete.



a b c

FIG. 2. Sequence to set up current and voltage levels

The HVCM's readout function (HVRF) needs two inputs, the test box serial location and the calibration value, to acquire the readback voltages from the mainframe, Fig. 3. HVRF outputs an array with measured voltages of the twenty-four channels. Once the voltages are acquired, the data is checked, Fig. 4, as per equation 1.

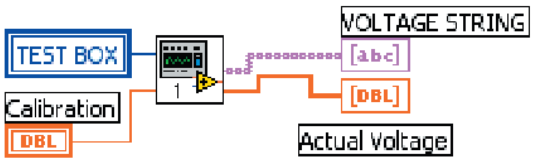


FIG. 3. HVCM readout function (HVRF)

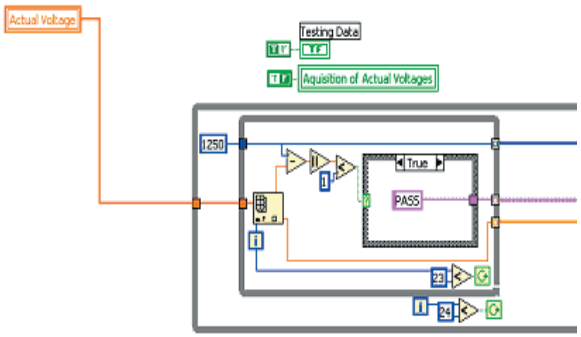


FIG. 4. Voltage Variation data testing

The channel isolation test measures the output voltages and checks whether powering a single channel or a group of channels changes the voltages of other channels by more than one volt. One channel is powered and changes in the voltages of the other channels are measured and recorded. Figure 5 shows the FP.

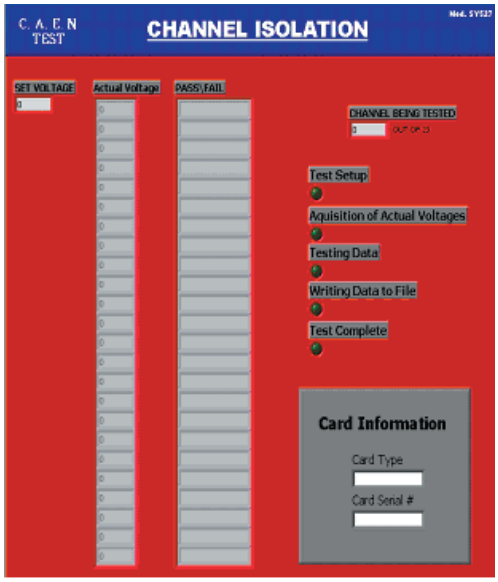
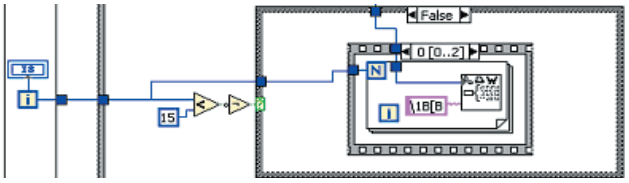
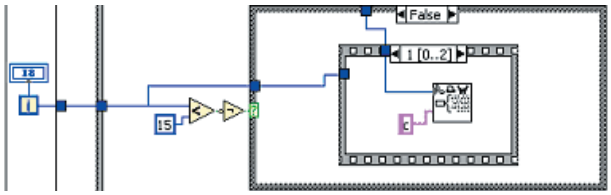


FIG. 5. Channel Isolation FP

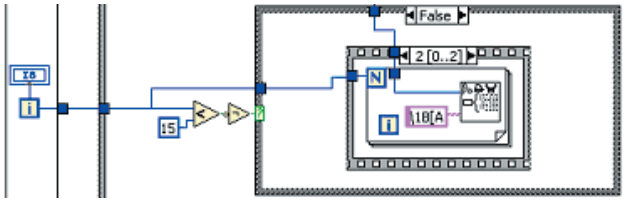
The cursor is moved to the channel that must be powered, Fig. 6a. When the channel to be powered coincides with the for-loop (inner-most loop in Fig. 6a) the program writes a "\1B[B to the mainframe and moves the cursor down to power the channel number it has extracted. The channel is powered by writing a "c" to the mainframe, Fig. 6b. Then the cursor is moved back to the start position by writing a "\1B[A", Fig. 6c. Voltage changes of the other channels are checked.



a. Moving cursor to turn on channel



b. Writing "c" to change channel status



c. Moving cursor to turn off channel

FIG. 6. Channel isolation power control

The voltage range test checks the maximum output voltage of the mainframe by ramping the voltage to 2500 VDC on all channels and measuring whether the voltages of all channels are 2500 +/- 6 VDC.

All channels are powered and given eight seconds to ramp up. The FP looks similiar to Fig. 5. Figure 7 shows details of the program.

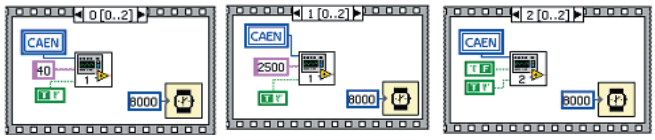


FIG. 7. Setting current and voltage

Once the output voltages are measured and read, the array that the HVRF produces are tested, loop in center of Fig. 8., and output to the FP.

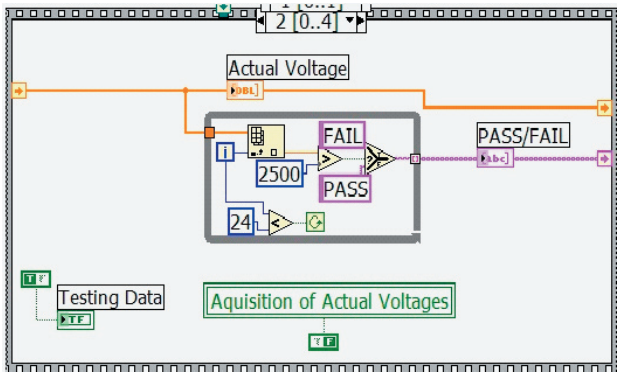


FIG. 8. Reading voltages

Voltage setting resolution and accuracy, FP shown in Fig. 9, checks the demand voltage setting of the mainframe's display by reading the mainframe's demand voltage setting, V_d, and comparing it to the output voltage, V_o, measured by the HVCM.

If $\Delta V := | V_d - V_o | < 6$ VDC $\Rightarrow Ch_{pass}$. (2)

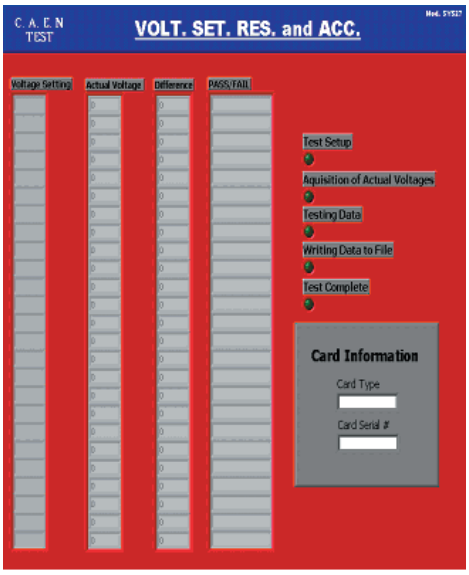


FIG. 9. Voltage setting, resolution, and accuracy FP

Once all channels are powered, the demand voltages are acquired from the mainframe, Fig. 10, using HVRF.

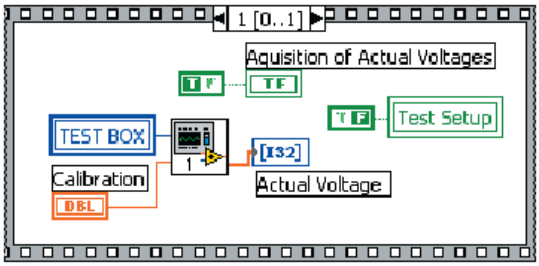


FIG. 10. Voltage acquisition

The measured voltage is acquired in an array from the HVCM, Fig.11, and passed to the next sequence for comparison with the demand voltages from the mainframe. In the comparison stage, Fig. 12, equation 2 is verified.

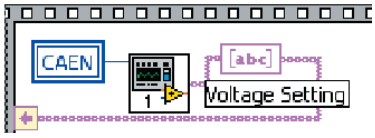


FIG. 11. Mainframe voltage readout

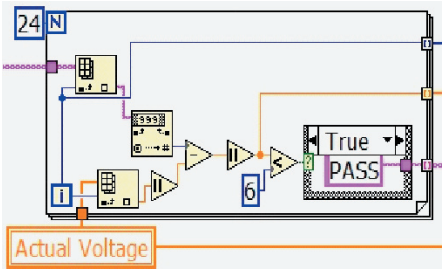


FIG. 12. Comparing actual voltage to mainframe's readout voltage

Voltage monitoring resolution, and accuracy test operates like the voltage setting resolution and accuracy test, except that it checks the readback voltage, not the demand voltage.

Current monitoring resolution and accuracy, FP similar to Fig. 9, checks the accuracy of the monitored current, I_m.

$$\text{If } \Delta I := |I_{cal} - I_m| \leq 2\% I_{cal} + 40 \text{ nA} \Rightarrow Ch_{pass} \quad (4)$$

The test is similar to the voltage monitoring resolution and accuracy test.

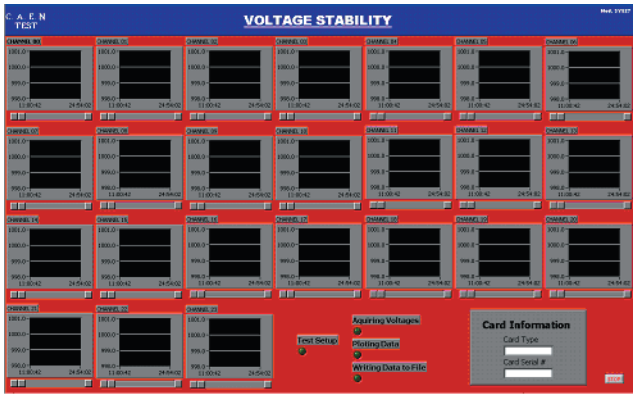


FIG. 13. Voltage stability FP

The voltage stability test monitors that the output voltage does not vary by more than one volt over a twenty-four hour period. This test ramps the voltage to the demand value and records the output voltage as measured by the HVCM. The FP displays the twenty-four voltage recording graphs, Fig. 13, one for each channel. The graphs record the voltage data until the "Stop" button in the lower right-hand corner is engaged. The voltages are passed on to the graph recorder, which records the voltage data with respect to time, Fig. 14.

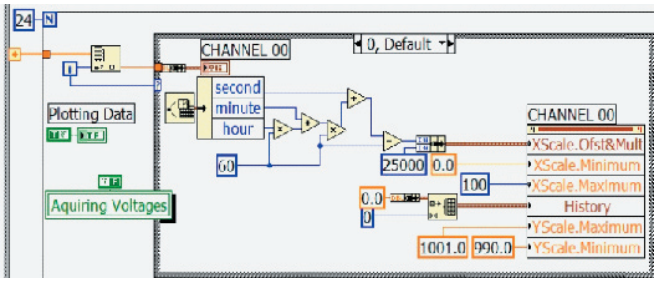


FIG. 14. Plotting voltage readings

The over current protection test, Fig. 15, ensures that the mainframe shuts down properly under over current conditions. The test starts by using the HVCM to monitor the output voltage of channel one, Fig. 16. Taking 25 MΩ out of the built-in voltage divider causes the current to increase and trip the channel, Fig. 17.

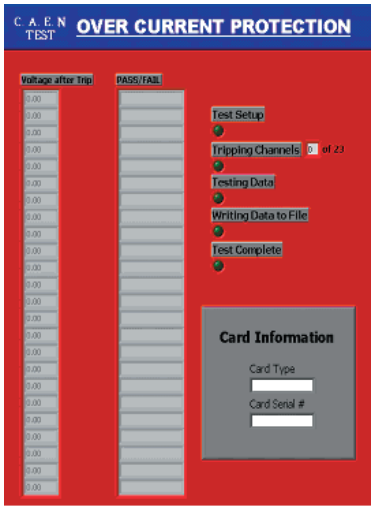


FIG. 15. Over current protection FP

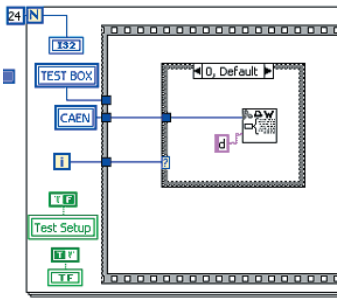


FIG. 16. Turning on a relay to read a channels voltage

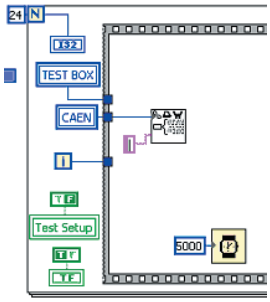


FIG. 17. Tripping channel command

Once the channel has tripped, the voltage is read by the HVRF. The test section of the program, Fig. 18, checks if V(t) = 0; t ≧ 10 s. As each channel is tested, the data on the FP automatically updates. Each channel is tested in sequence. The channel being tested is indicated next to the "Tripping Channel" LED.

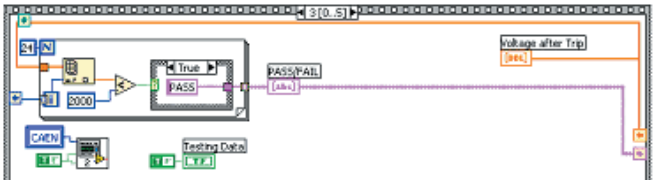


FIG. 18. Testing trip data

Cats aids proper selection of operating cards and allows the storage of test data essential for solving problems or repairing components of Sycaps. Cats tests and records the module's data accurately and effeciently.

[1] "First Article Test Results." High Voltage tests in detail. Req. 66250-S-10358

[2] National Instruments. LabVIEW v6 User Manual. Austin, Texas: National Instruments Corporation, 2000.