Status Report on the Prototyping of Silicon Vertex Tracker

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Hall B is considering a silicon vertex tracker (SVT) for the CLAS++ upgrade. A prototype study of the SVT is currently underway. This note gives a brief overview of the progress made on the SVT project.

The physics motivation for the SVT and a tentative design of the detector is given in the CLAS++ conceptual design report [1]. The SVT will consist of six sectors, Fig. 1. Each sector comprises three regions, Figs. 2 and 3, and has two super layers (u, v) each of which has strips that are 300 µm thick and a pitch of 300 µm. The u, v layers are angled at 4.6° with respect to each other, Fig. 4, which results in ~ 60,000 channels. Each super layer has a plane region which runs parallel to the beam axis that then meets up against a trapezoidal region, which is at 45° with respect to the beam axis.

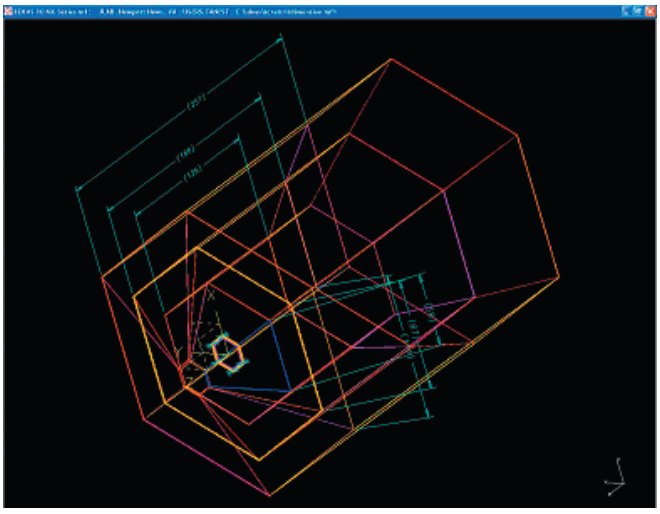

FIG. 1. Isometric view.

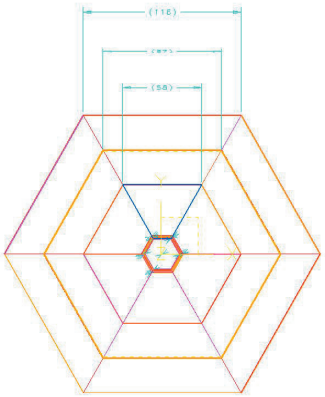

FIG. 2. SVT front view.

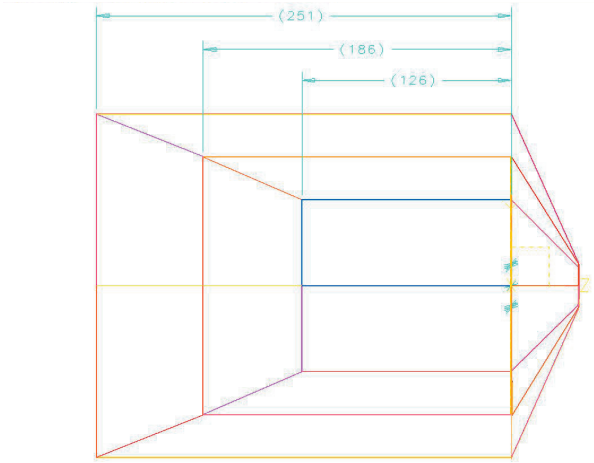

FIG. 3. SVT side view.

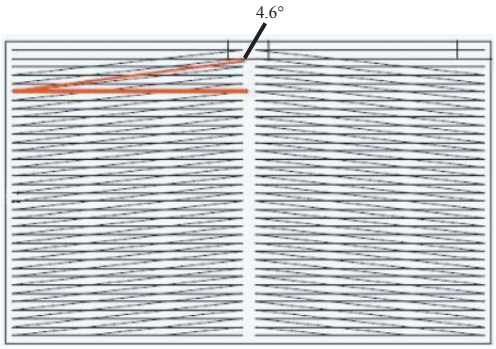

FIG. 4. Canted layers.

IDEAS is used for Finite Element Analysis and the flange that will be attached to the beam line is being designed in such a way that it will support the SVT with the scattering chamber and the target. Thermal analysis of the module is in progress. Figure 5 shows the styrofoam model of the SVT.

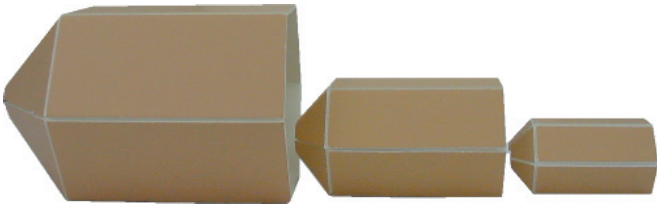

FIG. 5. Styrofoam model of three regions.

The read-out electronics will use the SVX4 readout chips, which have been used successfully at the Collider Detector Facility. Each SVX4 chip [2], Fig. 6, has 128 channels. Fig. 7 [2] shows an overall schematic of the chip. An individual channel of the front end [3] is shown in Fig. 8.

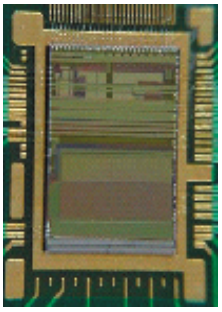

FIG. 6. SVX4 chip.

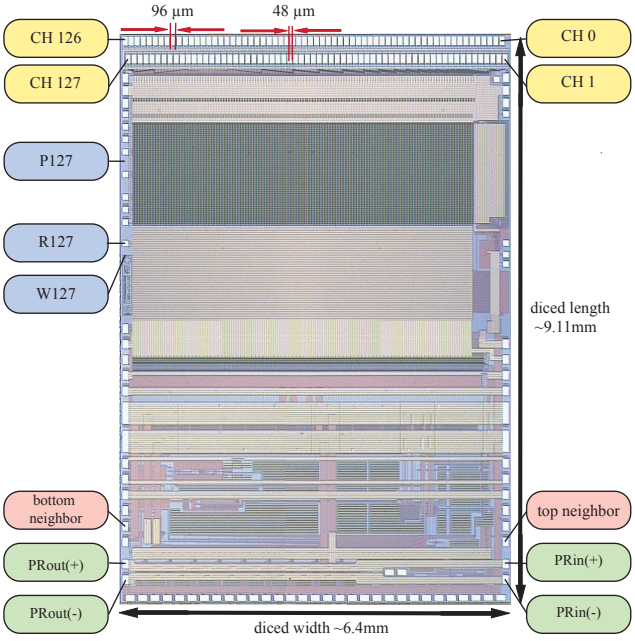

FIG. 7. Picture of SVX4 chip. The bottom is the back-end of the chip, the top the front-end. The 128 input pads are at the top; the Priority in/out and top/bottom neighbor are at the bottom. The three buffered diagnostic analog probe points of the last channel (127) are located on the left. This chip is fabricated with the 0.25 micron TSMC process on 300-micron thick silicon.

Fermilab has designed two boards: the PCI Test Adapter (PTA) and the Programmable Mezzanine Card (PMC), which plug inside a PC with a PCI bus, Figs. 9 and 10. These boards can be configured to test different hardware setups. FPGA's can be programmed to send control signal patterns to the test hardware and collect generated data. The host computer analyzes the data and evaluates the performance of the hardware.

Fermilab provided two SVX4 chips, a single-chip SVX4 test board, a hybrid module with four SVX4 chips (512 channels), Fig. 11, and an adapter board, Fig. 12. The PTA/PMC

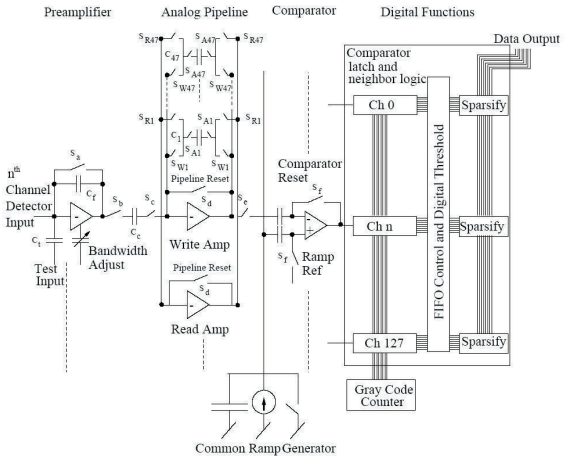

FIG. 8. Single channel block diagram.

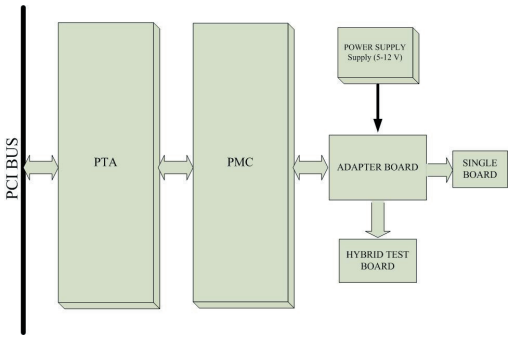

FIG. 9. PCI test stand.

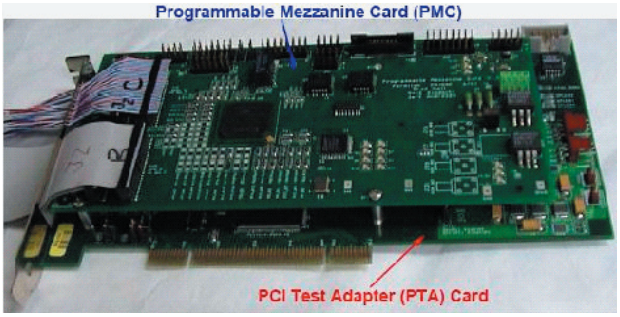

FIG. 10. PMC and PTA cards.

was procured from Kinetic Systems and firmware was installed in the FPGA. The software and the board with the SVX4 chip were tested with the Daq software provided by Fermilab, at Fermilab.

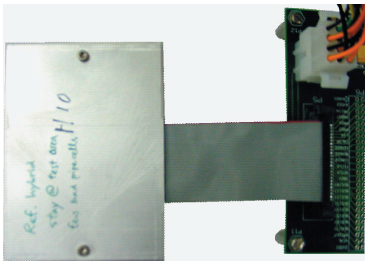

FIG. 11. Hybrid module.

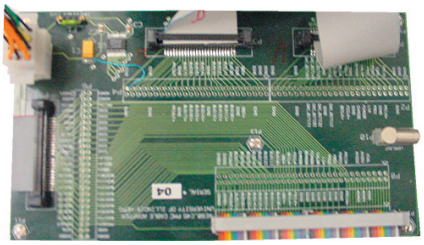

FIG. 12. Adapter board.

The single-chip test setup, Fig. 13, comprises a workstation, the SVX4 chip, a 5 VDC power supply, the PTA/PMC, an adapter board, and a ribbon cable with Samtec connector. The test setup for the single chip, Fig. 13, is similart to the test setup for the hybid module, Fig. 14.

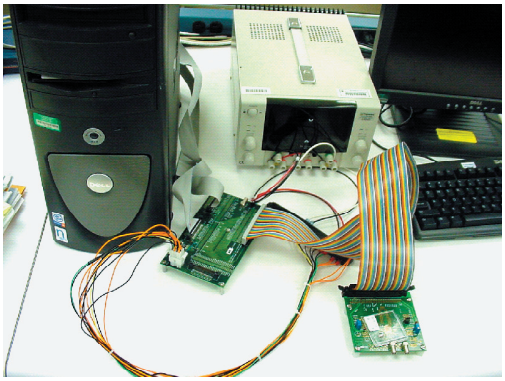

FIG. 13. Single board test setup.

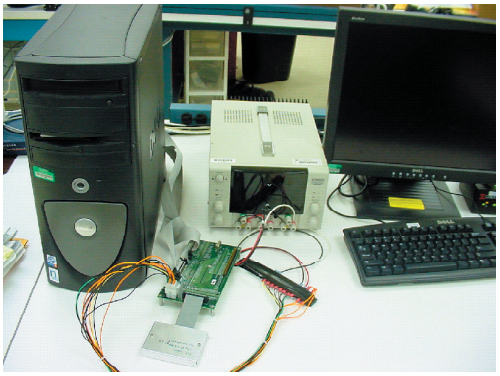

FIG. 14. Hybrid test setup.

ROOTXTL, a software package, controls the SVX4. It allows the user to run several tests of SVX4 chips, hybrids, or staves and makes plots such as pedestal, noise, and differential noise.

Results of the pedestal run and noise level test from the hybrid module are shown in Fig. 15. The top histogram shows the pedestal for channel 70. The mean is 76.5 ADC counts and the RMS is 1.1 ADC counts. The RMS value of each of the 512 channels (128 channels per chip) is shown in blue in bottom of Fig. 15 and the average ADC counts are shown in bottom of Fig. 16.

The cell ID histogram, top of Fig. 16, shows 9200 entries – channel 70 for each of the four chips × fifty runs × forty-six sequences per run. The sequences of a run are: acquire, then digitize and read out data stream, which is defined by the "Daq file".

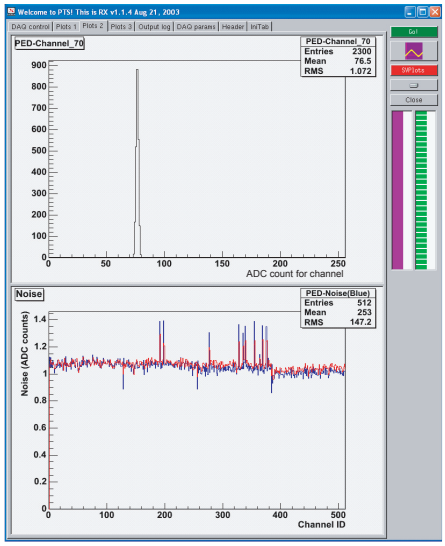

FIG. 15. Hybrid pedestal run and noise level versus channel ID.

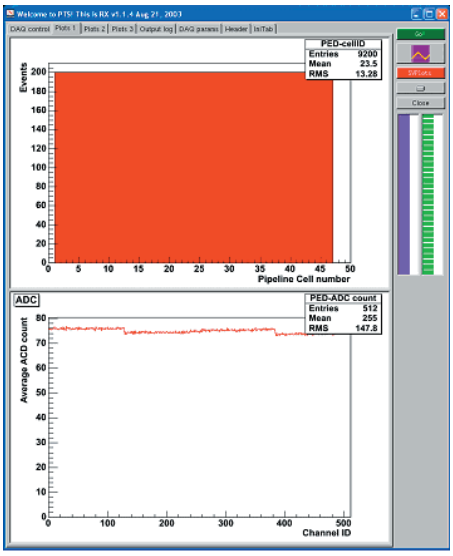

FIG. 16. Pedestal test for hybrid.

Fermilab has been contacted regarding a stave, Fig. 17, which includes the hybrid module with silicon sensor, Fig. 18.

Simulation of the SVT is being done with Geant4 [4], which provides a set of tools including geometry, tracking, detector response, run, event and track management, visualization, and user interface. The present simulation, Figs. 19 and 20, has minimal physics processes included. A plan to enhance the model and build a prototype that can be developed further to simulate the entire CLAS detector system in GEANT4 is envisioned. In this effort, a G4 user group has been formed and a three-day Geant4 workshop at Fermilab was attended.

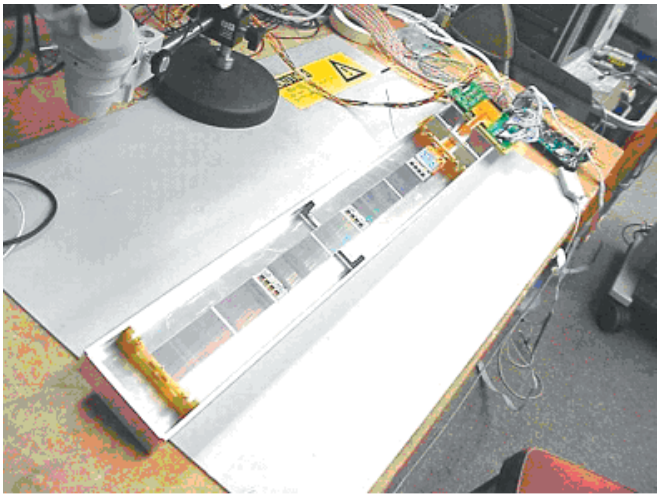

FIG. 17. Stave.

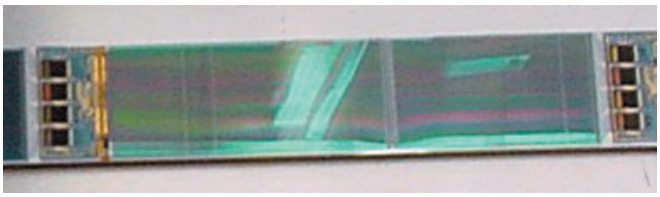

FIG. 18. Silicon sensor.

The read-out design is being done in-house. The SVT software is being developed to be compatible with CODA, so that analysis can be done with either A1 or RECIS for CLAS++.

In conclusion, the development of the SVT prototype is progressing slowly but steadily. The prototype study is planned in two phases – lab tests and beam tests. Lab tests will use a signal simulator. Most of the equipment for the lab tests is being procured. For the beam tests, a stave is required. At this time, negotiations to procure one are being initiated.

[1] CLAS++ Conceptual Design Report, V. Burkert et. al.
[2] SVX4 User manual, L. Christofek et. al
[3] SVX4 Front End, Tom Zimmerman
[4] GEANT 4 Simulation, M. Halappanavar et. al CLAS-Note 2004-013

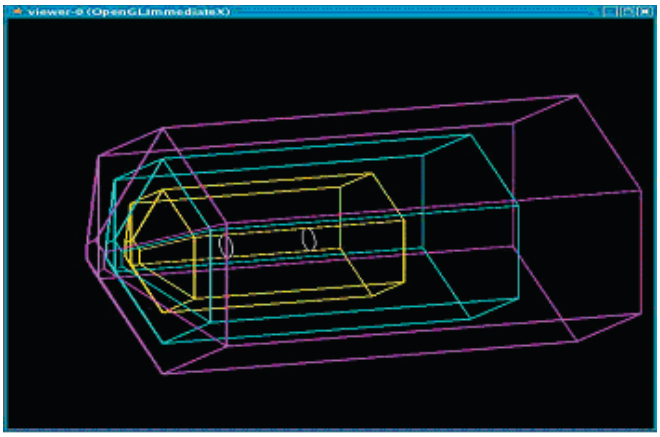

FIG. 19. GEANT4 geometric model of detector.

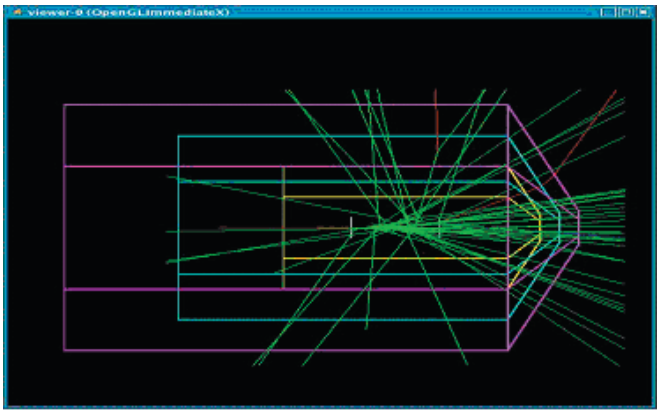

FIG 20. GEANT4 example run for SVT (E_e=500MeV, B=2T).