

Remote Reset of Level 2 Trigger with the HMS Monitoring System

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The level 2 trigger (L2T) of CLAS is generated in the Segment Collector Cards (SCCs) by track-segment patterns identified by the ninety-six hit bits of the twelve Segment Finder Subsystem Cards (SFSCs) – eight hit-bits per SFSC. Occasionally, the FPGAs of the SFSCs and SCCs need to be reset. This is done remotely by the HMS Monitoring System (HMS). Details of the HMS-based implementation of the L2T reset are given in this note.

Prior to the installation of HMS [1-3], if the L2T rate, as determined by running *l2_status* function from the CLON clusters, dropped to 0 Hz, an access had to be made into the end station to reset the SCCs in the analog-to-digital board (ADB) crate, Fig. 1.



FIG. 1. ADB crate.

HMS is capable of remotely resetting the FPGAs on the SFSCs, Fig. 2, and the SCCs, Fig. 3, via the trigger calibration interface card (TCIC), Fig. 4, and is capable of remotely power-cycling the ADB crates – resulting in reduction of down-time during beam.

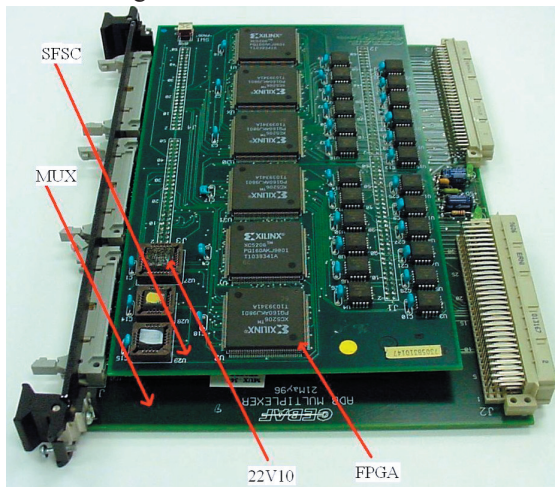


FIG. 2. SFSC.

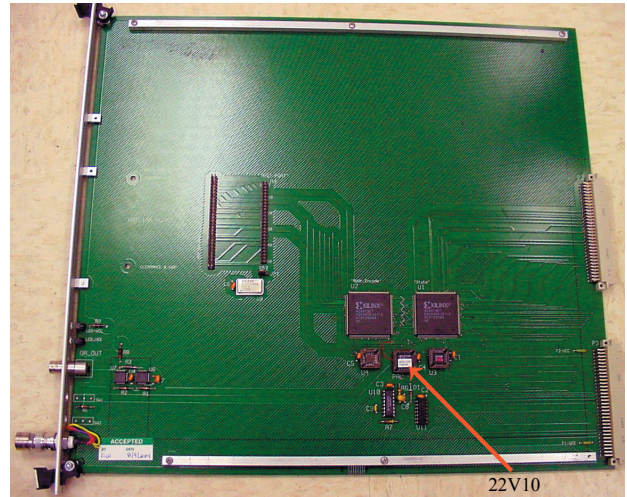


FIG. 3. SCC.

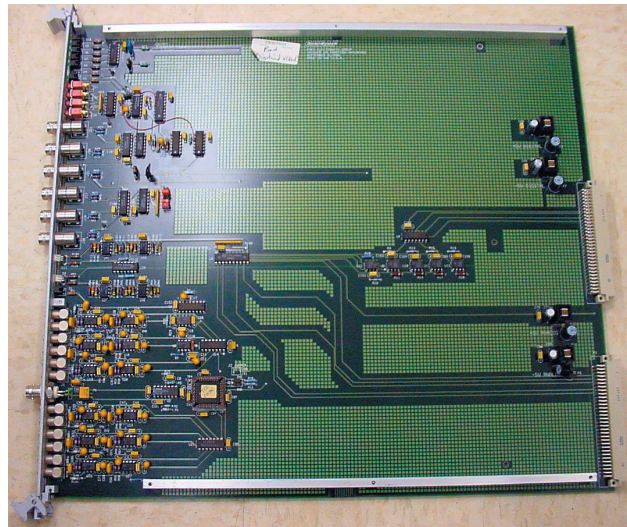


FIG. 4. TCIC.

The 22V10 EPROM on the SFSCs and SCCs need a TTL pulse less than 1 ms to be reset. On the TCIC, Fig. 5, the output reset signal from the NAND gate 7400 (pin 3 on U29) goes out to the buffer/driver pin 1, DC triggered multi-vibrator 74LS123N (U35). From pin 4 of 74LS123N (U35) the generated TTL signal goes to pins 6 and 8 of LS244 (U40), which drives the pulse to 22V10 on the SFSCs and the SCCs via the backplane, Fig. 6.

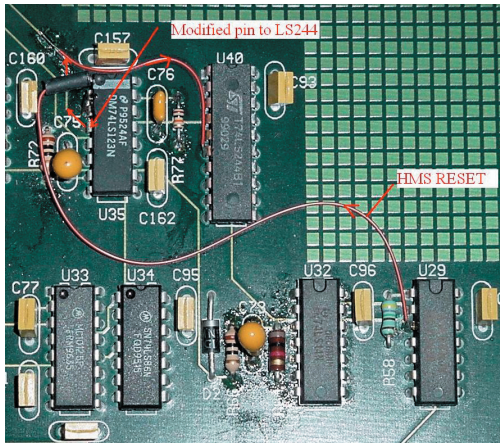


FIG. 5. TCIC detail.

The HMS-based L2T remote reset system has been implemented and tested. The remote reset feature removes a long-standing problem of having to enter the end station to reset L2T.

- [1] Antonioli *et.al* A Novel Monitoring System for Electronic Instrumentation. CLAS-Note 2003-018.
- [2] Eng *et.al* Software Design Elements of HMS. CLAS-Note 2004-001.
- [3] McMullen *et.al* Hardware Elements of the Electronic Instrumentation's Monitoring System. CLAS-Note 2004-011.

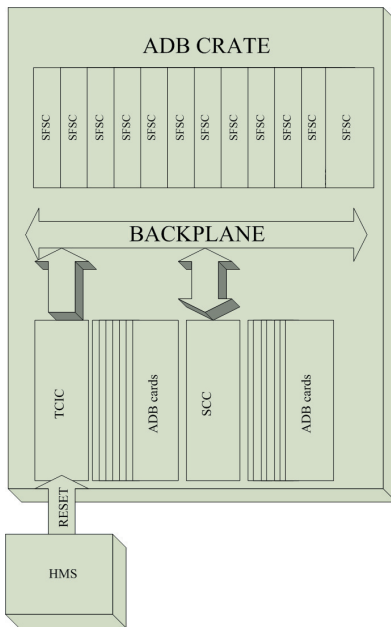


FIG. 6. L2T reset schematic.