

A Test Station for LeCroy 1877 Fastbus Time-to-Digital Converters

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This note presents details of the stand-alone Fastbus test station (FTS) developed to check the functions of the LeCroy model 1877 Fastbus time-to-digital converter (TDC) modules. FTS can be expanded to test other types of Fastbus modules.

CLAS wire chamber read-out system uses approximately two hundred LeCroy model 1877 Fastbus TDC modules. Testing the TDC modules and ensuring availability of spares is vital for the smooth running of the experiments.

FTS comprises an eight-slot Fastbus crate with a Struck Sis 4100 VME to Fastbus interface, a Motorola MVME-162LX single board computer (SBC) [1], a PC with Ethernet interface, a Stanford Research Systems' DG535 digital delay/pulse generator [2], a National Instruments ENET/100 GPIB-Ethernet interface, a Fastbus ECL fan-out module, and the TDC module to be tested. Setup of FTS is shown in Fig. 1.

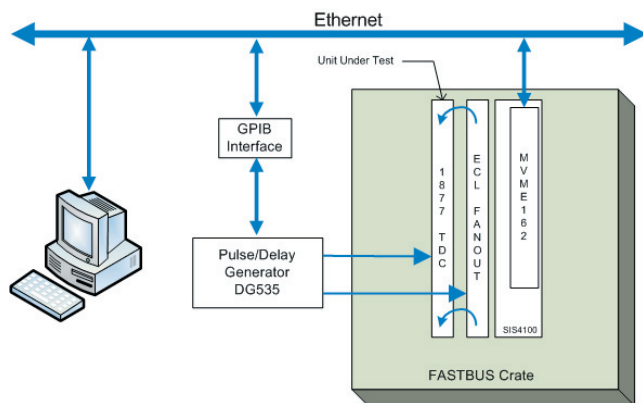


FIG. 1. Fastbus test station block diagram.

Ethernet connects the PC to the Fastbus crate through the SBC. The GPIB-Ethernet interface enables communication between the PC and DG535, which provides the COMMON signal to the TDC module and the input signal to the ECL fan-out module that in turn provides 96 individual differential ECL input signals, one for each channel of the TDC module, which works in either a common start or common stop mode.

Each channel of the TDC module is capable of recording time-data from multiple-hits up to a 32.768 μ s programmable time-range. During the time-range, the first 16 signal transitions (edges)—this number is programmable—can be recorded. Each channel may be programmed to detect rising or falling edges. To be recorded as distinct edges, the time separation between two adjacent edges must be at least 20 ns. Recorded data is stored in a Last In First Out memory. The TDC can hold up to eight triggers in memory.

Upon power-up of the SBC, VxWorks [3], and *server.c*, a C

program, are loaded on the SBC. *Server.c* monitors the Ethernet TCP/IP connection for incoming Fastbus commands and services basic commands such as read, write, and initialize.

Test routines are LabVIEW-based [4] and communicate with the crate via the PC's Ethernet TCP/IP connection and control DG535 through the GPIB-Ethernet interface.

TDC functions can be tested in either internal or external mode. When running the test station in the internal mode, after initialization, the TDC module is issued a master reset and the conditions of the control and status registers are checked. Then the TDC as programmed generates internally a burst of pulses to fill the event buffers with data. Recorded event time is read back and analyzed as are the geographical address, parity, buffer number, sign edge, and differential timing between the edges. Recorded data is written to an Excel spreadsheet. If errors are detected, the program is halted and the errors are logged.

If internal tests are successful, TDCs are tested with start and stop signal pulses generated external to the TDC module. For the external tests, the TDC is initialized and external timing pulses generated by DG535 are distributed to the TDC inputs by the ECL fan-out module. The remainder of the test is identical to the internal test. The internal/external test sequences are repeated as needed by the user.

The LabVIEW-based graphical user interface consists of test instructions, documentation, graphs, and two user-control screens that can be chosen from the tabs at the top of any of these screens. The test instruction screen shows equipment and cabling used and steps for conducting the tests. The documentation screen provides information about the equipment and web site links. The graphs screen, Fig. 2, displays the test results and the minimum, maximum, mean, and standard deviation for differential timing signals. Program options are set and test progress and errors are reported on the expert user or the basic user control screens.

The basic user screen, Fig. 3, has bar graphs that report progress of the internal/external tests. The screen also has the control settings for choosing the TDC Fastbus slot, test mode (internal/external), number of times for the test to be repeated, the VME SBC hostname, and DG535 ID.

The expert user screen, Fig. 4, offers control options for the TDC, such as common start or stop mode, timeout duration, single or double edge acquisition, single or block Fastbus reads, the number of edges to be stored per trigger, test pulse duration, and the acceptance window for the signals.

The user has the option of writing results to an Excel spreadsheet. A text message window that reports the operating state of the program, as well as help documentation is available during execution.

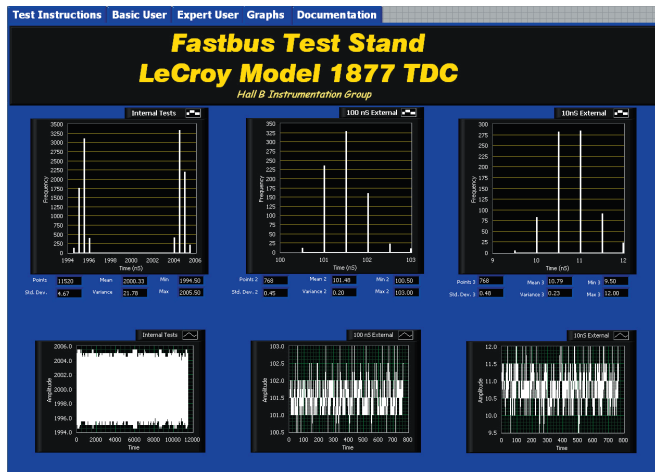


FIG. 2. LabVIEW graphs screen.

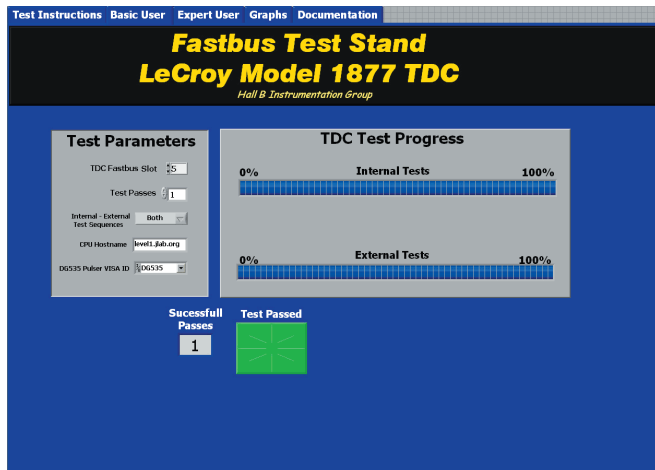


FIG. 3. LabVIEW basic user front panel screen.

In conclusion, the new, versatile FTS for the LeCroy model 1877 Fastbus TDC modules has been designed, programmed, and implemented. FTS has been used to test available spare TDC modules and has found one spare unit defective. FTS can be expanded to test other types of Fastbus modules.

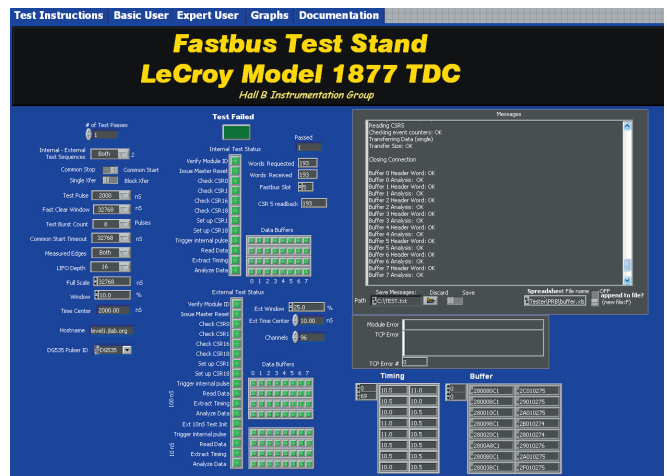


FIG. 4. LabVIEW expert user control panel screen.

- [1] Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282.
- [2] Stanford Research Systems, 1290-D Reamwood Avenue, Sunnyvale, CA 94901.
- [3] Wind River Corporation, 500 Wind River Way, Alameda, CA 94501.
- [4] National Instruments Corporation, 11500 N Mopac Expwy, Austin, TX 78759-3504.