

Proposal to Study a Section of the Silicon Vertex Tracker Envisioned for CLAS++

Amrit Yegneswaran, Mary Ann Antonioli, Peter Bonneau, Tanest Chinwanawich, Brian Eng, Tony Madany,
Marc McMullen, Armenak Stepanyan
Physics Division, Thomas Jefferson National Accelerator Facility, Newport News, VA 23606
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Hall B is studying the prospect of installing a silicon vertex tracker (SVT) in CLAS++. This note presents project-status, goals, cost, schedule, and labor estimates for the proposed study.

Physics motivation, a tentative design, and project-status of the SVT are given in references [1, 2]. As envisioned at present, the SVT, anticipated to have ~50,000 channels, will consist of six sectors, Fig. 1. Each sector will consist of three regions. The silicon-sensors of each region will consist of a rectangular section, parallel to the beam axis, that abuts a trapezoidal section which is at 45° with respect to the beam axis. Each section will have two (u, v) super layers angled with respect to each other at ~5°. Silicon-sensors' thickness and pitch will be ~300 μm.

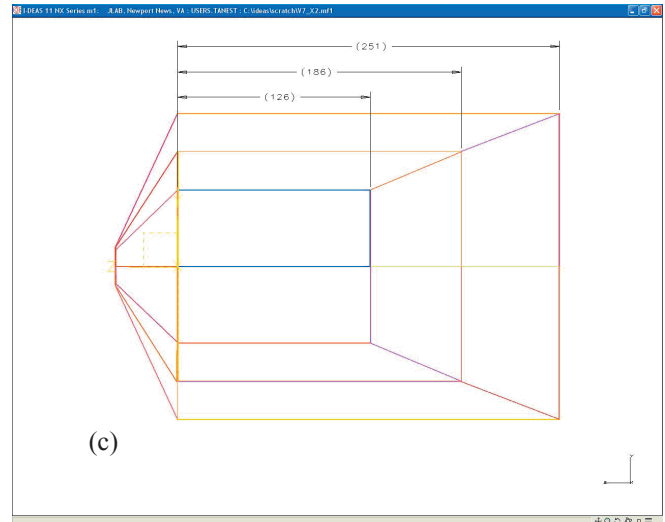
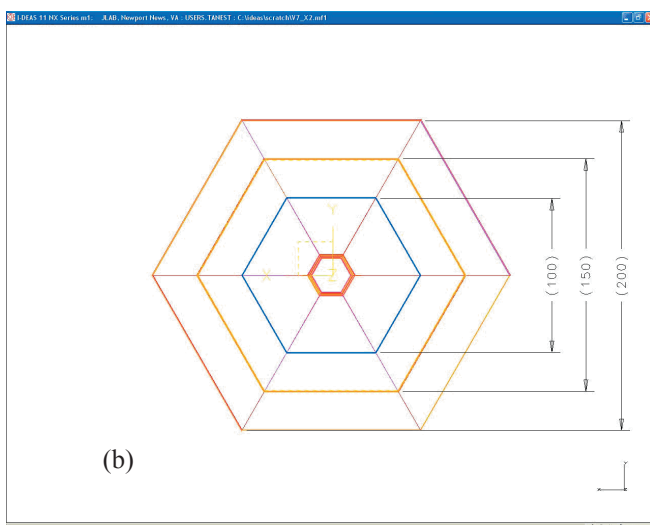
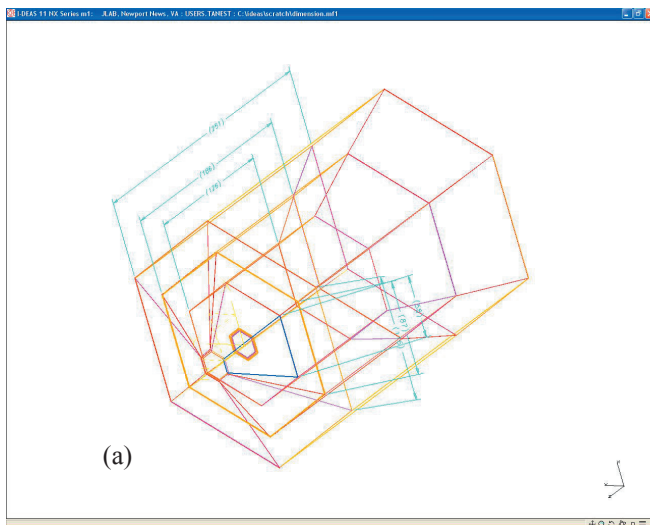


FIG. 1. SVT conceptual design. All dimensions are in millimeters. (a) isometric view, (b) end view, (c) side view.

Readout electronics will be based on CDF's SVX4 chips [3]. Each chip has 128 channels and each channel has a 42-cell analog pipeline. The front-end (detector-end) acquisition rate is ~10MHz.

Figures 2 and 3 show momentum and impact parameter resolutions, σ_p/p and d_o , for protons as a function of the

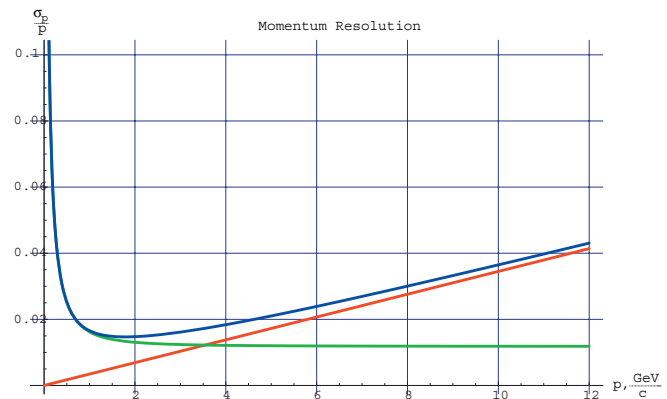


FIG. 2. Red line—spatial component of σ_p/p , Green line—multiple scattering component, Blue line—sum of the two components. Angular resolution, σ_θ/θ , due to finite read-out pitch has been disregarded.

proton's momentum, p . At 5 GeV σ_p/p is ~ 0.02 and d_o is $\sim 18 \mu\text{m}$. Input values for the estimates were: magnetic field ($|\mathbf{B}| = 5 \text{ T}$), single point resolution ($a = 10 \mu\text{m}$), percentage of radiation length of the silicon sensor and associated components for all three regions ($p = 2.5\%$), radial distance of the first region from the target ($r_1 = 0.04 \text{ m}$), inter-region spacing ($d = 0.4 \text{ m}$), number of position measurements ($n = 3$), and angle of incidence of proton on detector ($\theta = \pi/2$).

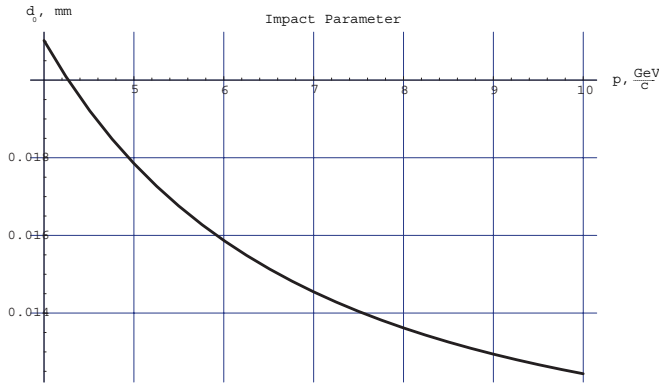


FIG. 3. Impact parameter resolution as a function of its momentum.

Simulation based on GEANT4 [4] has been started to study occupancy and angular and vertex resolutions. An initial working model, albeit with minimal physics, has been developed, Figs. 4 and 5.

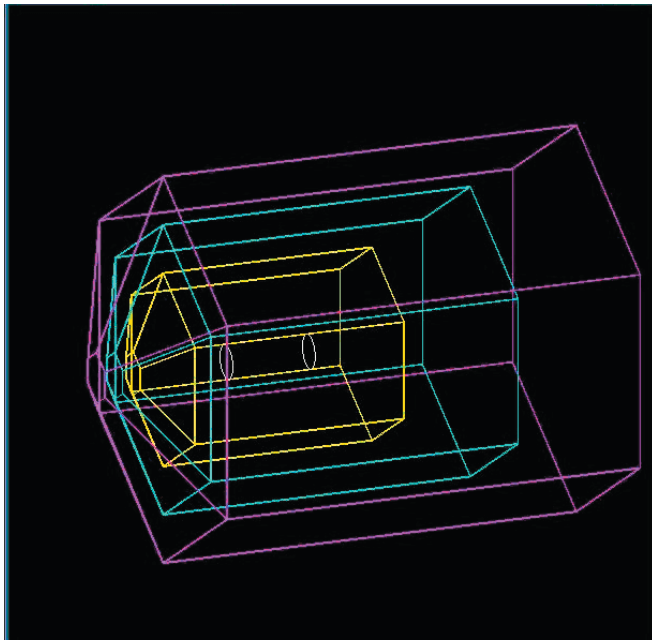


FIG. 4. GEANT4 geometric model of detector.

Figure 6 shows a rendering of the SVT in I-DEAS—the software package being used for the design and finite element analysis of the flange that will attach the detector to the beamline. Figure 7 shows the stress on the conceptual mounting flange.

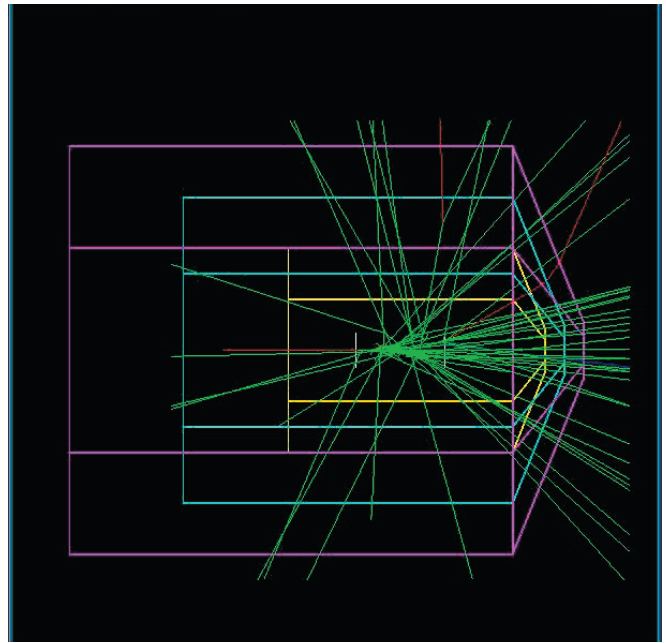


FIG. 5. GEANT4 example run ($E_p = 500 \text{ MeV}$, $B = 2 \text{ T}$).

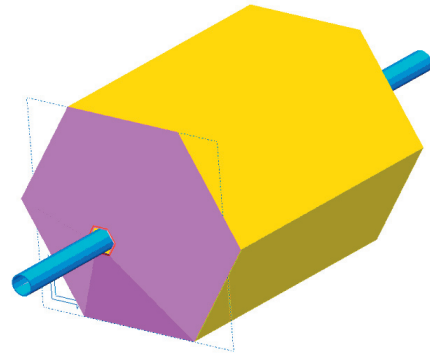


FIG. 6. I-DEAS rendering of the SVT.

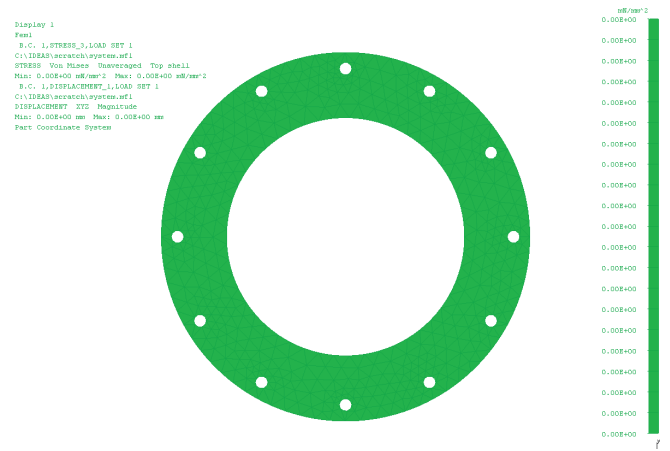


FIG. 7. The visualization of results shows that the mounting flange can support the weight of the SVT and bracket system. The green color indicates that the metal is not stressed.

Figures 8—11, from CDF’s Technical Document Review, show the components and dimensions of the stave (~3,000 channels) that is planned to be used in lab and beam tests for R&D of the project. Figure 8 shows a photograph of the stave outfitted with the necessary electronics.

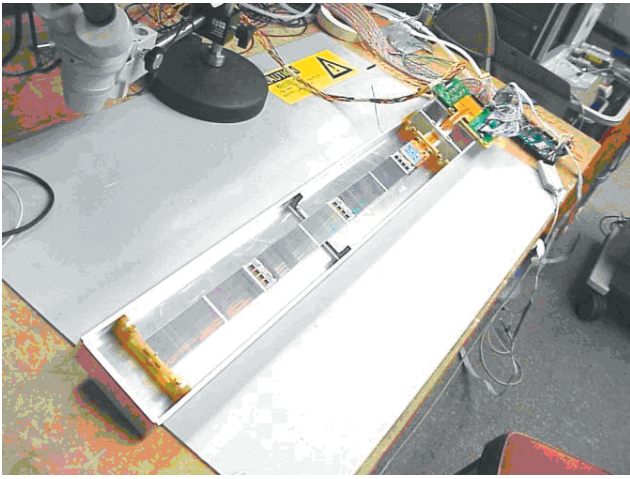


FIG. 8. Stave.

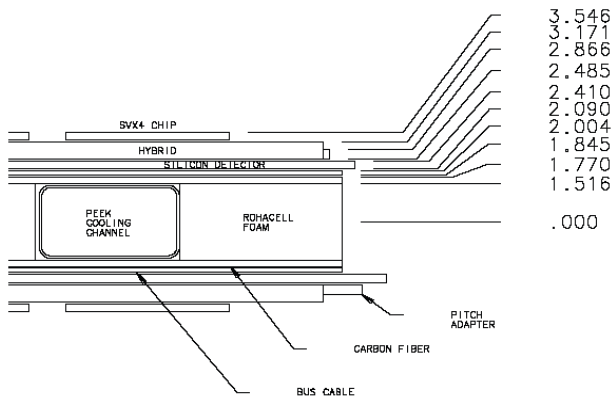


FIG. 9. End view of stave. Dimensions are in millimeters. The total thickness of the stave is 7.092 mm.

Figure 10 shows the unfolded view of the stave. Notice there are three pairs of silicon sensors for each super layer, each pair of sensor with its own HV connection pads and readout chips. The total length of the stave is 592.000 mm. The width is 39.500 mm.

Figure 11 shows the various percentages of radiation length for different paths through the stave.

A schematic of the test stand is shown in Fig. 12. The PCI Test Adapter (PTA) has 2 Mb of on-board memory and an Altera APEX EP20K200e FPGA, and the Programmable Mezzanine Card (PMC) has a Xilinx Vertex II XC2V 1000 FPGA. Both boards, designed at Fermilab, plug inside a PC with a PCI bus.

The FPGAs can be programmed to send control-signal-patterns to the test hardware and can collect generated data, which the host computer will analyze and evaluate.

The ROOT-based DAq, RootXTL, allows users to run several tests of SVX4 chips, hybrids, or staves and makes

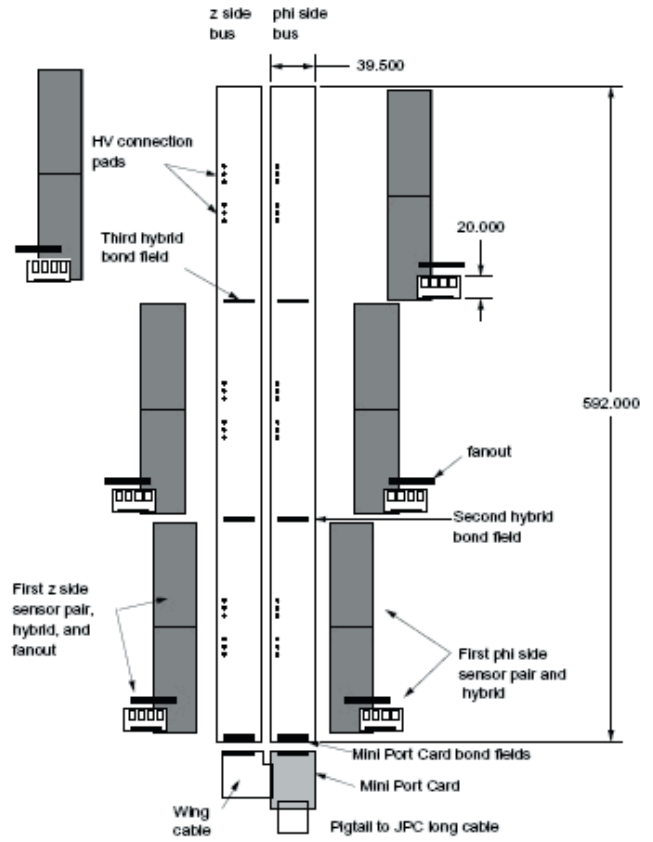


FIG. 10. Unfolded view of the stave.

Material Model for stave/bus design V1.0 27-Aug-2001 Carl Haber refer to spreadsheet for layer thickness and properties, shown are % of a radiation length for various particular paths through the structure.

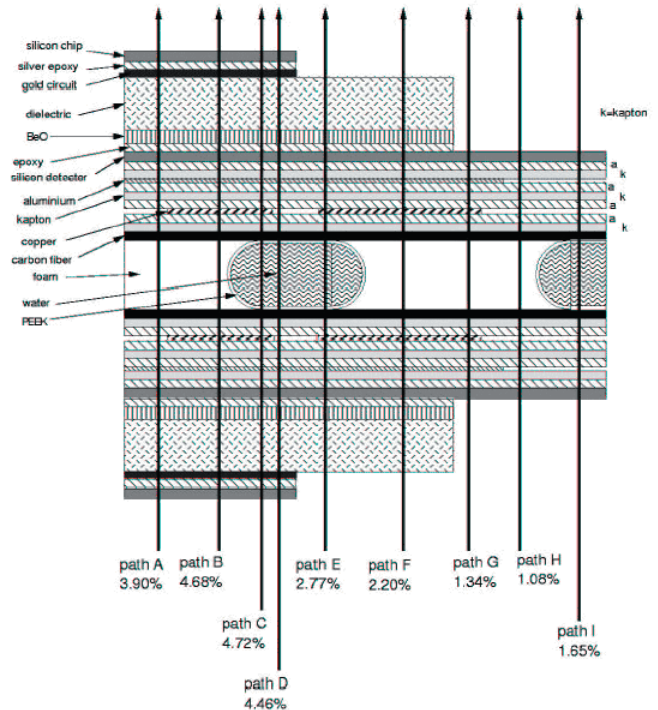


FIG. 11. Percentage of radiation length for different paths.

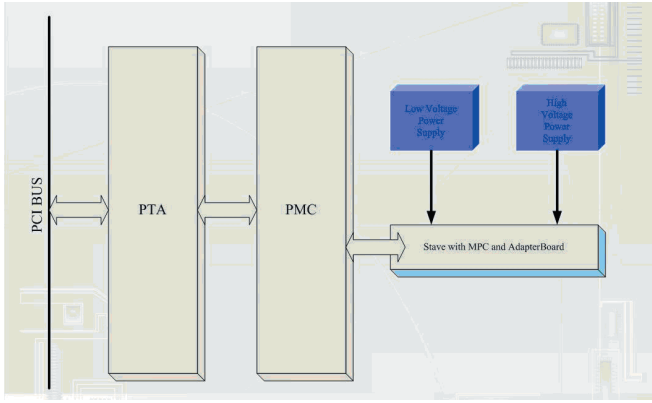


FIG. 12. Test stand.

representative plots such as pedestal and differential noise. Understanding the DAQ is necessary to convert acquired data into CODA format so that the data can be analyzed with A1 or RECIS.

Lab tests will evaluate chip efficiency and data quality ac-

quired under various input conditions. Beam tests will study the effects of the Moeller background on the detector, occupancy, and rates effects. Acquired data will enable the investigation of vertex and angular resolution. Detector assembly techniques will be investigated.

Fermilab estimates the price for the stave and peripheral components to be ~\$16,000, Table 1. Additionally, an adapter board, a low voltage power supply, (~ \$2,000), and a high-voltage power supply module (~ \$8,000) have to be procured. This reckons to ~\$30,000.

After receiving the stave, about six months are anticipated to complete the tests. A rough time line is:

- 01/15/05 receive stave
- 02/01/05 complete setup
- 05/15/05 complete lab tests
- 06/01/05 install stave in endstation
- 06/15/05 complete beam test
- 07/15/05 complete first draft of report

This schedule depends on the performance of CLAS during the above mentioned period.

Part	Number	Unit cost	Cost	
Silicon Sensors	12	\$420.00	\$5,040.00 Req. 162504	
Hybrids	6	\$975.71	\$5,767.74 Cost transfer on 22 Mar 04	
Bus Cable	2	\$150.00	\$300.00 Req. 164992	
Mini-port card + 3 cables	1	\$750.00	\$750.00 Req. 162233	
Mechanical stave core	1	\$455.00	\$455.00	
Stave Storage Box	1	\$400.00	\$400.00	
Total			\$12,712.74	
Assembly Step	Hours	Labor/hour	Frequency of step	Cost
glue sensors with kapton	1	\$50.00	6	\$300.00
wirebond sensors	1	\$50.00	6	\$300.00
Prepare stave core	2	\$50.00	1	\$100.00
lamine bus cable on stave core	1	\$50.00	1	\$50.00
mount module on stave	1	\$50.00	6	\$300.00
wirebond stave	0.5	\$50.00	1	\$25.00
Total				\$1,075.00
Indirect charges				\$2,366.66
Grand Total				\$16,154.40

TABLE I. Fermilab's estimate of stave cost.

To estimate required labor, the work load is partitioned as: procurement, design and fabrication of components, setup of test-station and DAq, data analysis, and design and development of mechanical apparatus for installation in the end station.

To complete proposed lab and beam tests within given time scale, it is estimated that at least four FTEs will be needed. Note, estimate does not include simulation or finite element analysis. Since, Hall B Instrumentation personnel will contribute significant portions of their time to the project, the estimated FTE count could be reduced to perhaps two.

The two phases, lab tests and beam tests, will help initi-

ate the understanding of all aspects of this complex detector — from assembling and installing to acquiring and analyzing the data.

- [1] CLAS++ Conceptual Design Report V. Burkert *et.al.*
- [2] Status Report on the Prototyping of Silicon Vertex Tracker, Tanest Chinwanawich *et.al* CLAS-Note 2004-29.
- [3] SVX4 User manual L. Christofek *et. al.* ; SVX4 Front End Tom Zimmerman.
- [4] Silicon Vertex Tracker's Simulation Status, M. Hallapana-var *et.al* CLAS-Note 2004-13.