CLAS-NOTE-93-014

# Tests of Pre-production LeCroy 1872A TDC

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## 1 Introduction

Work has been done to check the Pre-production LeCroy 1872A against the specifications desired [1] for such a TDC module. The module is one FASTBUS slot wide and accepts up to 64 signals in groups of 16. Each input signal is provided through differential ECL twisted pair cables. In addition to the 64 individual STOP inputs, there are also similar inputs for common START and Fast Clear signals. Outputs include a Conversion In Progress (CIP) signal on the front of the module and "Hit" signals out of the backplane for intended use with the CLAS second level trigger. A "Hit" channel is one that receives a valid STOP signal within the active times range of the TDC. It should be noted here that the data here represent the performance of the most recent version of the 1872A that has been delivered (two have been received), unless otherwise specified.

## 2 TDC Measured versus Specifications

Most measurements were made with CODA [3], using a pulser to generate inputs (22 nsec in duration) for the TDC and other related electronics. See Figure 1 for electronics setup. Other measurements were made directly from an oscilloscope (Tektronix model 2467B).

### 2.1 TDC Inputs

#### 2.1.1 Interchannel Isolation

Each individual channel on the TDC should be isolated from the others such that an input from another channel should not change the digitized value of that channel by more than one count. To check this, the values for the

individual channel by itself were compared to the values when another input is located in either the preceding or following channel. Other tests of this sort were done, such as placing a number of extra inputs into neighboring channels, adding delay to a neighboring input, and moving the extra input up to 4 channels away from the original. Overall, the change in the values for any of these tests were $\leq$2.0 counts (100 psec), with .625 count (31.25 psec) being the average change. See Figure 2.

### 2.1.2 Fast Clear

If a clear signal is received during a period between the STOP signal and conversion, called the Fast Clear Window, the board should be able to be reset itself and be ready for new data within 1 $\mu$sec. The duration of the Fast Clear Window should be adjustable between 1 and 4 $\mu$sec. In testing for these features, it was first seen that a clear signal sent during the Fast Clear Window did indeed stop the board from doing any conversions. Next, it was seen that the duration of the Fast Clear Window could be internally adjusted between 1 and 4 $\mu$sec, satisfying the requirements specified.

## 2.2 TDC Outputs

### 2.2.1 Conversion In Progress

The CIP is an output signal which indicates when the TDC is engaged in a digitization process. This signal gives logical true when digitization is in progress and logical false when there are no hits on the board. The conversion time, as determined by the CIP is 10 $\mu$sec for the first hit channel plus 3 $\mu$sec for each additional hit.

### 2.2.2 Hit Register

Hit channel data should be available through the backplane of the TDC within approximately 100 nsec of the start of the Fast Clear Window. These signals are read from a single pin. When triggering on a STOP signal, it was seen that there was a "time-out" of about 400 nsec between the STOP and the hit data. This period has been considered acceptable. The actual hit data are available on the backplane until after conversion has ended or until the reception of a Fast Clear signal.

### 2.2.3 RMS Spread

The root-mean-square (RMS) spread for an individual channel should be less than 50 ps over the whole dynamic range. The RMS spreads were measured to be $\leq$1.129 counts (56.45 psec) with .858 counts (42.9 psec) being the average spread. We have assumed the nominal calibration value of 50 psec/count. See Figure 3.

## 2.3 Active Range

The active range of the TDC should be at least 150 nsec, and the specifications for calibration should hold over the entire range. When measured, the active range of the TDC was shown to be 150 nsec, satisfying the specification, with the TDC data losing its linearity past this point.

## 2.4 Calibration

### 2.4.1 Single Channel

The TDC should convert time (STOP time - START time) to counts with a RMS resolution of less than 50 psec (1 count) over the entire active range for each channel. A quadratic fit was done for data, covering a 150 nsec range (64 nsec to 214 nsec) for each channel, giving an average deviation of $\leq$1.18 counts (59 psec) over the active range of a single channel. See Figure 4 for deviations of individual channels. A more accurate calibration should still be done, as the method of varying the delay between START and STOP pulses was a NIM delay module which may not be completely accurate to the degree needed here. An example of a typical calibration expression (channel 4 for example) is shown below,

$$T = -1997.6 + 20.689 * t + .00302 * t^2 \quad (1)$$

where T is the number of expected TDC counts, and t is the input time measured in nsec.

### 2.4.2 Channel-to-channel Variations

The linear calibration term from channel to channel should vary by less than $\pm$ 5%, and it was found that this term in fact varied by 2.4%, satisfying this

specification. See Figure 5.

## 2.5 Conversion and Readout Times

After a STOP signal is received, it is specified that the TDC should be ready for another event in no more than 30 $\mu$sec after this first STOP signal. It has been assumed that for a given TDC, there will be eight valid hits per conversion period. The method chosen by the manufacturer for meeting this time limit is to have a multi-hit first-in-first-out buffer, which can hold eight events at a time. The buffer can be read while the TDC is converting. For each set of hits, there is a 10 $\mu$sec set time for conversion processes (one hit only) plus an extra 3 $\mu$sec for each additional channel that received one of the hits (as can be seen by looking at the CIP output). For eight hits, this would give a total conversion time of 31 $\mu$sec as compared to the 30 $\mu$sec specified. See Figure 6 for an overall view of the relative timing of the START, STOP, FCW, and CIP signals.

## 2.6 Enable Time

The enable time is the minimum time needed between common START and STOP signals for the board to turn on and register the event. It has been specified that this time should be less than 30 nsec. When measured, however, it was found that the enable time of the second board was about 59 nsec. The first board had an enable time of 35 nsec (this was confirmed by LeCroy [2]), and it is not clear at this time why it was changed. The fact still remains that neither board conforms to the 30 nsec specified, and this problem should be addressed on future prototypes.

# References


[1] Elton Smith, "Specification 66340 - S - 00846 — Time-to-Digital Converters for Time-of-Flight Measurements With the CEBAF Large Acceptance Spectrometer," July 7, 1992.

[2] LeCroy Corporation, "1992 Research Instrumentation Catalog," October 1991.

[3] "CODA — CEBAF On-Line Data Acquisition, User's Manual," version 1.1.3, September 3, 1992.

# List of Figures

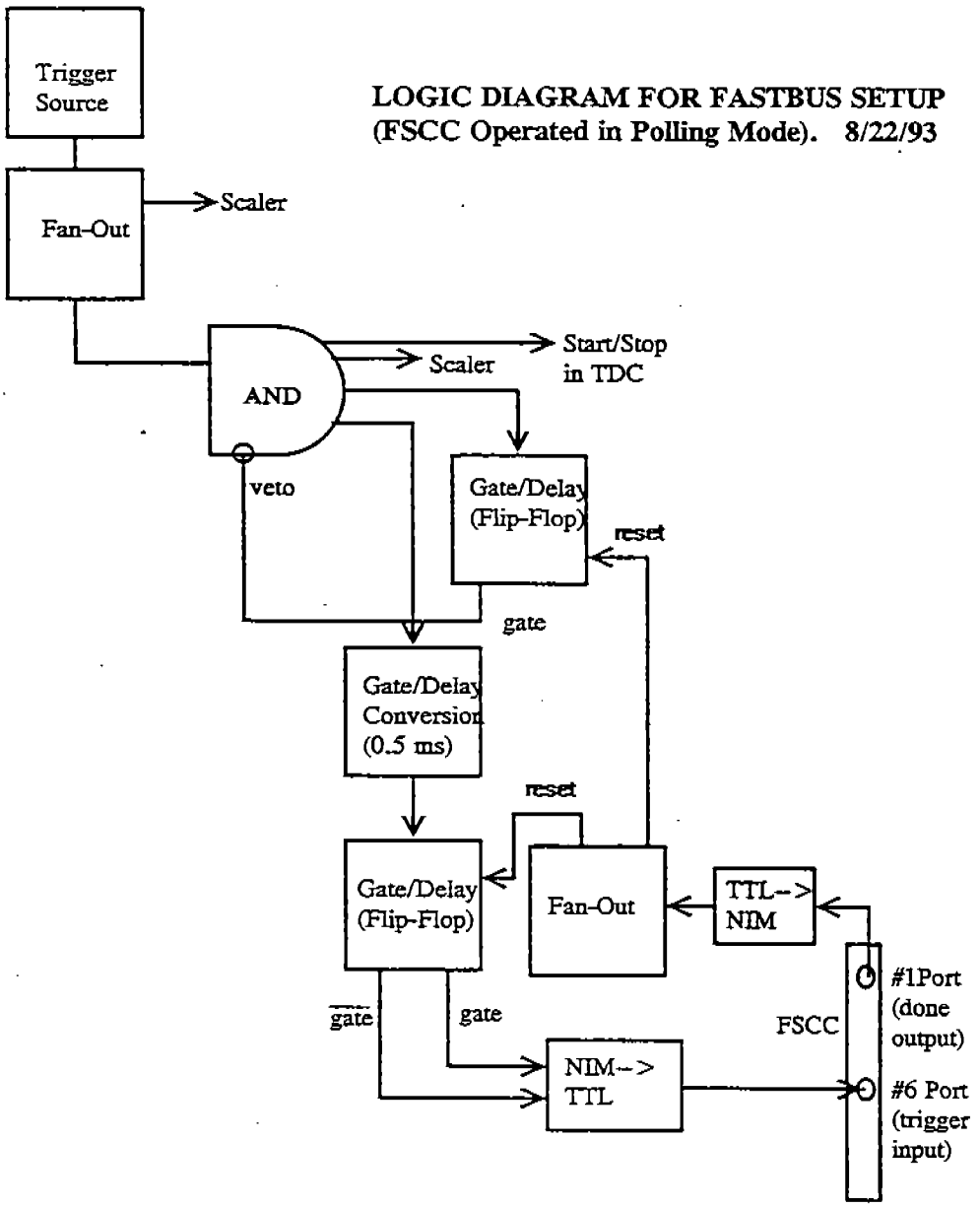


Figure 1: Setup for tests with LeCroy 1872A.

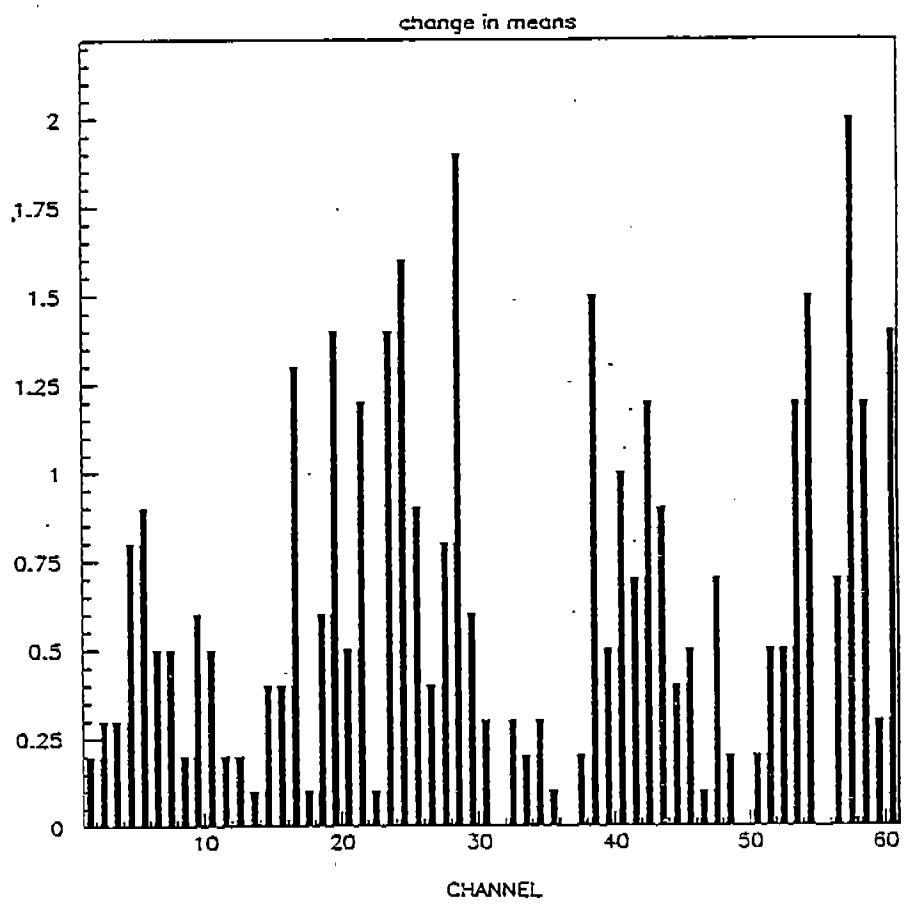


Figure 2: Change in the means of each channel (interchannel isolation).

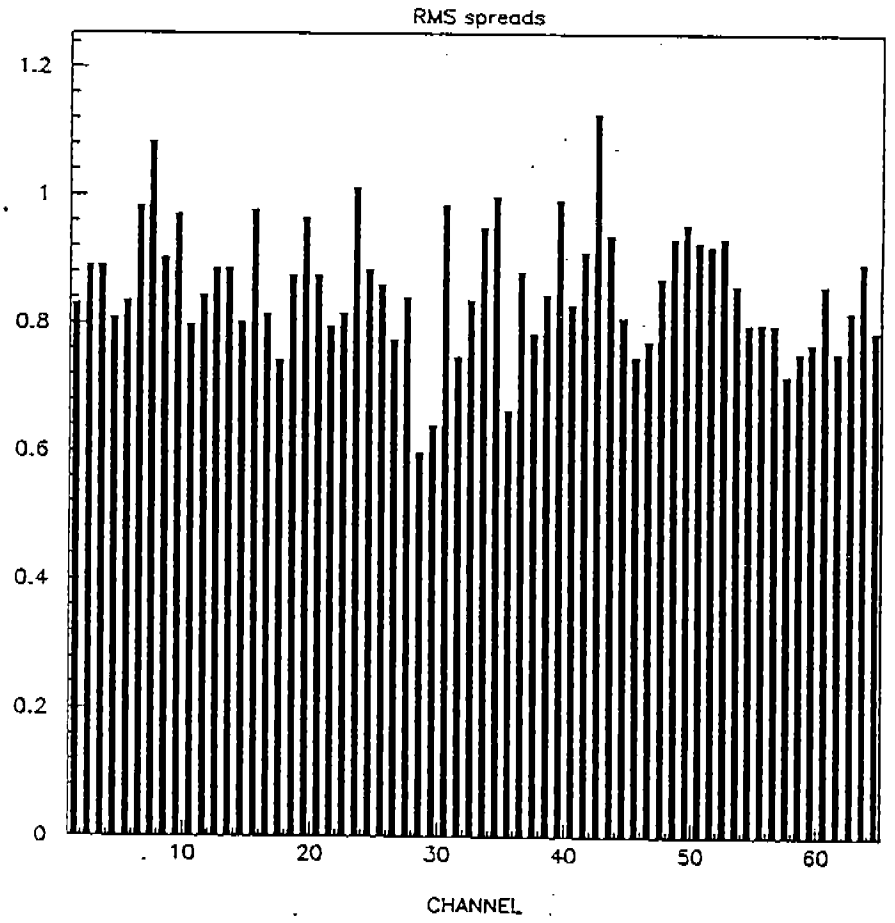


Figure 3: RMS spread.

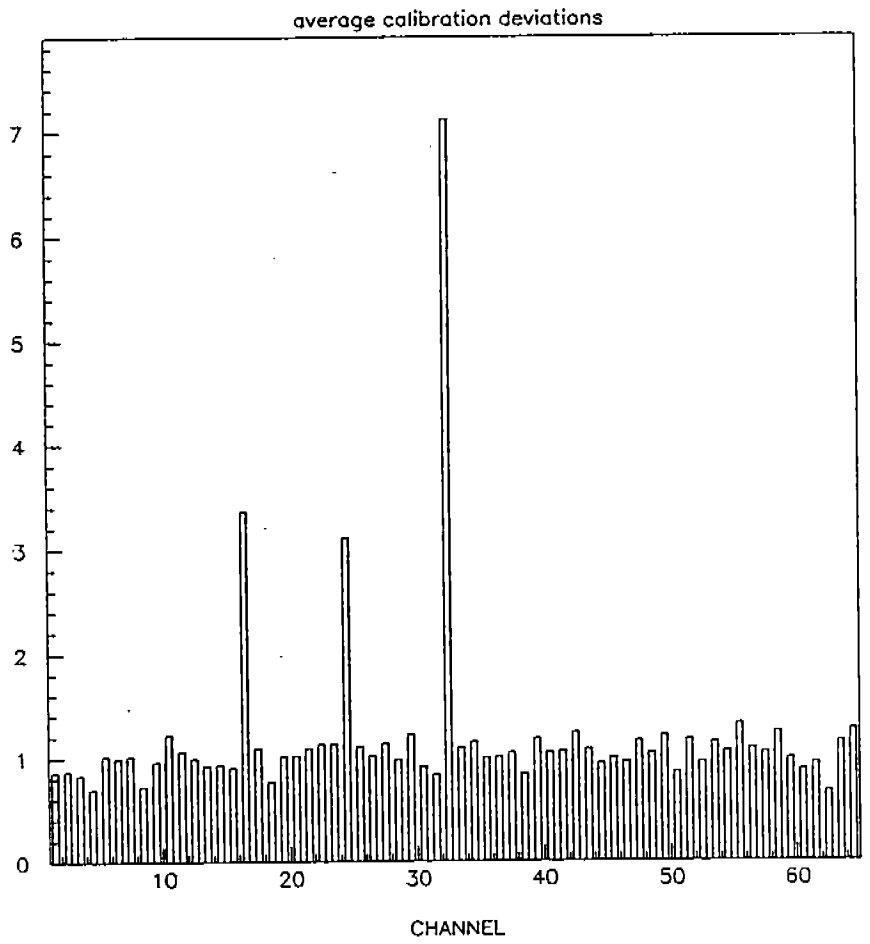


Figure 4: Average deviations from calibration.

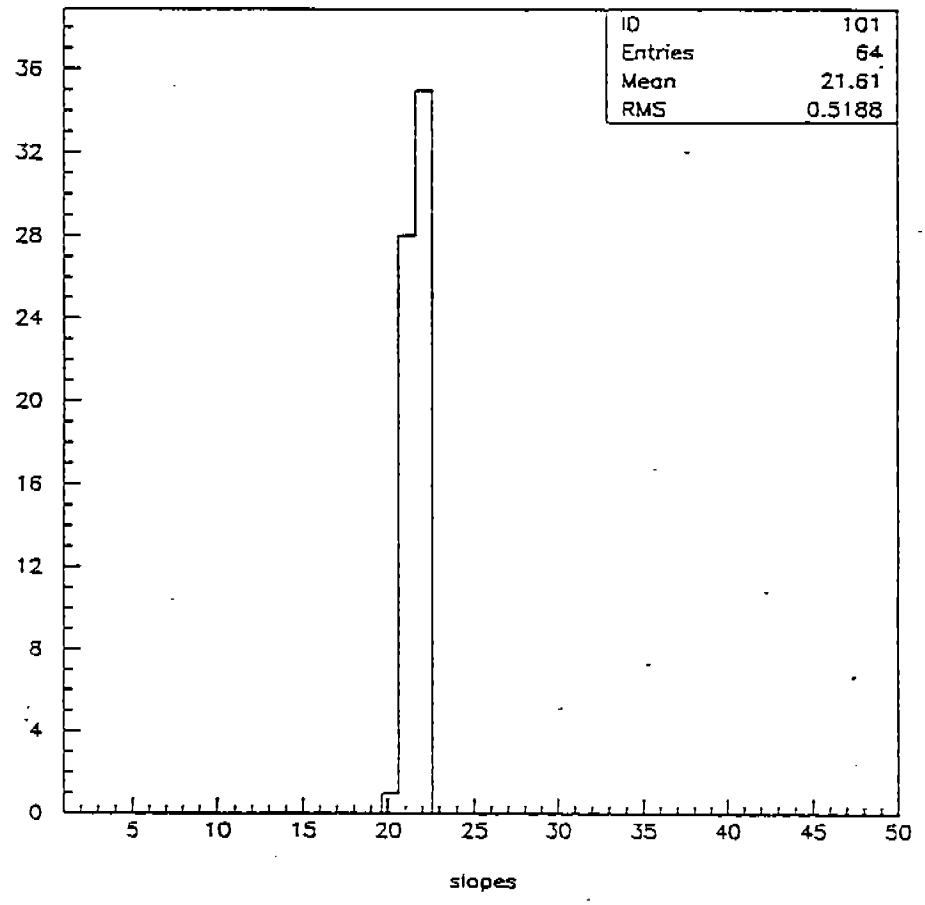


Figure 4: Linear calibration terms (slopes) in counts/nsec.

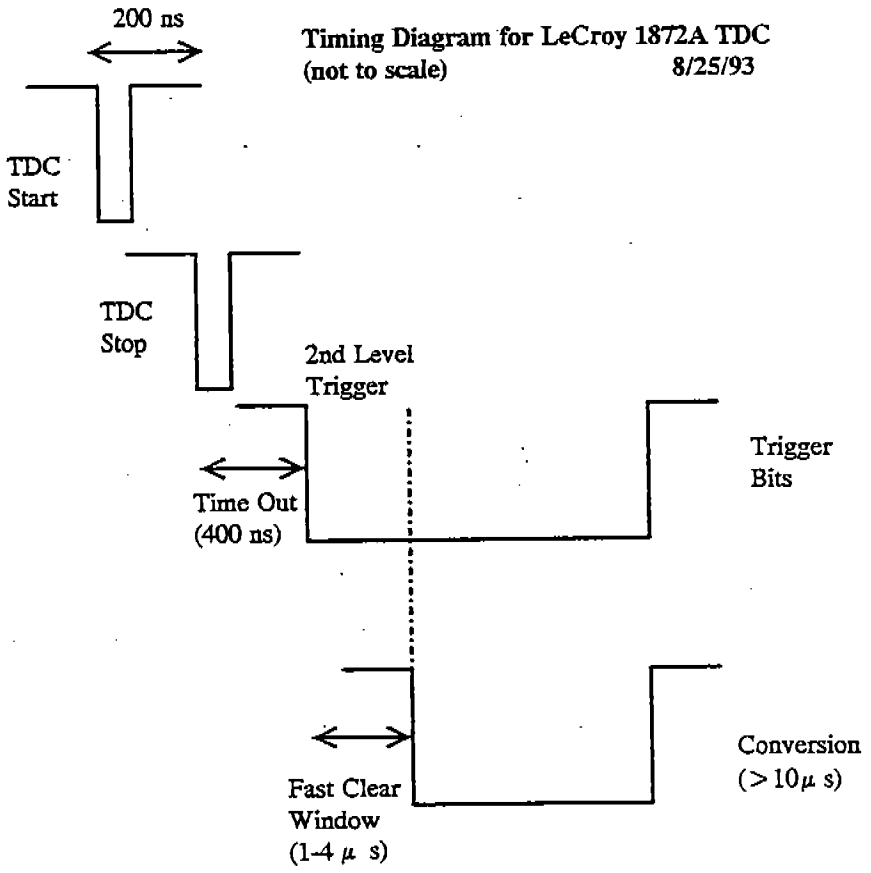


Figure 6: Timing of START, STOP, FCW, and CIP signals.