CLAS-NOTE-94-025

Tests of the LeCroy 1881M ADC for Digitization of CLAS PMT Pulses

Michel Guidal, Elton S. Smith and T.Y. Tung

December 19, 1994

The purpose of this note is to describe the procedure used to test and calibrate the LeCroy 1881M Analog-to-Digital Converter (ADC) FASTBUS module and present results of those tests. The performance specifications [2] were determined by the requirements of the CLAS [1] detectors using fast photomultiplier tubes (PMT's). CLAS has 2496 channels of ADC's and therefore an automatic testing procedure is required. Similar tests running CODA [3] have already been developed for the CLAS Time-to-digital Converters (TDC's) [4]. The goal was therefore to adapt the extisting hardware and software setup to the ADC's, but keep the aparatus operational for the TDC's.

The LeCroy 1881M is a 64-channel, 13-bit ADC packaged in a single-width FASTBUS module [6]. This module has a fixed conversion time of 12 μsec. Inputs channels with no data may be sparsified at readout to reduce data volume and transfer time.

1 Test Procedure

The testing procedure consists in producing a sequence of test signals from a CAMAC Phillips [7] 7120 QTG calibration module (16 bit DAC, 0-600 pC range) and read from the ADC via the FSCC FASTBUS Controller with CODA. The calibration module also generates a gate for the ADC and a signal which is used to produce a trigger for the FSCC with NIM logic. The sequences generated by the QTG and recorded by the ADC are written on files which can be compared and histogramed. The general setup and method are described in Ref. [4]. We will just discuss the subjects which are relevent to the ADC test.

1.1 Hardware

For the generation of the analog signals, we used the *charge* output of the QTG. It was directly linked through a NIM-ECL wire to a single ADC channel. The ADC gate was generated by the *gate* output of the QTG and a Phillips 726 NIM-ECL level translator. The gate was input via TR1 and TR2 using the FASTBUS Signal Distribution Card [5]. Taking advantage of the existing TDC setup, we used the *start* output of the QTG as the trigger. Parenthetically we note that to operate the QTG 1) the *charge* (Q) mode was enabled, 2) the *charge DAC* set to *CAMAC* and 3) the *time DAC* set to *Manual*. **It is important that the inhibit light of the CAMAC controller be OFF** before starting a run. Otherwise, LAMs are inhibited. The QTG range should be set to 600 pC, corresponds to 0.009154 pC/count. At present, the system is set up to read out a single ADC channel of one ADC module plugging in a preselected slot. The slot ID to be used is programmable.

1.2 Software

The computer used is clas72, an HP-715/75 workstation. CODA-1.3b is the data aquisition software. Special utility software exclusively developed for this particular type of test have been also used, such as Camac: Program to control QTG; Calibrate: Analyzer for the test data; CoEvb_unpack: Unpack the TDC or ADC data.

At present, the top dircetory for these tests is named /clas/clas72/usr/local /COSMIC, with three subdirectories named CODA_rc, DATA, Utility as the next level. The user is not required to have any knowledge about the directory tree. A cosmic group member can operate from the /clas/clas72/usr/local /COSMIC/CODA_rc/bin subdirectory using executable script files. Working knowledge for configuring CODA is necessary for advanced users who wish to move the module to a different slot or add new runtypes, etc.

For casual users, the following executable scripts are useful for our purposes.

- **doruncontrol**: Set up everything and pop out *Run Control* window.
- **doxcefdmp**: Pop up the xcefdmp window.

- **docamac**: Calling *RunCamac* to provide an interface between the user and the CAMAC Crate.
- **docamacADC**: Calling *RunCamac* to provide an interface between the user and the CAMAC Crate, this script will take the preselected option value from a file for 1881M ADC 13-bit test.
- **CalibrateTDC**: Offline analysis for a TDC calibration run, find scale and offset.
- **CalibrateADC**: Offline analysis for a ADC calibration run, find scale and offset.
- **diff_linear**: Offline analysis for a diffential nonlinearity test run, was decoupled from the old *Calibrate.exe*.

These scripts may be executated by typing their names on the terminal or double clicking on your file manager window. These script file have improved efficiency. As a result, a calibration can be done in less than 30 key strokes and mouse clicks and takes less than 10 minutes including analysis. In the future, we wish to develop a dedicated graphical interface to fit in these script files. During the course of getting things to work for LeCroy 1881M ADC, we had to fix many bugs and upgrade for the Utility programs. At present, the Coevb_unpack and Calibrate are adequate and reliable for testing both LeCroy 1881M ADC and LeCroy 1872A TDC. Certainly, as other software projects are, bug fixes and upgrades will continue.

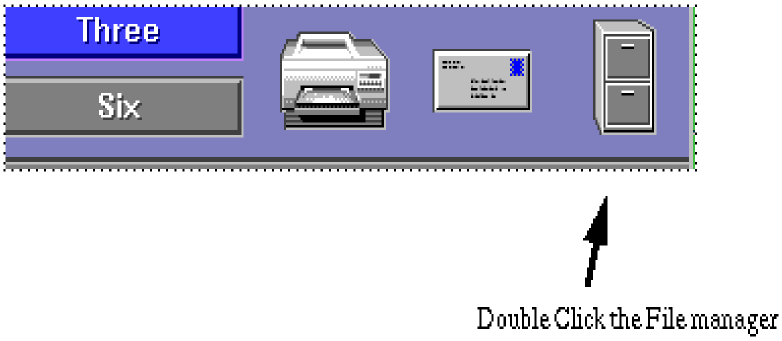
1.3 Calibration Strategy

Similar to the TDC calibration, the values of QTG counts for each event is required in the offline analysis. *RunCamac* saves these values to a file at the time it commands the QTG to generate a preprogrammed pulse. The *Calibrate*, which is called by CalibrateADC then compares the QTG file and the obtained ADC data. We therefore are able to obtain the calibnration constants. Both *Calibrate* and *RunCamac* have double digit number of options to set, the values of the options are related to the appications. The options can be set either interactively or using Unix command piping. The script files described in previous subsection apply the Unix command piping.

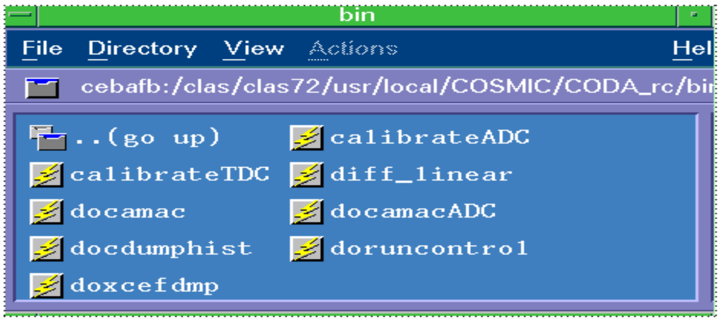
1.4 Operation

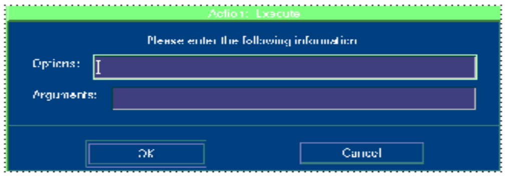
After the hardware is set up, the following procedures must be followed to calibrate the ADCs:

- Logon to a cosmic group account on clas72 from a terminal supporting HP VUE.
- Pop-up the VUE file manager window by double clicking left (right) button of the mouse on the two-drawer icon as below.

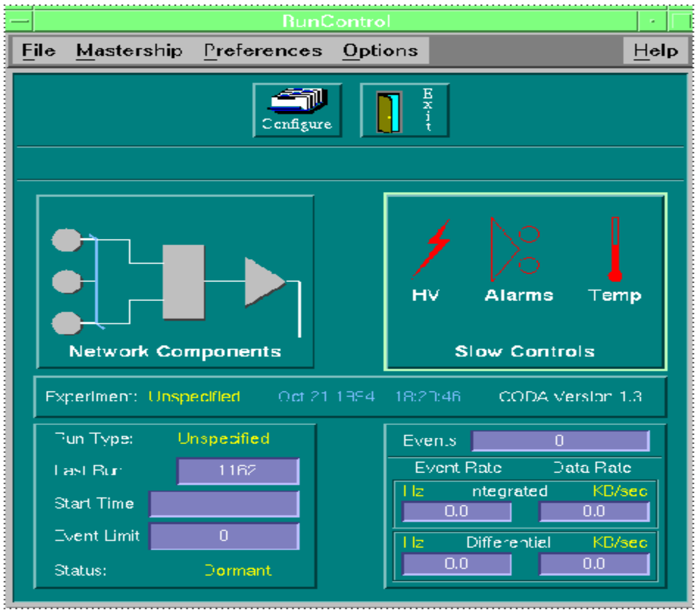


- Use the file manager to change directory to /clas/clas72/usr/local /COSMIC/CODA_rc/bin. Find "doruncontrol" and double click it. A second window appears, then click the OK button. This script runs the CODA *RunControl* program, details of which may be found in [3].

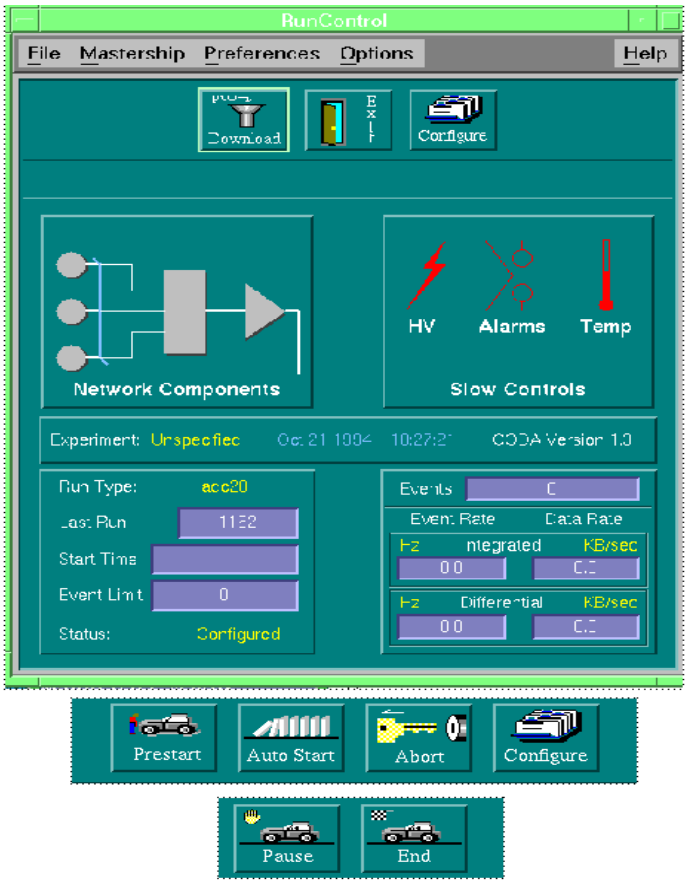




- The *Runcontrol* window appears as shown below. Click on "Configure," and a second window will pop-up. When the module to be tested is in slot 20, the run type to be used is "adc20."



- After acknowledging "OK" in the small window, the status of *RunControl* is changed to "Configured ". We are now ready to download the FASTBUS readout list to the FSCC, which is accomplished by clicking on the "Download" button. *RunControl* will then change to " Downloaded " status. The top panel will change to allow the user to Start (or Abort) the run. Click on "Auto Start" and data taking is enabled. The top panel will change to allow operator to "Pause" or "End" the current run. No triggers are yet taken, however, since these are controlled by the *RunCamac* program.



- The data acquisition system is ready to take data now. We need to start *RunCamac* to generate the desired trigger sequence and corresponding data to the ADC. The user needs to double click on "docamac" from the file manager window. An X-window will pop-up, and the user can set options from there. The default values are for 13-bit operation.

- The system can run a rate of about 20 Hz. The user should click on the "End" button in the *RunControl* window after *RunCamac* is finished. Select "calibrateADC" from the file manager for analyzing the integral linearity. Or, alternatively, select "diff_linear" from the file manager if the run is to check the differential non-linearity of the ADC. In either case, the results are stored in a postscript file named " adc.metafile " created in /clas/clas72 /usr/local/COSMIC/DATA.

2 ADC Configuration

The operation of the LeCroy 1881M ADC is detailed in the LeCroy manual. The general characteristics of the ADC are the following:

- Programmable 12-bit or 13-bit operation .
- 50 fC least count.
- 400 pC full scale above pedestal for 13-bit, and 200pC full scale 12-bit operation.
- 12 μs conversion time.
- Multiblock readout.
- Sparsification – data below individually preset programmable thresholds are not readout.

For our purpose, we have configured the ADC boards (as programming options or jumpers on the board) for the following:

- Floating ground.
- The ADC gate (250 ns wide), Fast Clear and Conversion-in-Progress are provided to the ADC via the FASTBUS backplane. This option must be implemented consistently in software and hardware.

3 Results

The software system previously described was used to check the dynamic range, noise, and linearity of the ADCs. The following features were verified in preparation for these tests:

- The Conversion-in-Progress signal from the FASTBUS backplane was measured on the scope to be 16.4 μs.
- David Abbott checked the Multiblock operation. The module tested had a similar problem to that found and corrected in the LeCroy 1877 pipeline TDC boards. The fix requires reprogramming an EPROM. LeCroy is currently working on this problem.
- Front-panel operation of the ADCs is functional.
- Sparcification is functional.

We now present the First-article test results for ADC boards B35021(serial number) and B35044.

3.1 Noise

The noise measurement is defined as the root-mean-square (RMS) spread of the pedestal when no input is plugged in, as stated in CEBAF specification. A typical spectrum is shown as in Fig. 1. The noise level is around 50 fC (1 ADC count).

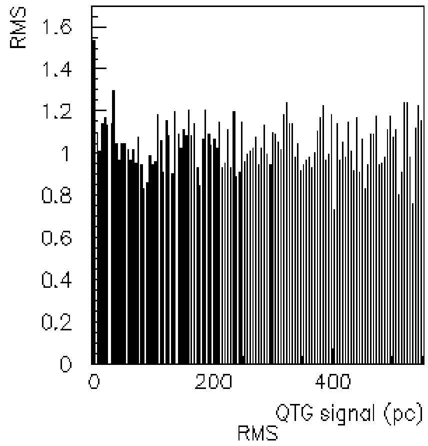


Figure 1: Noise spectrum for 13-bit operation, RMS versus QTG values is plotted.

3.2 Grounding

The ADC specification does not specify the RMS spread of measured values with input cable connected, as this is largely determined by a global grounding scheme for the FASTBUS crate and input cabling. However, this spread is of great interest since any use of the ADC requires external connections to be made. We have therefore made measurements of the spread of ADC values for constant input charge under various conditions. These may be used to help determine the overall grounding scheme for the detector.

Fig. 2 is a schematic diagram of the overall grounding scheme used for studies of the RMS spread under various conditions. Table 1 summarizes the measurements. These measurements were taken earlier this spring with a 1881 ADC, so represent a slightly different setup than that used for all other tests. Two general observations can be made from these data a) floating ground scheme resulted in smaller RMS and b) connection of crates (e.g. CAMAC and FASTBUS) with different grounds via cables increased RMS. A preliminary conclusion is that to reduce "noise" in the ADCs, the racks in the experimental Hall should have a solid connection to a common ground.

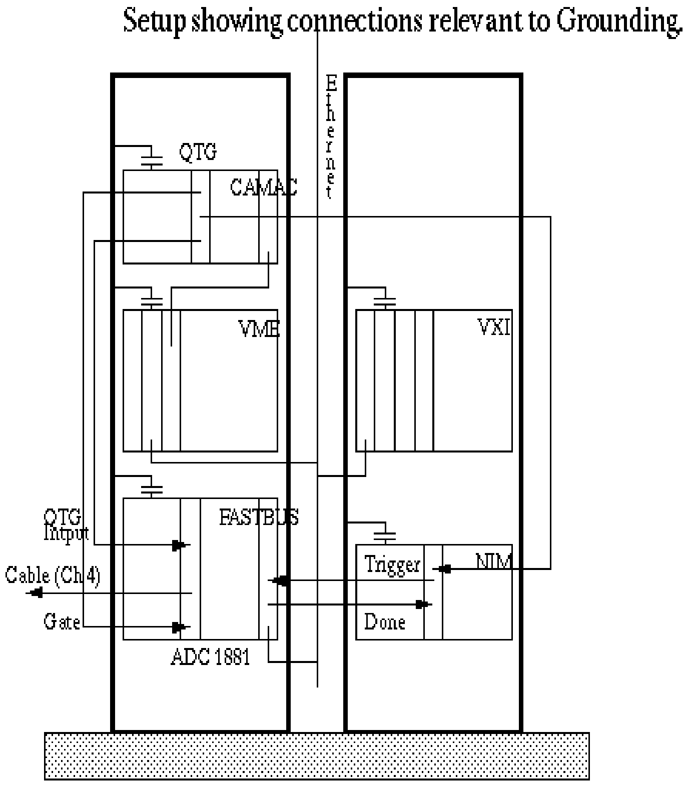


Figure 2: We show connections between crates for the measurements of noise. The crates were screwed to the racks but electrical connections were not necessarily very good. In order to connect various grounds to the ADC, we connected channel number 4 of the ADC to various modules in the other crates which were not expected to produce signals.

Table 1: RMS spread of ADC values under various grounding conditions. The RMS was measured over the entire 12-bit dynamic range (100 fC least count) of the 1881 ADC and was roughly constant. The quoted value shows a visual average over this range. Quoted errors reflect reproducibility of measurements. In all cases, the fitted deviations from the measured average were approximately one count or less.

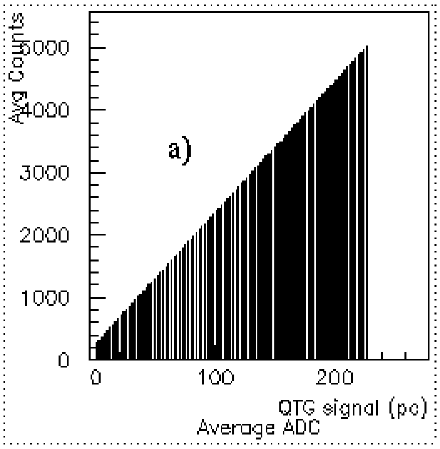
Ground Scheme of 1881 ADC	Cable (Ch 4) Connection	QTG signal RMS (counts)	Cable (Ch 4) RMS (counts)
Fixed	FASTBUS	4.5±0.5	1.5 ±0.5
Fixed	none	4.5±0.5	0.6 ±0.1
Fixed	CAMAC	4.5±0.5	6.0 ±1.0
Floating	FASTBUS	1.8±0.3	1.5 ±0.5
Floating	none	1.8±0.3	0.6 ±0.1
Floating	CAMAC	1.8±0.3	1.8 ±1.0

3.3 Dynamic Range and resolution

Since the availible linear fan-out module is rather noisy, only one ADC channel can be connected to QTG at a time. The results shown subsequently are from the channel 2 (counted from 0 to 63), board B35021.

The QTG has a full range of 600 pC for 16-bit resolution, the least-count being 9.154 fC. To test the dynamic range for both 12-bit and 13-bit operation, we have programmed the QTG to send pulse from 0 to 300 pC, and from 0 to 500 pC , respectively. Fig. 3 shows the average ADC counts versus QTG sent for both 12-bit and 13-bit cases. The dynamic range is greater than 200 pC and 400 pC for 12-bit and 13-bit, respectively.

Note that the 1881M ADC uses the lower 14-bit to write out the data. Upon overflow, '3FFF' is written for both the 12-bit and 13-bit cases,to the lower 16-bits of the 32-bit ADC word transferred. Thus, the overflow condition is signaled when the 16 lower bits equal to '3FFF.'



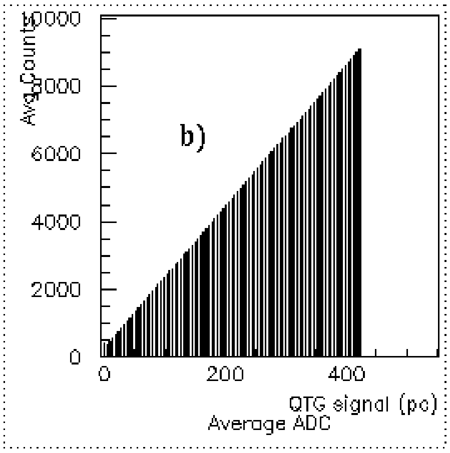


Figure 3: Dynamic range for 12-bit and 13-bit operation for a) 12-bit case and b) 13-bit case.

3.4 Integral Linearity and Least Count

The ADC measures the integrated charge of an electronic pulse. Typically, a capacitor charges up when the gate is open. The integrated charge is then stored, digitized and recorded as the "ADC" count. Generally, the relation between charge and the ADC count is linear. The least count can be determined from the slope of this linear fit, which has been performed on the data and shown in Fig. 3 . The least count obtained by linear fit is 47.9 fC for both 12-bit and 13-bit cases, respectively.

The integral linearity is defined as the maximum deviation from a straight line of the measured versus actual charge for a given ADC input. To determine the linearity properties of the ADC, we implicitly assume the charge generator (QTG), with is with its 16-bit resolution, is linear. The deviation from a fit of the measured ADC compared to the QTG programmed charge then determines the linearity of the ADC. We plot the deviation from both the linear and quadratic fits in Fig. 4. The maximum deviation is less than 8 counts, or 400 fC. A typical deviation is less than two counts, or 100 fC. We note that for our purposes the assumption of linearity is adequate, the fitted quadratic term is -0.62×10^{-4}.

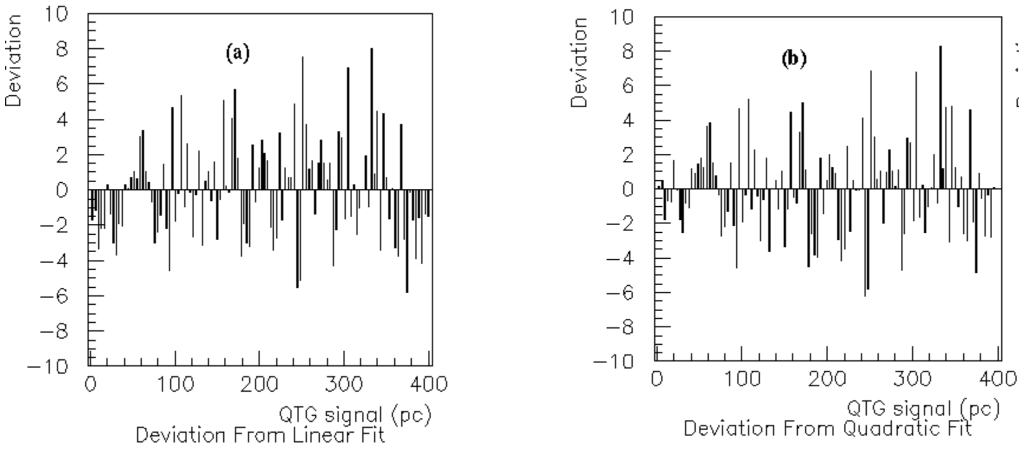


Figure 4: Integral non-linearity for 13-bit case, here we plot a) the deviation from a linear fit and b) the deviation for a quadratic fit. (*cf* Fig. 3)

3.5 Differential Linearity

The standard procedure for testing differential non-linearity consists of inputing a white (uniform and random) spectrum of pulse heights over the range of interest. Significant deviations above that expected from statistics, in the number of entries between ADC bins indicate non-linearities in the system. We have substituted a random distribution of signals with a uniform distribution with a granularity small compared to an ADC count. By programming the QTG to its maximum resolution (16-bits), and histogramming number of events versus ADC counts, channel-to-channel fluctutation are a measure of ADC differential non-linearity. A run for the range of 150 ADC counts takes more than 2 hours to achieve 3% statistics. Fig. 4 shows spectrum of number of events versus ADC counts, where the dashed and dotted lines are the $\pm15\%$ limit set by CEBAF specification, the solid line is the average counts. In earlier tests of an 1881 ADC, the entire dynamic range of the ADC was tested and found to be consistent with measurements of smaller ranges checked here for the 1881M ADCs.

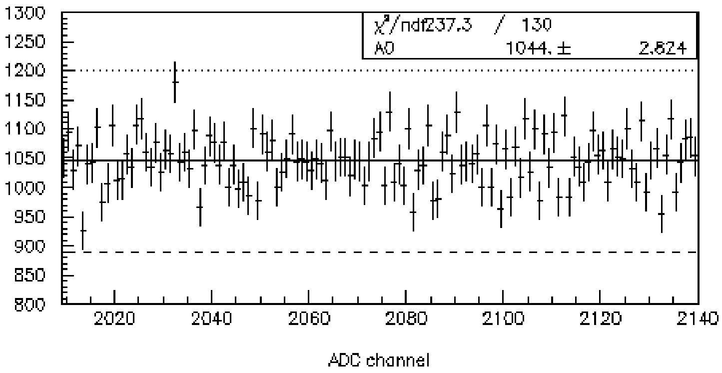


Figure 5: Differential non-linearity spectrum, ADC counts are histogrammed here. The horizontal solid line is the average; the dashed and dotted lines represent ±15% of the average.

4 Summary and Conclusion

The test results and the comparison with the CEBAF specification is given in Table 2. In all cases, the ADC exceeds our specification. Therefore, the LeCroy 1881M ADC was accepted under the CEBAF First-article Test Clause.

Table 2: **Comparison of test results with CEBAF specifications.**

	CEBAF Specs	Test Results
Integral Linearity	500 fC	400 fC
Differential Linearity	$\pm 15\%$	$\pm 10\%$
Noise	$\leq$ 200 fC	$\leq$ 70 fC
Dynamic Range	$\geq$ 200 pC	$\geq$ 400 pC
Sparsification	required	functional
Sensitivity	11-bit	13-bit
Conversion Time	30 μs	16.4 μs

References

[1] "Conceptual Design Report — Basic Experimental Equipment," CEBAF April 13, 1990.

[2] "Charge Sensitive Analog-to-digital Converters for the CLAS," CEBAF Specification 66550-S-01099.

[3] "CEBAF On-line Data Acquisition User's Manual," Version 1.2, March 12, 1993.

[4] "Calibration CLAS FASTBUS TDCs," Robert Millner and Elton Smith, CLAS-NOTE-093-017, Sept. 27, 1993.

[5] Preliminary note on "Description and Instructions for a FASTBUS Signal Distribution Module," Chris Cuevas, April, 1994.

[6] LeCroy Corporation, "1994 Research Instrumentation Catalog," 700 Chesnut Ridge Road, Chestnut Ridge, NY 10977.

[7] Phillips Scientific, 305 Island Road, Mahwah, NJ 07430.