AUTOMATED TESTS FOR THE PREAMPLIFIERS OF THE CLAS DRIFT CHAMBERS

CLAS Note # 96-013

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Abstract

The automated test set-up and the test procedure to evaluate the preamplifiers of the CLAS drift chamber are presented in this paper.

Introduction

To reconstruct charged particle trajectories in the CEBAF Large Acceptance Spectrometer (CLAS), eighteen multiwire drift chambers will be used. The chambers are located in three regions which are defined by the toroidal magnet. Region 1 is positioned around the target. Region 2 is located in the gap between the cryostats. Region 3 is situated beyond the outer radius of the cryostats. Along the azimuthal direction each of the regions is subdivided into six sectors, each of which is sixty degrees apart as defined by the cryostat. [1]

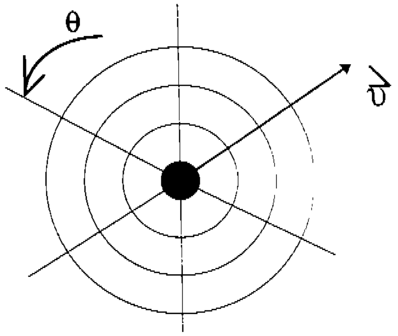


Figure 1. This is a two-dimensional representation of CLAS. The dark center is the target area. The circles surrounding the target area represent the regions. The lines extending through the regions show the six sectors.

Each drift chamber is instrumented with at least ten Signal Translator Boards (STBs). These boards cover an entire endplate. Each preamplifier located on the STB is connected to a sense wire. All the preamplifiers on the STBs need to be tested before installation. Hence, an automated test procedure has been developed to evaluate the condition of each preamplifier.

The test procedure uses LabView and a programmable multiplexer to direct test pulses in and out of each preamplifier. LabView compares expected values to actual values measured and determines whether the preamplifier is working properly. Preamplifier output signals are viewed on the PC and results of the comparison tests are documented to a spreadsheet.

Signal Translator Boards

Signal Translator Boards cover an entire side of the wire chamber endplate. A connection is made between the signal wire and STB using a conductive rubber "boot". A decoupling capacitor is located by the sense hole to stand-off all of the high dc-voltage from the preamplifier. Each sense trace terminates at a preamplifier. There are at least three blocks of preamplifiers on each board depending on which region the board is located. These blocks are labeled one through three on Region 3 STBs. Each preamplifier has its own identifying label. For Region 3 STBs, the first preamplifier located in block one is labeled C1C1. The last preamplifier in block one is labeled C1C16. These preamplifier blocks are referred to as SIPset A, B and C. Although the same procedure is used to test the Region 2 STBs, the primary focus of this paper will be on the testing of the Region 3 boards.

Preamplifiers

The preamplifiers are designed specifically for the CLAS drift chambers. The preamplifiers are in a single inline package (SIP) format. The SIPs have complementary outputs designed to amplify signals by a factor of 2.25mV/μA. Besides high gain, characteristics of the SIPs include: fast rise and fall times (3ns to 4ns), wide frequency bandwidth, wide dynamic range, low noise and low power dissipation (65mw). The power requirement for a single SIP is 5VDC at 0.03A. The schematic and a diagram of a SIP is given in the Appendix Sheet 1 [2].

Labview

Labview uses a graphics based programming language which interfaces with the test equipment via a General Purpose Interface Bus (GPIB) board or an I/O port. Programs in LabView are called Virtual Instruments (VI's).

There are two parts to a Labview VI: the front panel and the block diagram. The front panel is like an instrument panel with controls and indicators. Every object that appears on the front panel has a terminal that associates it to the block diagram. Instrument-input-devices are called controls and instrument-output-devices that display data acquired from the block diagram are called indicators, devices that supply data to the block

The block diagram consists of nodes, terminals and wires. Nodes are executable elements much like statements, operators, functions and subroutines found in conventional programming language. Wires carry data between nodes and terminals [3].

Multiplexer Groups and Relays

The Cytec PC-A/128-1 programmable multiplexer (MPX) is used in conjunction with LabView to test three sets of SIPs at a time. The multiplexer has four sets of sixteen relays (4-16x1). A relay in each set can be activated at any given time. The relay sets are numbered 0-3 and are partitioned into groups (0-7). Set 0 contains groups 0 and 1, set 1 contains group 2 and 3, set 2 contains group 4 and 5, and set 3 contains group 6 and 7. Each group has 8 relays numbered 0-7.

Each SIP-set consists of sixteen pairs of signal outputs and a pair of test pins. The multiplexer is set-up such that groups 0 and 1 address sip-set A, groups 2 and 3 address sip-set B, and groups 6 and 7 address sip-set C. The remaining groups 4 and 5 are reserved for the test pins on each SIP-set. Figure 2 shows the configuration of sets, groups and relays for the Region 3 STBs*.

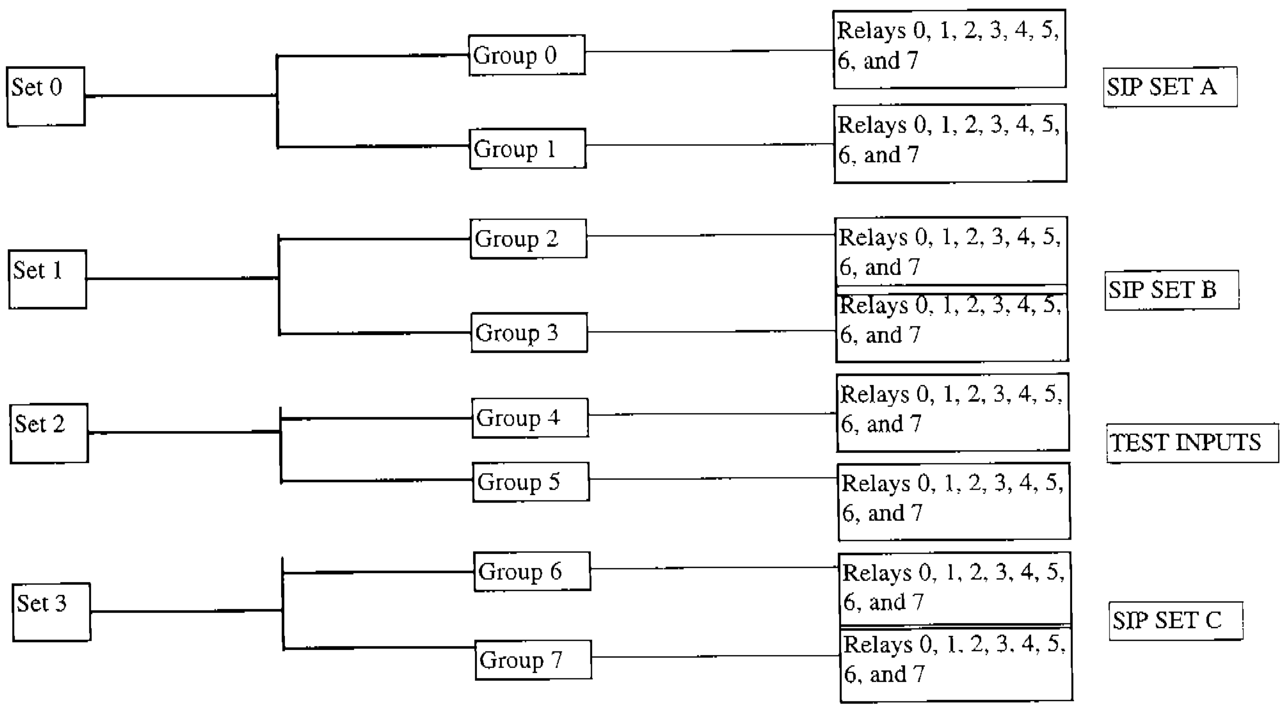


Figure 2. Multiplexer set , group, and relay connections.

*The multiplexer configuration for the Region 2 STBs is 2x16x1. This allows for two SIP sets to be tested at a time on a board that contains 12 SIP sets.

Experimental Set-up

Hardware, communications and software design of the experimental set-up is as follows:. The hardware is matched according to the test requirements, and the hardware is compatible with LabView. Communications links LabView with the hardware. Software design incorporates many LabView sub VIs into one program in order to execute the test procedure.

Hardware

The hardware consists of :Two Tektronix TDS 644A (four channel oscilloscopes) are used to study the preamplifiers output waveforms. These scopes are chosen because the analog bandwidth for each model is greater than 500MHz, which is large enough to accommodate the test requirements of 353MHz. The scopes have sample rates of 2 Gigasamples/sec. Each scope has four acquisition channels and waveform math channels. Both scopes are GPIB and LabView compatible and has a hard drive and a floppy disk drive which allows for saving and recalling test set-ups and waveforms. A Cytec PC-A/128-1 128 Channel Programmable Multiplexer with a LabView driver module is used to select SIPs to test. A Wavetek 20MHz Function Generator was chosen for its capability of generating pulses with rise times of about 3.75ns. It also features good amplitude, frequency, pulse width and delay ranges. A Hewlett Packard 6651A Power Supply is used to power the SIPs on the STBs.

Multiplexer Connections

A function generator is connected to the multiplexer port JC. The function generator inputs a test pulse at MPX port JC which is directed via the multiplexer to the port JB. At JB, the test pulse is sent to the STB preamplifiers. The amplified pulse is returned to the multiplexer as a input on Ports JA or JB and is multiplexed to the output JC. Three oscilloscope channels are connected to JC.

Figure 3 shows the inputs and outputs between the STB, the multiplexer, the function generator and the oscilloscope. Appendix sheets 3 and 4 list connector pinouts of JA, JB and JC.

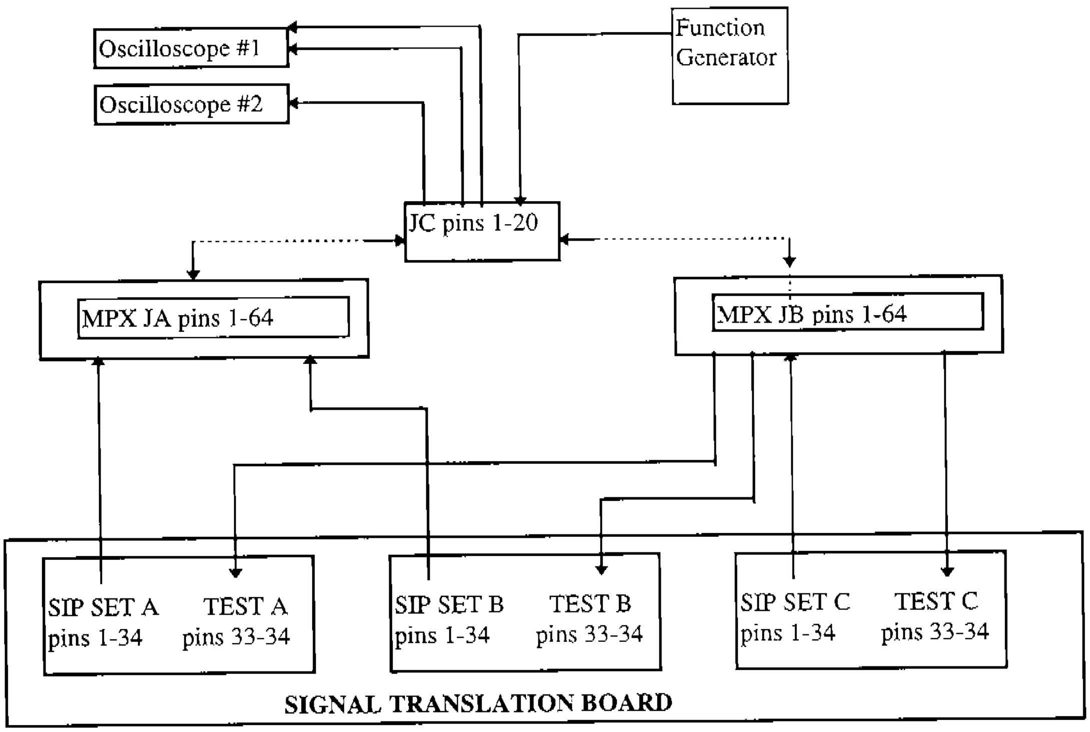


Figure 3. MPX, STB, function generator and scope connection diagram. Dashed lines represent MPX internal connections.

Cabling
Three laminated 17 pair cables about 5 feet long connect the multiplexer to the STB. They are labeled A, B and C. At the STB end, three 34 pin crimp type ribbon cable connectors are used to attach the cables to the output connectors. At the multiplexer end, two 64 pin crimp type ribbon cable connectors are used to attach the cables to the JA and JB ports. Two of the three cables (A and B) from the STB were laminated together and connected to MPX port JA. The third cable C from the STB and the three test pairs from each STB port are connected to MPX port JB.

MPX port JC is connected to three channels of the oscilloscope and to one channel of the signal generator.

Communications
For Labview to control the test equipment via the GPIB, the instrument must be programmable and compatible with Labview. A list of such equipment is included with the Labview package and test set-up instruments were selected from this list. GPIB addresses established for the program are Tektronix Oscilloscope Model 644A [1] and Tektronix Oscilloscope Model 684A [2]. The multiplexer communicates with LabView over a PC-I/O Interface module and has a decimal I/O address of 896.

Programming VIs

The flow chart for this program is located in Appendix A, sheet 5.

SIPTEST.VI consists of three nested "For loops": The Chassis For loop, the Group For loop and the Relay For loop. The Chassis For loop controls which multiplexer will be addressed. Since only one multiplexer is used, the Chassis For loop executes only once. During execution, the start-group number is subtracted from the stop-group number to determine the number of times the Group For loop will execute. It sends the start group number to the Cytec multiplexer sub VI, CYTEC SELECT.VI.

Inside the Group For loop ,the start relay-number is subtracted from the stop relay-number to determine the number of times the Relay For loop will execute. The Group For loop sends the start-relay number to the CYTECSELECT.VI. The test-input group and relay number are determined by a series of case structures match the case with the input and send the proper test-input group and relay numbers to CYTECSELECT.VI.

Inside the Relay For loop is the CYTECSELECT.VI which addresses the proper relays for the multiplexer to close throughout the course of the test.

A series of sequence structures are also located in the Relay For loop. The sequence structures execute each time a relay is addressed by CYTEC SELECT.VI. The first sequence structure (0) contains the sub VI, TEK TDS EXAMPLE.VI. This VI communicates with the oscilloscope. It sends the following commands: initialize the oscilloscope, recall setup from file VIEWSIP.SET and send math waveform data to Labview. Sequence structure 1 reinitializes the scope if the GPIB address changes and/or the test type (sense input or test input) changes. Sequence structure 2 pauses the program for 1.5 seconds so the scope can be reinitialized before the tests are executed. The next four sequence structures 3-6 contain comparison tests. Each comparison test has a predefined condition and an error tolerance determined by the user. The first and second tests analyze the high and the low points of the pulse. The third test analyses the width of the pulse. The fourth test examines the fall time (which is the rise time of a negative pulse). If a SIP fails any one of the tests, the program stops sequencing and loops repeatedly on the failed SIP. The oscilloscope continues to update the waveform and signal characteristics on the PC. This allows the user to find, test and correct the problem. The continue button allows the program to begin sequencing again. Sequence structures 7-8 calculate the amplitude by subtracting low voltage value from the high voltage value. The input current is calculated by dividing input voltage by the circuit impedance. Current gain is determined by dividing the amplitude by the input current. The value for the current gain is sent to the front panel and displayed as a gain history chart and histogram. Sequence structure 9 controls the data written to Excel. The spreadsheet number, test type, and SIP numbers will be determined by the user. The date/time, row number, high, low, pulse width, and fall time data is written to Excel automatically. Sequence structure 10 controls the continuing execution of the program depending on the test type. If the test input mode is in effect, the program continues and closes the next relay in sequence. If the sense input mode is in effect, the program pauses until a button labeled Continue Test is pushed.

Experimental Procedure

There are a total of 13,824 SIPs to be tested on the Region 3 boards and a total of 13,566 SIPs to be tested on the Region 2 boards. There are 288 Region 3 boards and 78 Region 2 boards. Each board is inspected for loose or missing components, debris, oil and sharp points. A multimeter is used to check the power trace and test input trace for shorts to ground before the boards are tested. Two types of tests are conducted. The test input mode and sense input mode. The first test performed is the test input mode which is fully automated. The test pulse is multiplexed to each SIP block over the seventeenth pair of wires in the cable. The output of each SIP is multiplexed to the scope where it is sampled by the LabView program. The sense test is manual. A probe placed in the sense hole sends the test signal from the function generator to the SIP. The output of each SIP is treated the same as the test input mode.

A 100mV square pulse which has a width of 100ns and a frequency of 1k Hz is used as the input signal for both tests. The SIPs differential outputs are converted into a single negative pulse by the oscilloscope at a sampling rate of 20 samples per second. The scope subtracts the positive differential pulse from the negative differential pulse and displays a "math waveform". The "math waveform" is what is sampled by LabView.

The tests are designed to measure output amplitude, rise time and pulse width and compare these measurements to predetermined values for acceptance.

If the measurements fall within the limits of acceptance, the test continues to the next SIP. If any one of the measurements are out of the limit range, the test will stop and inform the user of the problem.

The following are the SIP acceptance factors :

	Test input mode		**Sense input mode**	
high reference	0mV	+/- 3mV	0mV	+/- 3mV
low reference	57mV	+/- 6mV	290mV	+/- 30mV
horz. width	95ns	+/- 2.5ns	95ns	+/- 5ns
fall time	20ns	+/- 10ns	30ns	+/- 10ns

Channel 1- low half of the differential output
Channel 2- high half of the differential output
Math Channel = Channel 1 - Channel 2

The test results are written to Excel. The gain of each SIP is calculated automatically in Excel.

Gain Calculation

The gain is defined as: $GAIN = V_{out}/I_{in}$.

$I_{in} = V_{in}/R_{total}$ $R_{total} = R_{board} + R_{SIP} = 1k\Omega + 120\Omega = 1120\Omega$

I_{in} is 89.3μA when V_{in} is 100mV.

Data Analysis

Mean amplitude, mean gain and the standard deviations of the means are calculated using Sigma Plot. A histogram and scatter plot of all sense input test samples follows.

The average mean amplitude is 289mV with a standard deviation of 25mV. The minimum amplitude is 204mV and the maximum amplitude is 348mV. The standard error is .00164.

The output amplitude of each sample is much higher than expected due to impedance ringing caused by mismatching impedance's in the set-up and overshoot caused by the decoupling capacitor located at the sense hole on the STB.

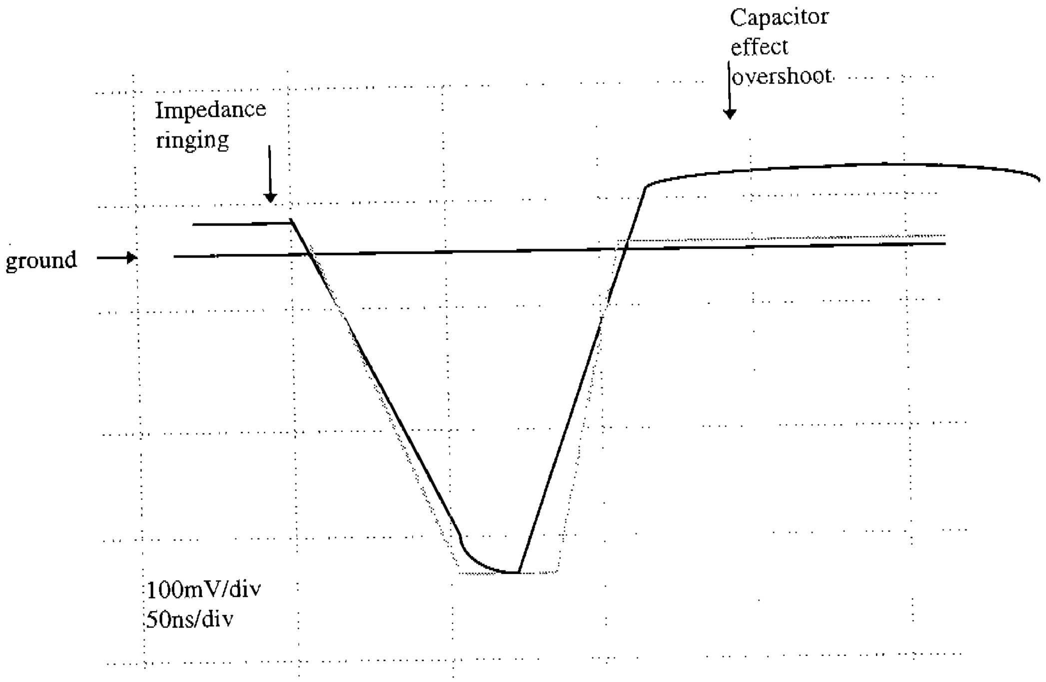
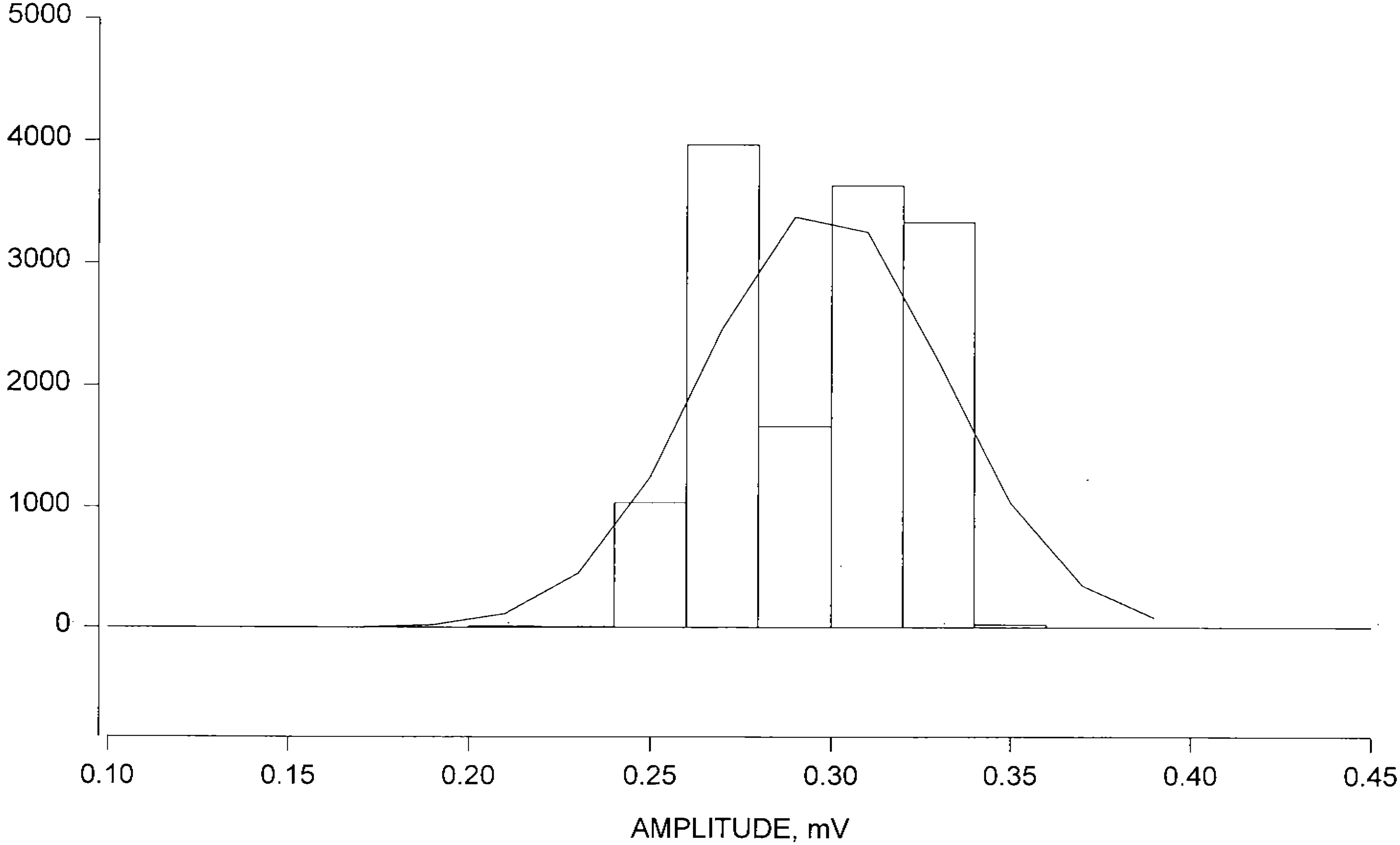


Figure 4. A typical output pulse of a SIP mounted on a STB (shown in black), for this test set-up, versus a typical output pulse of a SIP not mounted on a STB (shown in gray).

The scope samples the entire pulse including the ringing and overshoot. The correction for each measurement of amplitude is approximately +52.3mV. The correction for gain is approximately -0.46mV/µA. The data listed in the appendix does not reflect this correction.

The data analysis that follows is for all the samples taken. It should be noted, during the first week in May the multiplexer configuration was changed from 4x16x1 to 2x32x1 to accommodate the Region 2 STB testing. This new configuration changed the impedance of the multiplexer thus increasing the amplitude of the SIPs. A week by week account of the data has been included in Appendix C along with scatter-plots comparing the amplitude versus multiplexer configuration. Refer to Cambry Massey's paper *Analysis of STB SIP Test Data* for a detailed statistical analysis of this test.

SENSE TEST AMPLITUDE
ALL DATA



	DATE	MEAN AMP	ST DEV	MIN	MAX	# SAMPLES	ERROR
	24-Jan	0.2924	0.0256	0.24	0.33	528	0.00112
	2-Feb	0.2889	0.0304	0.22	0.33	336	0.00166
	5-Feb	0.2825	0.0306	0.204	0.33	384	0.00156
	6-Feb	0.2824	0.0287	0.206	0.33	432	0.00138
	7-Feb	0.2784	0.0261	0.24	0.33	529	0.00114
	8-Feb	0.2921	0.0306	0.24	0.33	478	0.00140
	9-Feb	0.2775	0.0282	0.206	0.326	48	0.00412
	11-Feb	0.287	0.0313	0.24	0.33	960	0.00112
	12-Feb	0.287	0.0313	0.24	0.33	960	0.00101
	13-Feb	0.284	0.0327	0.24	0.33	192	0.00236
	14-Feb	0.2804	0.0255	0.206	0.33	480	0.00116
	15-Feb	0.2879	0.0297	0.24	0.325	48	0.00429
	16-Feb	0.2924	0.0256	0.24	0.33	528	0.00112
	18-Feb	0.2945	0.0243	0.24	0.33	240	0.00157
	20-Feb	0.2851	0.0304	0.22	0.338	863	0.00103
	21-Feb	0.2906	0.0325	0.24	0.33	576	0.00136
	22-Feb	0.2903	0.0321	0.24	0.33	336	0.00175
	28-Feb	0.289	0.0299	0.24	0.33	576	0.00125
	1-Mar	0.2865	0.0288	0.24	0.328	144	0.00249
	4-Mar	0.2883	0.0281	0.24	0.348	364	0.00118
	8-Mar	0.27	0.0269	0.22	0.338	720	0.00100
	11-Mar	0.2879	0.0309	0.22	0.33	335	0.00169
	22-Mar	0.2697	0.0292	0.24	0.325	48	0.00422
	27-Mar	0.29	0.0298	0.24	0.336	384	0.00152
	29-Mar	0.2961	0.0305	0.24	0.34	671	0.00118
	1-Apr	0.2947	0.0313	0.24	0.34	243	0.00201
	3-Apr	0.2973	0.0313	0.24	0.34	288	0.00185
	7-May	0.2939	0.0185	0.26	0.31	608	0.00075
	8-May	0.292	0.0168	0.27	0.32	992	0.00063
	9-May	0.3031	0.000753	0.26	0.31	143	0.00053
	10-May	0.281	0.0168	0.24	0.31	96	0.00171
	15-May	0.2928	0.0143	0.22	0.322	384	0.00073
	16-May	0.2942	0.0119	0.26	0.31	128	0.00105
	21-May	0.2874	0.0151	0.24	0.31	141	0.00127
	22-May	0.2938	0.0139	0.26	0.31	141	0.00117
	28-May	0.3052	0.00939	0.296	0.32	6	0.00383
Average		0.289	0.025	0.238	0.327		0.00164
Total						14330	
Min		0.270	0.001	0.204	0.310		0.00053
Max		0.305	0.033	0.296	0.348		0.00429

Results

All 288 Region 3 STBs have been tested. Appendix B contains a printout of the Excel spreadsheet containing all the samples. A total of forty-one boards failed. Ten out of forty-one boards were defective. The defects include missing components, traces shorted to ground and missing heat sink masks. The remaining thirty-one boards had one or more defective SIPs. A total of thirty-five SIPs were replaced. The SIP failure rate was 0.0025%. The STB failure rate was 14%. All boards have been repaired and are ready to mount on the chamber.

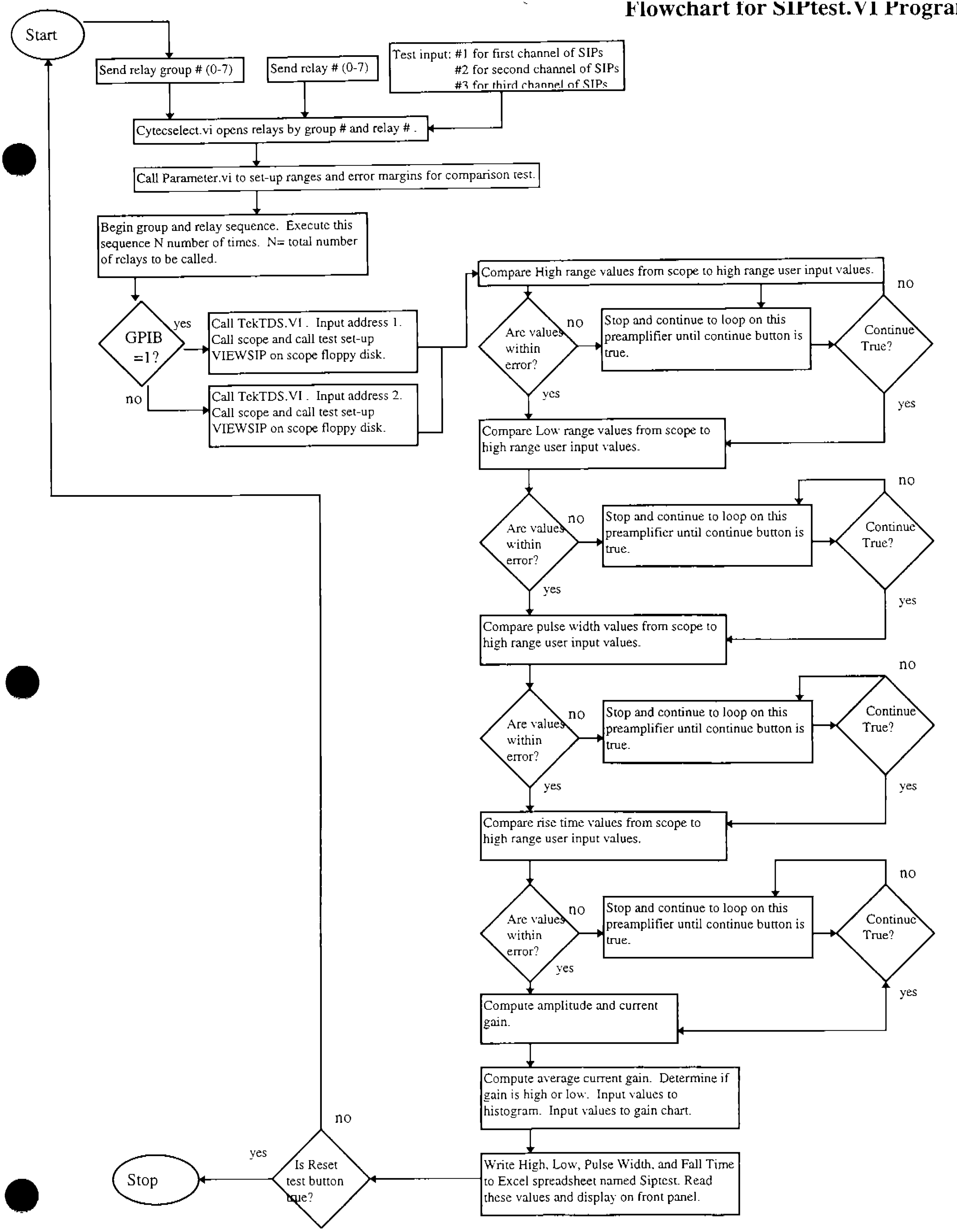
The Region 2 STBs are still being tested. A supplement to this paper containing the results will be added when the boards have been completely tested.

References

1. Conceptual Design Report Basic Experimental Equipment, CEBAF, 1990.
2. *A Preamp for the CLAS DWC,* Fernando Barbosa, CLAS-note 92-003.
3. LabView User Manual, D. Applegate, National Instruments Corporation, 1993.
4. *Bench Test Results of the Prototype STB for Region 3 Drift Chambers of CLAS, Cambry Massey, CLAS-note # 95-015.*

Appendix A

Flowchart for SIPtest.VI Program

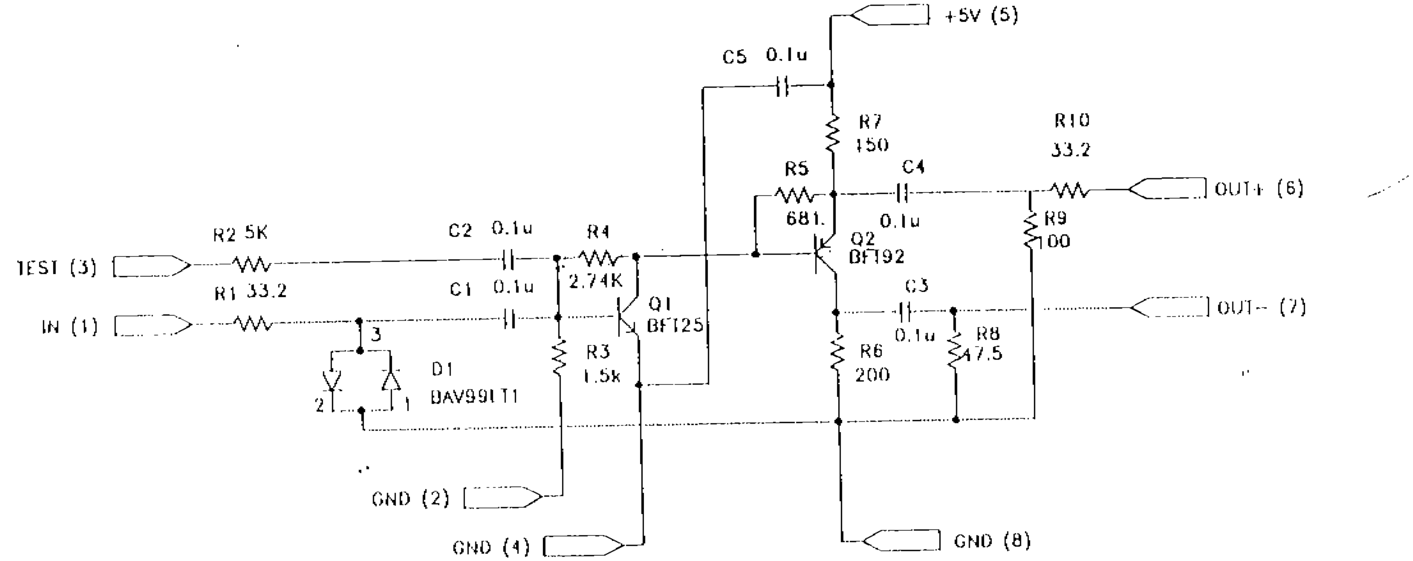


4x16x1 configuration				
Group	**Relays**	**Pin Hi**	**Pin low**	
0	0-15	1	2	
		3	4	
1	16-31	5	6	
		7	8	
2	32-47	9	10	
		11	12	
3	48-63	13	14	
		15	16	
Form C1 common		17		
Form C2 common			18	
Ground		19	20	
*Note Each group is commoned with two output pairs.				

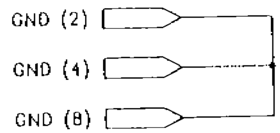
Multiplexer JA & JB Connections

STERO SIGNAL TRANSLATOR BOARD				AXIAL SIGNAL TRANSLATOR BOARD			
SIP #	**GROUP#**	**RELAY #**	**MPX PIN #**	**SIP #**	**GROUP#**	**RELAY #**	**MPX PIN #**
C1C9	0	0	JA 49,50	C1C8	0	0	JA 49,50
C1C10	0	1	JA 51,52	C1C7	0	1	JA 51,52
C1C11	0	,2	JA 53,54	C1C6	0	2	JA 53,54
C1C12	0	3	JA 55,56	C1C5	0	3	JA 55,56
C1C13	0	4	JA 57,58	C1C4	0	4	JA 57,58
C1C14	0	5	JA 59,60	C1C3	0	5	JA 59,60
C1C15	0	6	JA 61,62	C1C2	0	6	JA 61,62
C1C16	0	7	JA 63,64	C1C1	0	7	JA 63,64
C1C1	1	0	JA 33,34	C1C16	1	0	JA 33,34
C1C2	1	1	JA 35,36	C1C15	1	1	JA 35,36
C1C3	1	,2	JA 37,38	C1C14	1	2	JA 37,38
C1C4	1	3	JA 39,40	C1C13	1	3	JA 39,40
C1C5	1	4	JA 41,42	C1C12	1	4	JA 41,42
C1C6	1	5	JA 43,44	C1C11	1	5	JA 43,44
C1C7	1	6	JA 45,46	C1C10	1	6	JA 45,46
C1C8	1	7	JA 47,48	C1C9	1	7	JA 47,48
C2C9	2	0	JA 17,18	C2C8	2	0	JA 17,18
C2C10	2	1	JA 19,20	C2C7	2	1	JA 19,20
C2C11	2	,2	JA 21,22	C2C6	2	,2	JA 21,22
C2C12	2	3	JA 23,24	C2C5	2	3	JA 23,24
C2C13	2	4	JA 25,26	C2C4	2	4	JA 25,26
C2C14	2	5	JA 27,28	C2C3	2	5	JA 27,28
C2C15	2	6	JA 29,30	C2C2	2	6	JA 29,30
C2C16	2	7	JA 31,32	C2C1	2	7	JA 31,32
C2C1	3	0	JA 1,2	C2C16	3	0	JA 1,2
C2C2	3	1	JA 3,4	C2C15	3	1	JA 3,4
C2C3	3	,2	JA 5,6	C2C14	3	,2	JA 5,6
C2C4	3	3	JA 7,8	C2C13	3	3	JA 7,8
C2C5	3	4	JA 9,10	C2C12	3	4	JA 9,10
C2C6	3	5	JA 11,12	C2C11	3	5	JA 11,12
C2C7	3	6	JA 13,14	C2C10	3	6	JA 13,14
C2C8	3	7	JA 15,16	C2C9	3	7	JA 15,16
C3C9	6	0	JB 17,18	C3C8	6	0	JB 17,18
C3C10	6	1	JB 19,20	C3C7	6	1	JB 19,20
C3C11	6	,2	JB 21,22	C3C6	6	,2	JB 21,22
C3C12	6	3	JB 23,24	C3C5	6	3	JB 23,24
C3C13	6	4	JB 25,26	C3C4	6	4	JB 25,26
C3C14	6	5	JB 27,28	C3C3	6	5	JB 27,28
C3C15	6	6	JB 29,30	C3C2	6	6	JB 29,30
C3C16	6	7	JB 31,32	C3C1	6	7	JB 31,32
C3C1	7	0	JB 1,2	C3C16	7	0	JB 1,2
C3C2	7	1	JB 3,4	C3C15	7	1	JB 3,4
C3C3	7	,2	JB 5,6	C3C14	7	,2	JB 5,6
C3C4	7	3	JB 7,8	C3C13	7	3	JB 7,8
C3C5	7	4	JB 9,10	C3C12	7	4	JB 9,10
C3C6	7	5	JB 11,12	C3C11	7	5	JB 11,12
C3C7	7	6	JB 13,14	C3C10	7	6	JB 13,14
C3C8	7	7	JB 15,16	C3C9	7	7	JB 15,16

Schematic of Hybrid Preamplifier



NOTE: PINS 2, 4 & 8 connected through leads on BOT LAYER (Ground Plane)



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	BY:	Fernando J. Barbos
Revision: V1 Hybrid	24 MAY 1993	Page 1 of

Diagram of the Preamplifier