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Performance Testing of the Drift Chamber Pipeline TDCs

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1 Introduction

The testing of the Lecroy model 1877 time-to-digital converters (TDCs), to be used for the wire chamber read-out of the CEBAF Large Acceptance Spectrometer (CLAS), was carried out at Ohio University during 1994-5. The TDCs are 96-input fastbus-standard boards. Each input records the time of a logic voltage signal with a resolution of 0.5 ns, and a memory of 32 μs for up to 16 'edges' (voltage transitions). The CLAS detector requires about 220 of these boards.

One of the primary tests is to check that all 96 inputs are working on each board. Since each TDC input is connected to one or more of the wires in the drift chambers, an absent input is equivalent to a blind spot in the detector. Our bench-tests of the TDC's are now nearly complete, resulting in rejection of about 10% of the boards. Testing the functionality of the TDCs before installation in the CLAS detector has saved valuable time, as it would be more difficult to track down absent input signals once the detector is assembled. Considering the large investment of money and the years of effort constructing CLAS, the screening of the TDCs is justified, and a 10% failure of the TDCs at commissioning time has been averted.

2 Details of the Testing

It is not possible to exhaustively test every feature of every input over the whole time-range of the TDC, so a limited series of tests were performed using the CODA data acquisition system, running on a DECstation 5000/25 computer. A programmable pulser (Stanford

Research, model DG535) was connected to the DECstation by GPIB bus, and the outputs were fanned-out into the TDC inputs. The tests performed at Ohio University consisted of three main groups:

- **linearity:** the digital output should be linear in time.
- **uniformity:** a random-time input should be uniformly distributed.
- **functionality:** specialized design features must work properly.

The first two tests, known as integral linearity and differential non-linearity, were the primary tests. Problems with either of these aspects of the TDCs would affect the time-to-position calculations in the wire-chamber tracking routines, leading to a larger error in in the measurement of the particle's momentum, and possibly to false identification of the particle. In addition, a bad calibration of the time-to-position calculation would increase the χ^2 of the fit of the measured trajectory of the particle, resulting in a decreased signal-to-noise ratio, making it more difficult to extract the signals of interest in the CLAS experiments.

2.1 Integral Linearity

Testing for integral linearity took place in two stages. In one stage, the linearity was calibrated over the entire 32 μs range of the TDC. In the other, we examined the linearity more closely, over a range of just 4 μs, corresponding to the expected drift-time in the wire chambers. In either case, the procedure was basically the same. The pulser was programmed to send many pulses of a specified delay (100 ns for the full-range test, 20 ns for the 4 μs range test) relative to a start pulse. After accumulating enough statistics (> 200 counts) to get a peak centroid and width at a given delay setting, the delay was incremented by a specified amount (400 ns or 20 ns) and pulsed again. This process was repeated until the maximum range was reached. These data were fit to a straight line, and then compared with the expected slope of 0.5 ns per channel. A TDC would be rejected if the slope deviated even 1% from this value, or if the slopes were not consistent among the 96 inputs of the board. A total of 2 TDCs were rejected for this reason.

Plots of the results of the integral linearity tests are shown in Fig. 1a and 1b for the 32μs range, and Fig. 1c for the 4μs range. In the upper left corner is a plot of the TDC channel versus time, which shows the fit to a straight line with a slope of 0.5 ns per channel. Each point was determined by finding the mean value and RMS deviation of the peak. The peak width, represented by σ_{RMS}, is plotted for each point in the upper right corner. Typical values are near 0.5 channels, as expected based on the TDC design, but vary from board to board, as shown by comparing Figs. 1a and 1b, labeled by the board serial numbers. The RMS width, averaged over the time range, is perhaps the most useful measure of the TDC performance. Also shown is the deviation of each point from the straight-line fit in the lower left corner, and the deviation from a straight-line projection from the previous point, using a slope of 0.5 ns per channel. Both plots show a structure over the full 32μs range which is not purely statistical. This structure is presumably due to the interpolation of the TDC, rather than the pulser (which has better linearity specifications), and is similar for all TDC boards. Over the 4μs range, the deviation from previous value shows a smooth behavior which is not present in the deviation from fit plots, which indicates a changing trend in the time calibration (zero intercept) as a function of channel. Over the 4μs range, the spread in deviation from fit is nearly that expected from statistics. In all cases, the deviation from fit is bounded to within ± 0.3 channels, which is acceptable for use with CLAS.

The RMS width, as shown above, is nearly the same for all channels, although there is some variation across the time range. An average RMS width over all channels has been calculated for each input, then averaged over the 96 inputs for each board. The results are plotted in figures 2a and 2b, corresponding to the short (4 μs) or long (32 μs) time scales, respectively, for all boards that passed the tests. In general, a given TDC input will have a time resolution of 0.55 channels (from fig. 2), given enough statistics. The variation of the RMS widths, calculated using the standard deviation formula over all channels, has also been determined. The results have been averaged over the 96 inputs on each board, and are shown in figures 3a and 3b. In general, the time resolution is measured to be nearly the same for all channels, to within an error of 0.05 channels.

2.2 Differential Non-linearity

In order to test for differential non-linearity (DNL), two separate pulsers were used to generate a coincidence pulse of nearly random time delay, up to a maximum delay of 5.6 μs. A board with zero DNL would have a perfectly uniform response to a random time spectrum. The DNL of the 1877 TDC is specified at 20%, meaning that the spread in counts from channel to channel is not more than 20% of the average counts in all channels. The statistical variation with an average of 100 counts is 10%, so more than 100 counts per channel is needed over the useful range of the TDC in order to test the DNL. The 5.6μs corresponds to about 11200 channels, requiring over 10^6 events collected for each of the 96 inputs. Because the analog interpolator that determines the binning of the time input, and hence the DNL, is common to each set of 8 inputs (see Lecroy Application Note AN-50A), only 12 of the 96 inputs were connected to the random-time signal (we have verified that each set of 8 give the same response, at least in a few boards). This was the most time-consuming part of the testing, since it takes about 24 hours to read in 10^7 data words using our computer setup.

Not all of the channels have counts that are within 20% of the average. From statistical fluctuations, we expect about 2% of all 11000 channels to fall outside of this range. A typical spectrum of the DNL is shown in figure 4a and 4b, for two different boards. The measured DNL can vary quite a bit for different boards, and is another useful measure of the performance of the TDC. When more than 10% of the channels had counts deviating from the average count by more than 20%, the board was considered unacceptable and sent back to Lecroy for repair. This accounted for a total of 11 boards returned for repair.

The standard deviation, as determined using the average number of counts in figures like those of 4a and 4b, is shown in figure 5a. This histogram displays the accumulated values of the standard deviation for all boards. Figure 5b shows the variation of the standard deviation values among the different inputs on a given board. In general, an input to a given TDC board will have a DNL with a σ of 8% (see fig. 5a), i.e., a FWHM of 20% in the variation around the average counts. The FWHM is nearly the same for all 96 inputs, to within about 5% (see fig. 5b).

2.3 Functionality

The functionality tests examine the following aspects of TDC operation:

- Conversion time: how long for the TDC to digitize an event

- Fast clear: does the TDC reset in response to a 'clear' input
- Pulse width resolution: minimum time for 2 pulses to be resolved
- LIFO buffer: programmability of the last-in-first-out buffer

Each of these features are an important part of the TDC performance. For instance, if a given TDC is read out prematurely, because of an unexpectedly long conversion time, the data would be bad. This test is important because a problem here may become apparent only in actual data-taking, since it would still pass the linearity and DNL tests. Similarly, the fast clear test is equally important, because if this feature were to fail, the TDC would read out data from the previous event, resulting in useless data for some events. Like the problem with conversion time, failure of the fast clear can be misleading because the TDC would appear to be fine when examined on the test bench. We also look at the minimum pulse-pair resolution of the TDCs. The width of the pulse in the CLAS detector indicates which wires in the drift chamber fired, and two wires are combined in an exclusive OR into a given TDC input. If the TDC reads out two separate pulses as one larger pulse, not only will the wire be misidentified, but the information on the second wire is lost. An intermittent problem of this kind can be very hard to diagnose. Finally, the LIFO buffer, which determines how many past events are in the TDC memory, must be programmed properly in order to get the data properly ordered in the event stream with respect to data from other TDCs.

2.3.1 Conversion Time

The 1877 TDC requires some time between receipt of the common stop signal to when the digital read-out is ready. The minimum time for this to happen is 1.75 μs, even if only one input was 'hit'. If many inputs are hit, the digitization time follow the following formula,

$$t_c = 0.05 \cdot N + 1.25 \tag{1}$$

where t_c is the conversion time and N is the number of inputs hit. Since the minimum time is 1.75 μs, this formula is valid only for $N > 10$.

The conversion time can be monitored by the BIP (buffer-in-progress) signal on the backplane of the fastbus crate, which we hooked up to a logic analyzer (HP model 54620A).

First, the TDC was sent 16 hits, corresponding to $t_c = 2.05\ \mu$s, and the BIP was measured. Then another 16 hits were added (32 total), corresponding to $t_c = 2.85\ \mu$s, and the BIP was measured again. No boards were rejected on the basis of these limited tests.

2.3.2 Fast Clear

The fast clear can be sent to either the front input of the TDC board, or through the back-plane of the fastbus crate. We tested only the latter configuration. To be within specs, the time from the leading edge of the fast clear pulse to the end of the BIP pulse should be no more than 250 ns. At this time, the TDC should be ready to take new data. This allows the computer to reset the event trigger in a short period of time, as needed for the high rates expected in CLAS. The fast clear feature worked perfectly on all 'production' boards that we tested, although it failed on earlier versions of the TDC.

2.4 Pulse Width Resolution

In order to examine the minimum pulse-pair resolution on the TDCs, we sent two pulses into the same input for each event, then decreased the time between those pulses by 0.1 ns until the TDC resolved only one pulse. The time between those pulses was a measure of the TDC pulse-pair resolution. On average, the resolution was about 12 channels, or 6 ns, with little variation between different TDC boards. This can be compared to the minimum of 20 ns expected for CLAS events.

2.4.1 LIFO buffer

The LIFO buffer is programmable, so that we can specify how many edges of a given input are stored in memory by the TDC, up to the maximum of 16 edges. We did not exhaustively test this feature, due to limited time, but rather did just one configuration to check the LIFO programmability. The LIFO was programmed to remember just 12 edges, then sent a series of pulses with 16 edges to the TDC, and checked whether it recorded only the required 12 edges in the data buffer. The TDC can also be programmed to record only leading or falling edges, but this feature was not tested on all boards.

3 Tests Not Performed

There were several problems found in the pre-production (beta-testing) version of the 1877 TDC that were not tested on every board. For example, it was found at one time that the TDC produced random output for a known input about 1% of the time when 2 stop pulses came close together, so that the TDC was doing read-out of the first stop while still digitizing the information from the second stop pulse. This was known as 'read-out during conversion'. This problem was identified with a design flaw in the boards, and was fixed for the production TDCs. Because of the complexity of this test, and the assumption that the design was fixed and therefore would not reoccur, we did not test all boards sent to CEBAF for this flaw.

Another programmable feature is the digitization time window (DTW). The DTW, referred to in the Lecroy manual as 'time measurement full-scale', specifies how far into the past the TDC remembers the signal it has received. This feature was tested on both the pre-production TDCs and one of the first production TDCs, and worked properly. It was decided that this feature was inherent in the board design, and not crucial for the operation of the TDCs at CEBAF, so it was not tested on the production boards.

4 Conclusions

A listing of the reasons for failure of the TDCs we tested is given in table 1. A total of 27 boards failed the testing procedures, out of approximately 273 boards tested (220 for Hall B, 53 for Hall A). This accounts for approximately a 10% failure rate. Most of the failures came from the DNL tests, and some of these boards would possibly have been OK for real data from CLAS, since the DNL spreads the time measurement into a few channels, amounting to only 1 or 2 ns error in the drift time. However, there is no reason to accept marginal quality unless we are forced to do so.

In conclusion, the testing of the Lecroy 1877 TDC boards at Ohio University has been completed. The testing required about 24 hours per board, taking nearly one year to finish, plus several years before the production testing to set up the data acquisition hardware and software, to find bugs in the pre-production board designs and allow time to fix them, and to converge on an orderly testing procedure. These tests have saved time in the commissioning time of the CEBAF detectors by removing the TDC boards with the most critical faults. In addition, testing procedures have been worked out that will help us check the functionality of any 1877 TDC with an apparent failure during data-taking at CEBAF.

TABLE 1: Listing of the types of failures for the Lecroy 1877 TDC boards tested at Ohio U.

1877 TDC failures	How Many
Bad differential non-linearity	11
Bad integral linearity	2
LIFO non-functioning	2
Bad multi-block read-out	2
Random or excessive noise	2
Failed minimum pulse-resolution	1
Excessive cross-talk	1
Other*	6

*such as: no power LED, bent pins, system crashing, etc.

Figure 1:

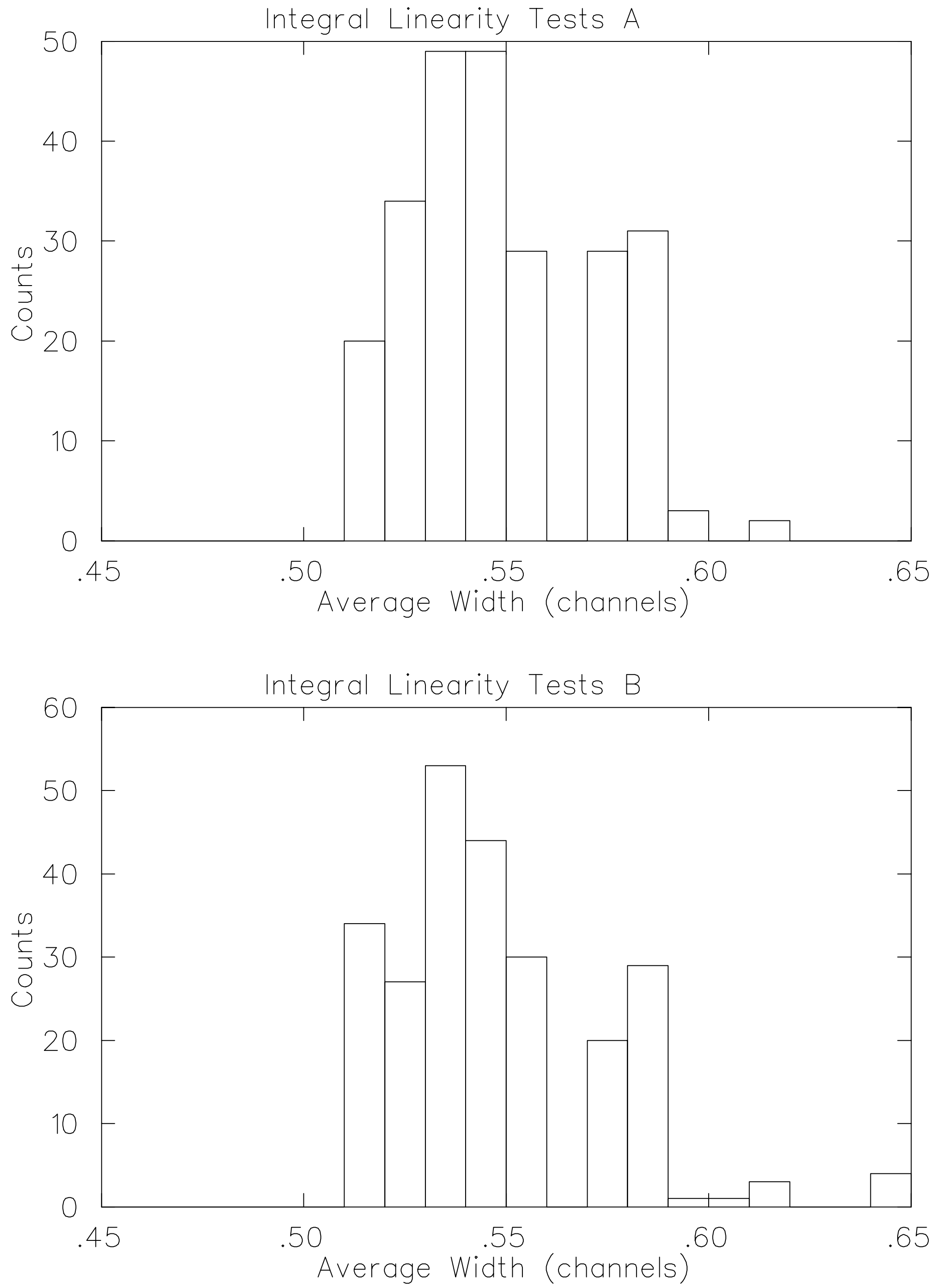

Figure 2: Integral linearity test, average.

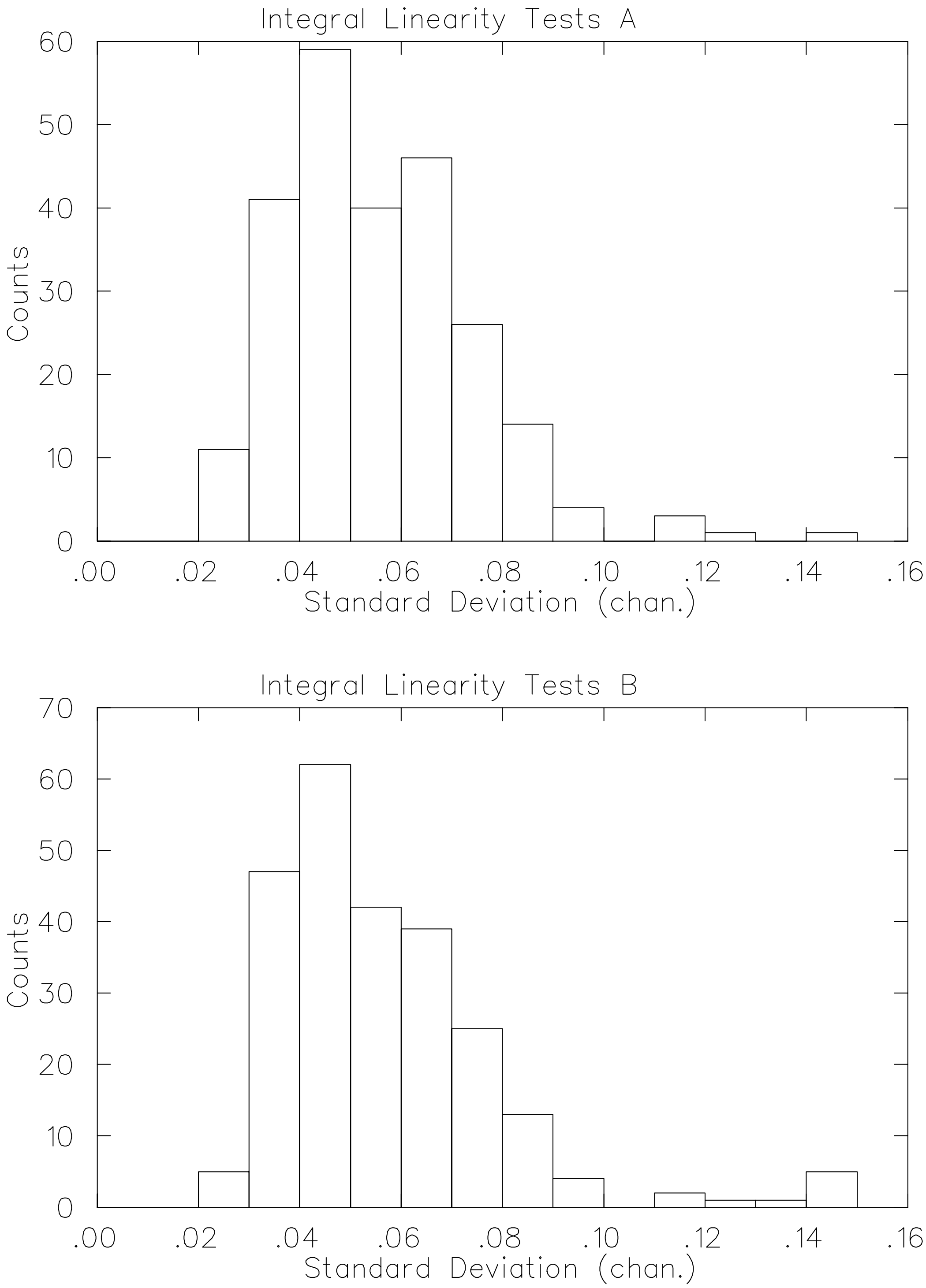

Figure 3: Integral linearity test, standard deviation.

Figure 4:

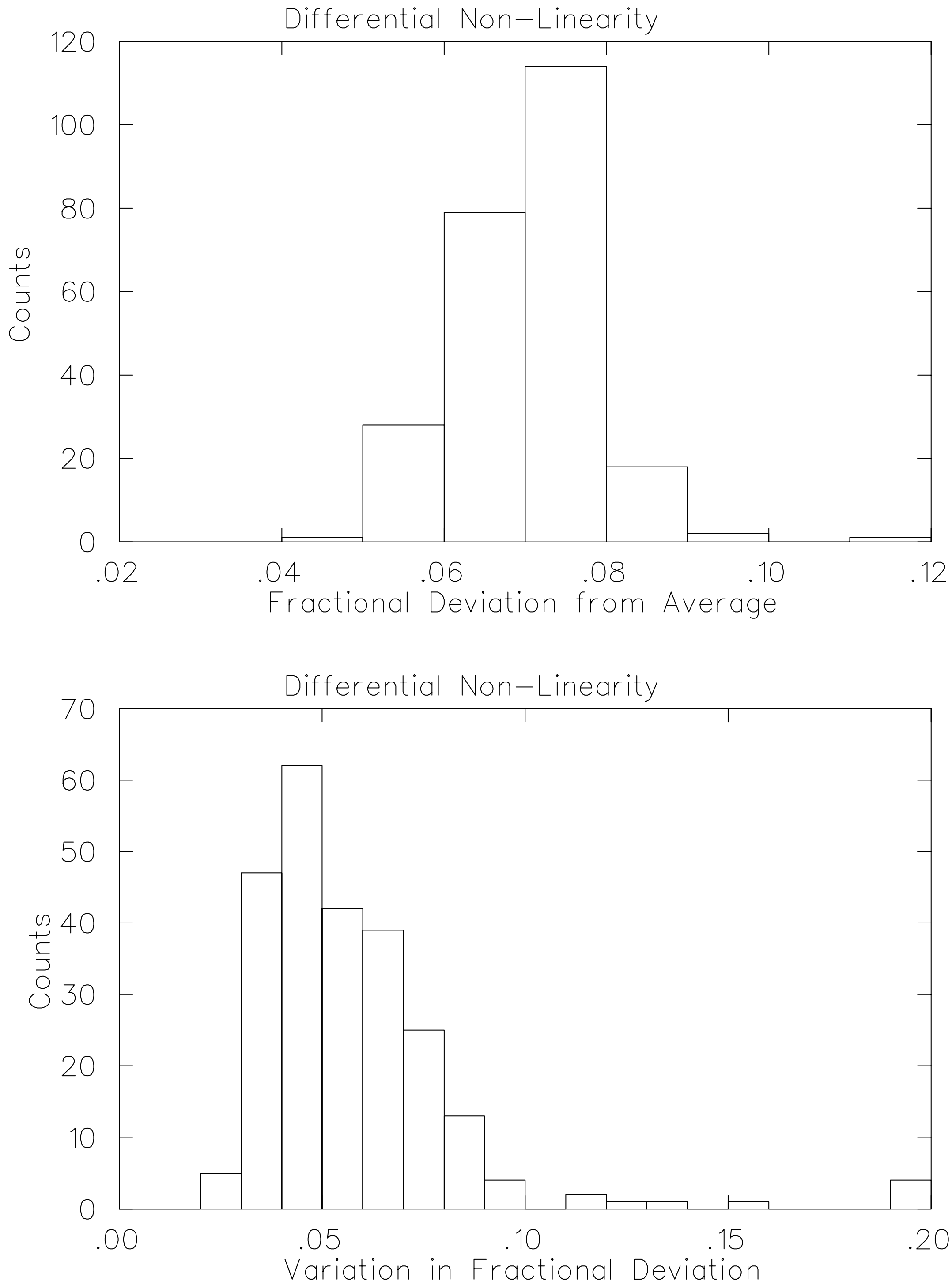

Figure 5: Differential non-linearity