CLAS_NOTE 98-009

Timing Problems

of the

CAEN V560E

Scaler Boards

Authors:
Michael Necaise – CNU, Steve Barrow – FSU, Christiana Martin – JLAB

June 4, 1998

Introduction

Over the entire commissioning period (September 1996 through November 1997), during data acquisition the scaler readouts of time-of-flight, electromagnetic calorimeter, and cherenkov detector systems were not livetime gated. As a result, the scalers (CAEN V560E 16 channel boards) continued to count even while the data acquisition system was busy processing a previous event.

Prior to the first data run in December of 1997, the veto logic of the scalers for all three of these detector systems was modified such that the busy signal, generated by the trigger supervisor board while it was processing an event, was fanned out to the veto input of each scaler module. The motivation for making this modification was to prevent the scalers from counting during the time intervals that the data acquisition system was unable to accept triggers. With such an arrangement, the scaler information for these three hardware systems is considered to be live time corrected.

It was clear by examining the scaler information for some preliminary runs, that the scalers were malfunctioning. Several boards did not function at all and were replaced. It was also noticed around this time that some scaler channels counted backwards! The number of counts read out in a particular channel exceeded the number of counts that were read out in a subsequent time interval for the same channel. (The scalers are read out once every ten seconds.) These problems appeared to be related to the introduction of the veto to the scaler counting logic.

To verify the operation of these boards, and discover any failure modes that might exist, a series of tests were devised. In all five boards were tested. Of these boards, one board had been previously tested and accepted as functional, two were new boards, and the remaining two were "suspect" boards which had been removed from Hall B. This paper presents the test procedures and their results.

Testing

A schematic of the hardware configuration used is shown in Figure 1. The test setup consisted of two pulse generators (A and B), an oscilloscope, NIM crate, VME crate, MVME162 crate controller, and a personal computer.

Initial tests were performed to verify correct operation of the scaler boards with no veto input; i.e., the pulse generator (B) for the veto input was disabled, and the veto input to the scaler card was terminated. Operation of each of the boards was checked by providing a chain of uniform 50 ns pulses to the scaler inputs. Bursts of high frequency pulses were also used. The rate of the input pulses was varied from 10 Hz to 1.0 MHz by orders of magnitude. During these initial tests, software control of the commands increment, veto, and clear, were also tested. One channel, channel #8 on board #5, did not pass all of the tests. It consistently over-counted the number of input pulses by ~ 0.15%, hence it was excluded from further studies.

In the tests that followed, scaler cards were examined to look for anomalous behavior in veto operations. The card being tested was provided with a veto input from pulse generator B (Figure 1). A second card with no veto input was used as a control. The CAEN specifications require a minimum lead time of 35 ns for the veto relative to the input pulse, and a minimum pulse width of 50 ns for the veto signal, as illustrated in

Figure 2. Scaler cards were tested with input rates varying from 10 Hz to 10 MHz and veto rates from 10 Hz to 1.0 kHz. The step size was in increments of orders of magnitude. The timing for the veto signal was varied in 5 ns increments beginning with the specification values. It was determined that for any veto pulse of width less than 50 ns, the veto failed. Additionally, it was found that if the veto signal did not lead the input pulse by at least 17 ns, the scaler veto failed; the lead time result is better than the specifications. These values were used in addition to the manufacturer specifications in future testing.

The scaler cards were then tested to find the relationship between counting errors and input rates. Pulse generators A and B were configured for free-run mode. Veto signals were not synchronously locked, although the pulse rates were fixed. Scaler boards which received the veto began to produce discrepancies between adjacent channels as shown in Figure 3. This was confirmed by comparison with the control, since the control scaler board verified that, when the veto was not applied, all channels counted the same number of pulses. Analysis of the results indicated that error rate depended on the veto rate. This was the first sign of consistent errors and these results confirmed the suspicion that the veto pulse was the cause of the observed malfunctions.

Since it was previously determined that the veto failed when the signal did not lead the input by more than 17 ns, the timing between the signals was re-investigated. It was confirmed, as shown in Figure 4, that for a lead time greater than 17ns, the veto worked correctly. When the lead time was less than 15ns, the veto consistently failed. Between these values, the scaler counters behaved erratically. There is a 2.5 ns window at the edge of veto failure where the veto-state is not well defined. Within this window it was observed that some scaler channels over counted, some significantly.

Since the manufacturer specifies that veto lines must be terminated with a 50 Ω load, the effect of not terminating the cable properly was also investigated. In all of the previous testing a terminator was used. It was found that removing the terminator shifted the veto's undefined region ~ 0.5 ns.

The final study was to determine the cause of the observed backward counting effect, in which the number of counts recorded in a particular scaler channel appeared to drop between consecutive readouts. A program was developed to monitor the scaler counters and search for instances of scalers counting backwards. This was accomplished by comparing subsequent read-out values. Backward counts were observed every 4-5 seconds at high rates (Figure 5). Further analysis determined that the error in counting was not a function of either the pulse rate or the veto rate (in fact, the errors still occurred with no veto signals present). Following a backward count, the subsequent value on the scaler counter corrected the previous error. Additional analysis showed that the backward counting was originating on the scaler card when a channel was concurrently incremented and read out.

Conclusion

It was observed that there appeared to be random errors in the counting. It was determined experimentally that there exists a window of approximately 2.5 ns, during which the veto state is not well defined in the hardware (Figure 4). If a veto signal falls within this 2.5 ns window, beginning 17 ns prior to the arrival of the input signal, the scalers have a tendency to over count. Since scaler veto signals generated by the hardware and software will generally happen at random intervals with respect to the input signals, it is difficult to set the timing of the veto pulse. A solution to this problem is to avoid use of the veto inputs to the CAEN V560E if at all possible. Where this is not realistic, it is better to apply the veto directly to the signal by inserting logic before the scaler input(s) (Figure 6).

In addition, the CAEN V560E scaler boards would occasionally appear to be counting backward. This problem was also observed during the testing, and is again due to an undefined region of operation for these CAEN scalers. The undefined region occurs as a channel is simultaneously read out and incremented. It was observed that upon the next VME bus read of the channel(s) in question, the affected channels returned to the correct count. This is an artifact of the scaler card being unable to present the correct data to the VME bus while that scaler is being incremented; it does not represent an error in the scaler count.

Figure 1:

General configuration:

Specific configurations depended upon the test being performed. The layout was designed to emulate typical configurations used in Hall B. In cases where veto was not required, only one pulse generator and scaler card would be used. Scaler operation and readout was performed via the VME backplane. The host computer (on the JLAB CUE cluster) provided the user interface.

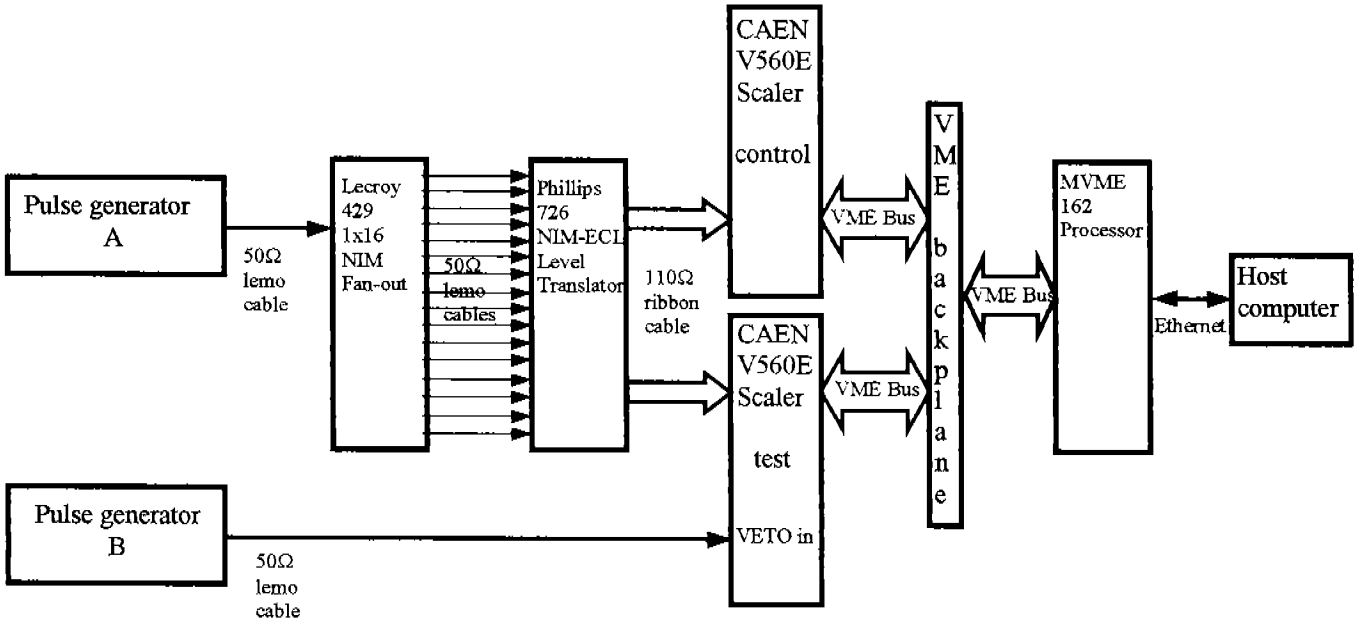
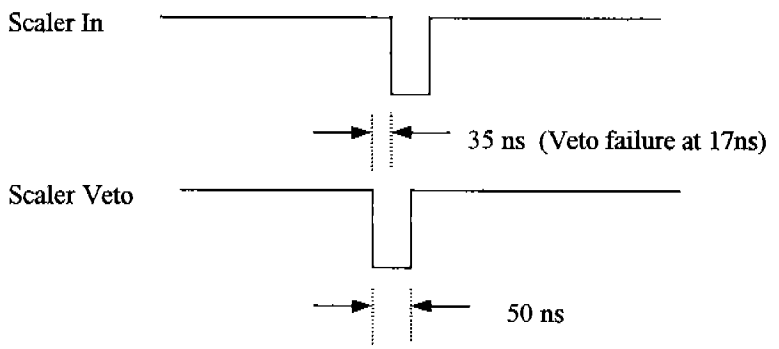


Figure 2:

Testing Basic Veto Operation:

Beginning with the manufacturer's specified signal parameters, operation of the scaler counter's veto was examined for various input rates and veto frequencies. In order to characterize the operation of the scaler veto, the pulse width and lead time were reduced incrementally until failure of the veto was observed.

Minimum Signal Timing per CAEN Specification



For minimum veto parameters, input rates tested:
10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, 10MHz

Using a 1 kHz input rate, the following veto signal parameters were tested:

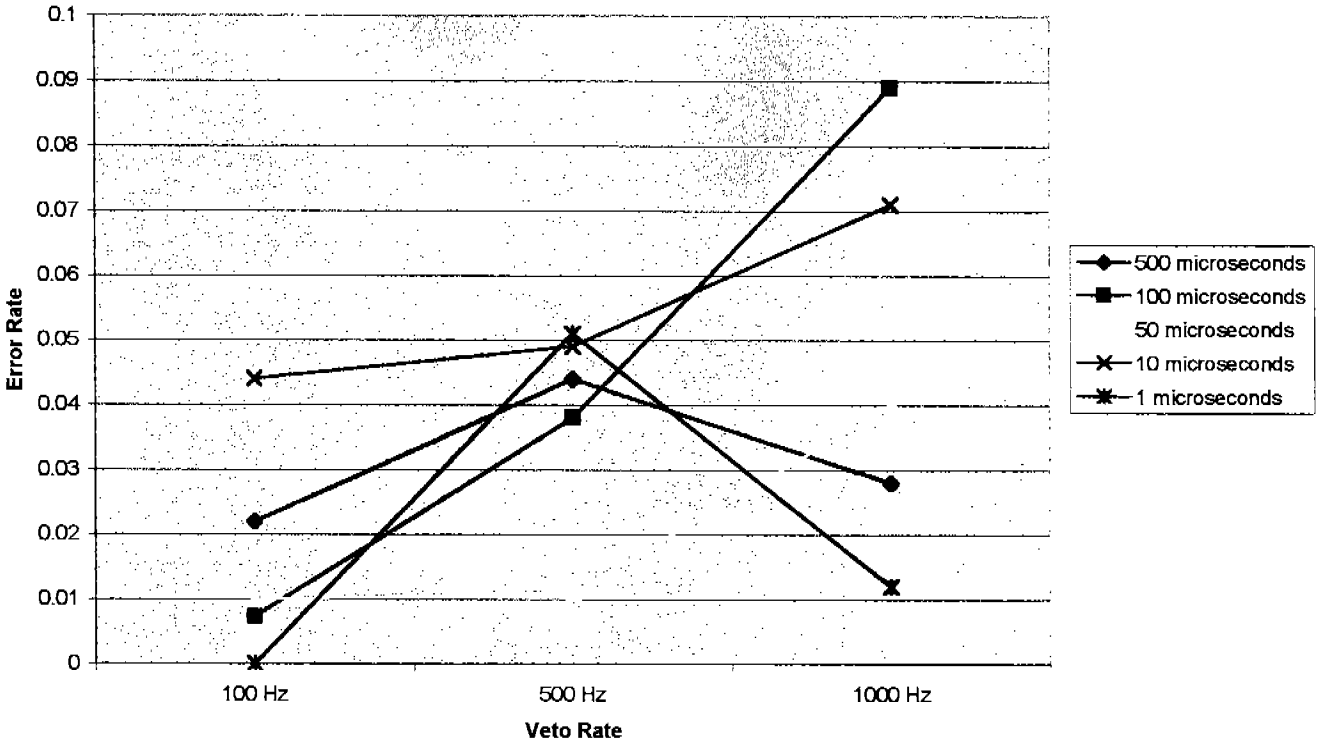
Lead Time	Pulse Width: 50 ns	45 ns	40 ns
67 ns	OK	fails	fails
62 ns	OK	fails	fails
57 ns	OK	fails	fails
52 ns	OK	fails	fails
47 ns	OK	fails	fails
42 ns	OK	fails	fails
37 ns	OK	fails	fails
32 ns	OK	fails	fails
27 ns	OK	fails	fails
22 ns	OK	fails	fails
17 ns	fails	fails	fails

Figure 3:

Analysis of Errors vs. Rates

The frequency of the veto signal was varied from 10 Hz to 1.0 kHz (10 Hz, 50 Hz, 100 Hz, 500 Hz, 1000 Hz) and the width of the veto signal was varied from 1 μs to 500 μs (1 μs, 5 μs, 10 μs, 50 μs, 100 μs, 500 μs). Testing was repeated for different input rates ranging from 1 kHz to 1.0 MHz.

Sample of data showing error rate as a function of veto rate and width. The error rate was determined by comparing the readout from 8 channels receiving veto signals with the control channels, and calculating the standard deviation from the control value. Scaler input rate is 50 kHz.

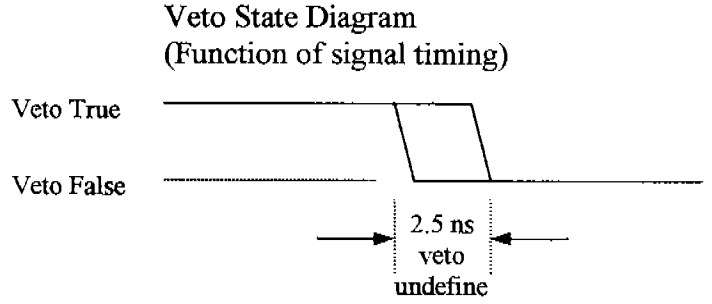


The overall trend appears to be a reduction in error rate along with a reduction in veto frequency. Exceptions occur for the 1 μs and 500 μs veto width at the 1000 Hz veto rate. It is believed that these exceptions are a coincidence of the input and veto signal which provided conditions appropriate for a low error rate at the high end, i.e. 1.0 kHz.

Figure 4:

Analysis of Veto Signal Timing

Timing of veto signal with respect to input signal was controlled. The veto lead time was reduced from the manufacturers specified minimum of 50 ns to <10 ns. The state of the CAEN scaler card hardware was determined to be as shown.



Within the undefined region, scaler read-out was erratic. In the following sample data, the board with base address F0030000 was receiving a veto signal in the undefined region. The board with base address F0040000 is the control. The scaler counter input was 8000 pulses at a rate of 500 Hz.

```
Reading scalers at base address f0030000
Scaler counter 1 contains:  8000
Scaler counter 2 contains:  18192
Scaler counter 3 contains:  0
Scaler counter 4 contains:  0
Scaler counter 5 contains:  12009
Scaler counter 6 contains:  30926
Scaler counter 7 contains:  0
Scaler counter 8 contains:  8000
Reading scalers at base address f0040000
Scaler counter 1 contains:  8000
Scaler counter 2 contains:  8000
Scaler counter 3 contains:  8000
Scaler counter 4 contains:  8000
Scaler counter 5 contains:  8000
Scaler counter 6 contains:  8000
Scaler counter 7 contains:  8000
Scaler counter 8 contains:  8000
```

Figure 5:

Backward Counting

For the purpose of the search, the following parameters were set:
Input rate: 50 kHz
Veto rate: 100 Hz
Veto width: 250 μs

Sample of data generated in searching for instances of scaler cards counting backward:

```
THU JAN 01 00:12:23 1970

Number of pulses generated:  783

scaler 0 previous value:  755    current value:  757

scaler 1 previous value:  755    current value:  757

scaler 2 previous value:  759    current value:  757
scaler 3 previous value:  756    current value:  757
scaler 4 previous value:  756    current value:  757
scaler 5 previous value:  756    current value:  758
scaler 6 previous value:  756    current value:  758
scaler 7 previous value:  756    current value:  758
THU JAN 01 00:12:28 1970
Number of pulses generated:  251770
scaler 0 previous value:  245563 current value:  245565
scaler 1 previous value:  245563 current value:  245565
scaler 2 previous value:  245563 current value:  245565
scaler 3 previous value:  245567 current value:  245565
scaler 4 previous value:  245564 current value:  245565
scaler 5 previous value:  245564 current value:  245565
scaler 6 previous value:  245564 current value:  245566
scaler 7 previous value:  245564 current value:  245566
```

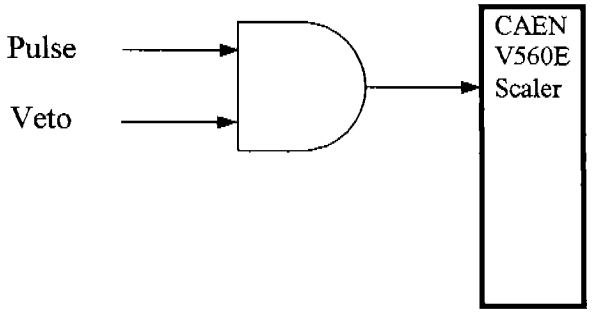
Notice that the backward count is highlighted.

Where the problem occurs, the previous value was larger than adjacent channels, and readout appears to be concurrent with an increment. Subsequent values were correct when compared to adjacent channels. All channels received the same input.

The rates were varied to study the effect on the error rate. The veto rate had little effect; errors still occurred with no veto signals present. Error rates varied with input pulse frequency.

Figure 6:

Veto external to the scaler



Using asynchronous external ECL logic, the pulse can be vetoed before reaching the CAEN scaler card. This can be used to avoid the CAEN scaler's veto problems.

Appendix

Specifications of the CAEN V560E VME scaler board:

Input Channels: Differential ECL level, 110 Ω impedance
Maximum Frequency: 100 MHz
Minimum Width: 5 ns
Minimum Interval: 5 ns

Veto Input: NIM level, high impedance
Minimum Width: 50 ns
Lead time required to veto input signal: 35 ns
VME bus addressable

Clear Input: NIM level, high impedance
Minimum Width: 60 ns
VME bus addressable

Test Input: NIM level, high impedance
NIM level, high impedance
Maximum Frequency: 50 MHz
Minimum Width: 10 ns
VME bus addressable

For further information, refer to CAEN V560E user manual.

Testing equipment used:

Lecroy 9210 Pulse Generator s/n A82854
Tektronix HFS 9030 Pulse Generator s/n B010109
Lecroy 429A NIM Logic Fanout s/n A41639
Phillips 726 NIM-ECL Level Translator
Motorola MVME 162 VME Controller s/n 1406650