NPS FADC and Trigger test plan

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For NPS collaboration

Hall C collaboration meeting
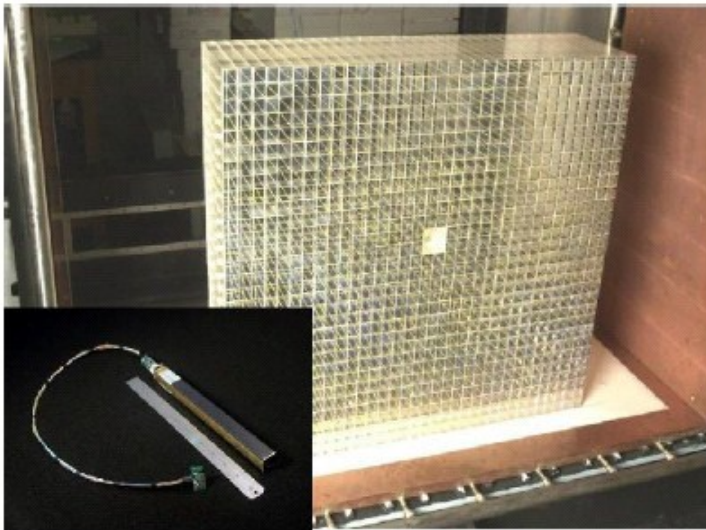February 21st 2014

Outline

- NPS calorimeter
- JLAB pipeline electronics
- Test plans
  - FADC test with PbF2
  - Calorimeter trigger test
  - Possible test beam
  - Full setup
- Possible developments
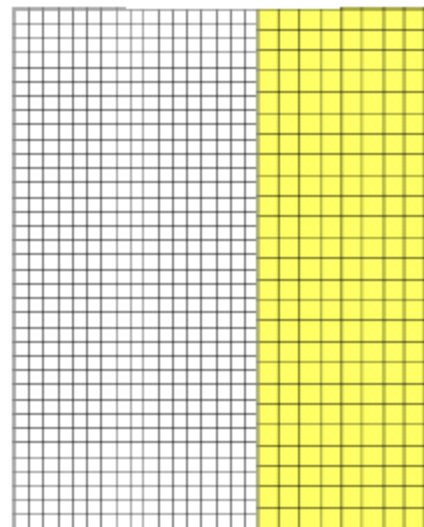- Conclusion

NPS calorimeter

- 31x36 array of calorimeter blocks
  - 208 PbF2
  - PbWO4
- Sweeping magnet
- Small angle
- High rate
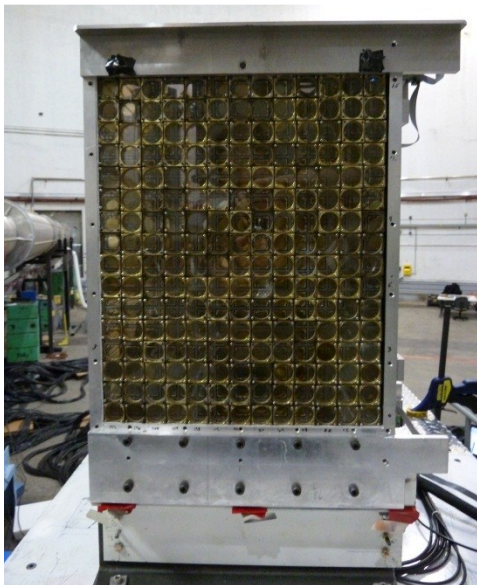- High radiation capability

NPS calorimeter configuration

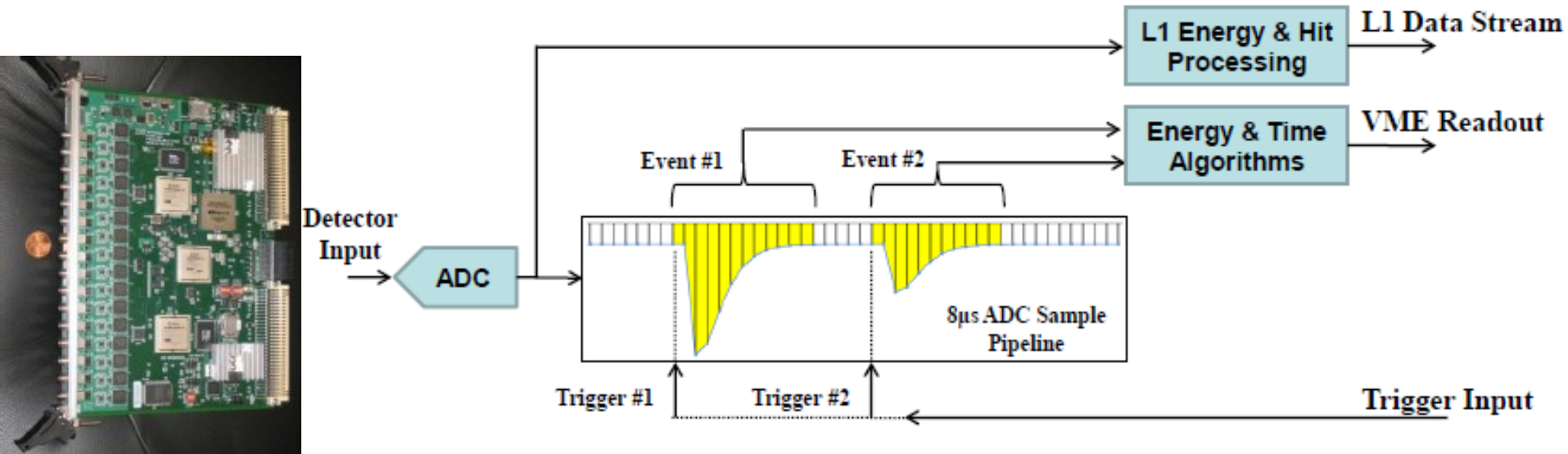Primex PbWO4

DVCS
PbF2

59×75 cm²

612 PbWO$_4$ + 200 PbF$_2$

JLAB FADC

Pipelined electronics 250 MHz sampling rate 12 bit
On board FPGA processing : pedestal subtraction, thresholds , integral and time
and summing of channels for triggering purpose

Can record complete waveform but large amount of data
Can record time and integral of pulse : improve rate but no information on pile up
Looking into dealing with pile-up at FADC level

Front-end Crates: Level 1 Trigger

• Each FADC250 stream L1 board energy sum/hit to Crate Trigger Processor (CTP) residing in VXS switch slot A

• Crate Trigger Processor computes a crate-level energy sum (or hit pattern)

• Computed crate-level value sent via 10Gbps fiber optics to Global Trigger Crate (32bits every 4ns)
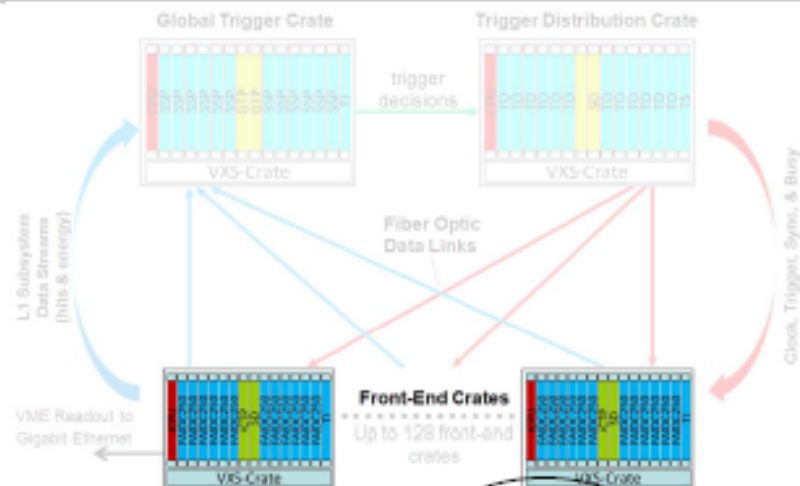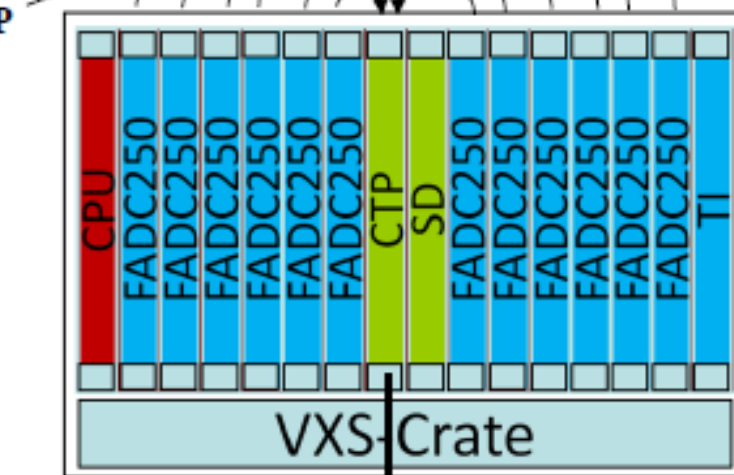
CTP Prototype:

Fiber Optics Transceiver

VXS Switch Connector

Board Energy/Hits 5Gbps to CTP

Crate Sum/Hits
10Gbps Fiber to Global Trigger Crate

Jefferson Lab

JSA

Small scale test

- Easy to setup
  - Test response of FADC with PbF2 pulse
  - Test performances transferring full waveform
  - Test data reduction on CPU

- On hand : 1 VME64X, 1 CPU,1 FADC, 1 TI
- Need : SD only

PbF2 and PbWO4

- PbF_2 is pure Cerenkov
- $PbWO_4$ has Cerenkov and Scintillator component
- $PbWO_4$ used in CLAS DVCS Calorimeter for DVCS and HPS but with APDs (signal wider)
- Want to test using PMTs to check FADC response with fast signals of PbF_2 and $PbWO_4$
- Sampling frequency might have an effect on PbF_2 readout since only few samples will be readout

PbF_2 pulse

$PbWO_4$

New J. Phys. **10** (2008) 025003
doi:10.1088/1367-2630/10/2/025003

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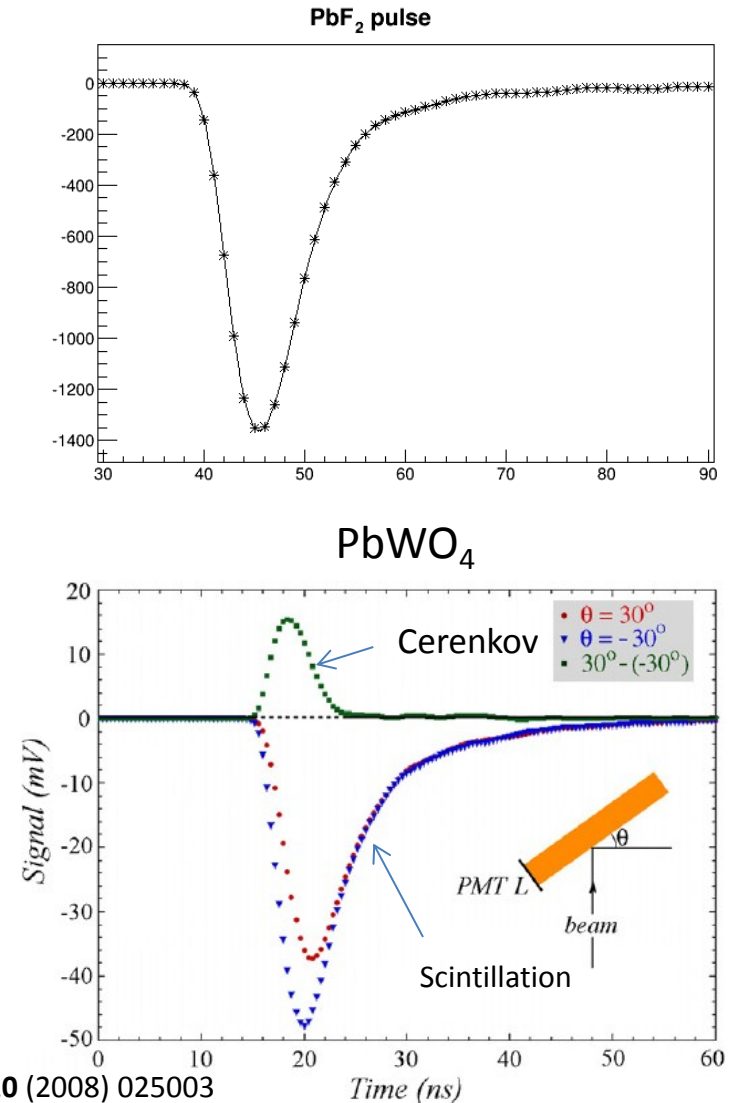
FADC test with detector

- Can test transfer speed
- Effect of the 250 MHz sampling on signal with about 10 ns FWHM using cosmics on DVCS calorimeter
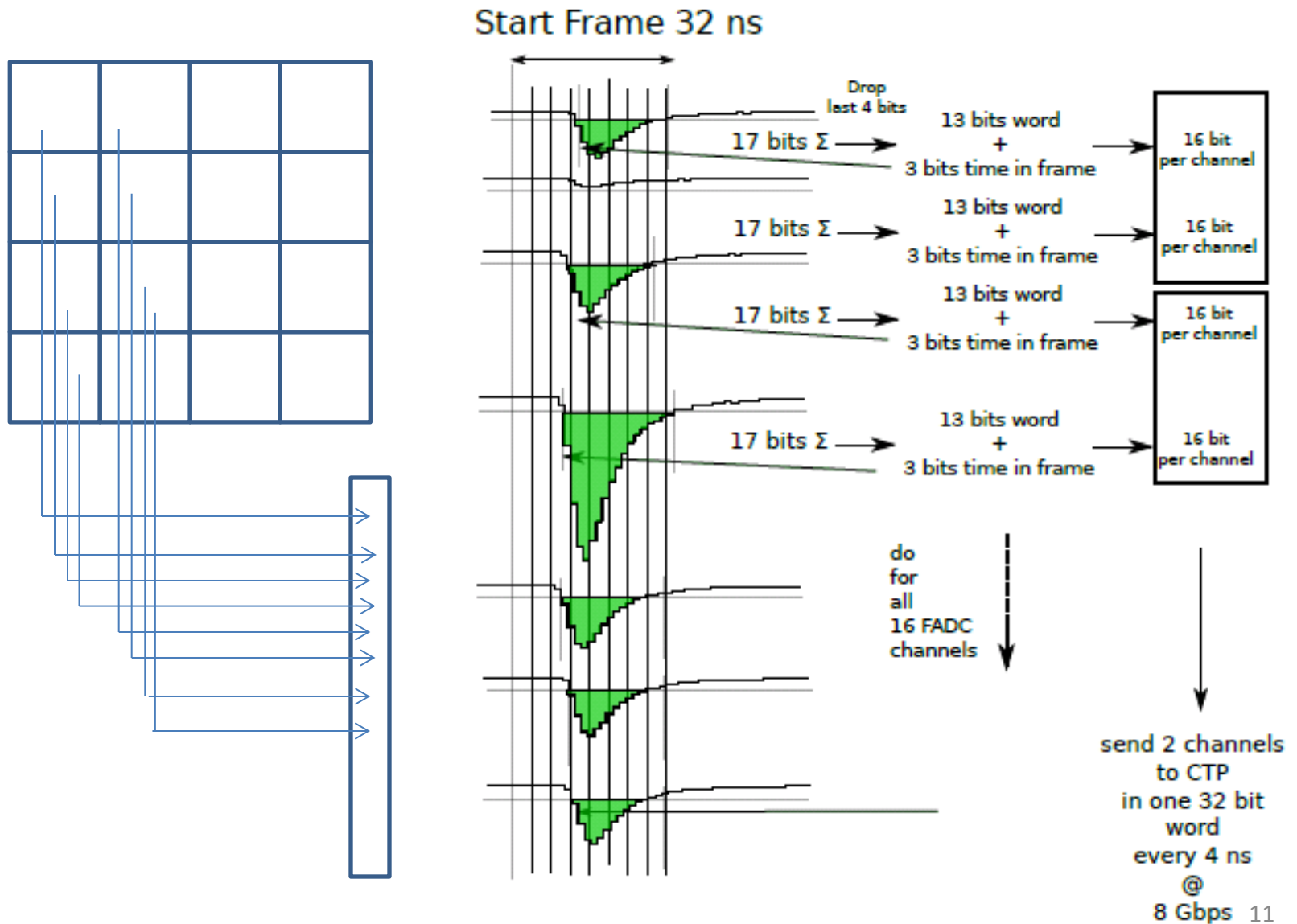- might need to optimize signal shape/integration

refshapem.txt
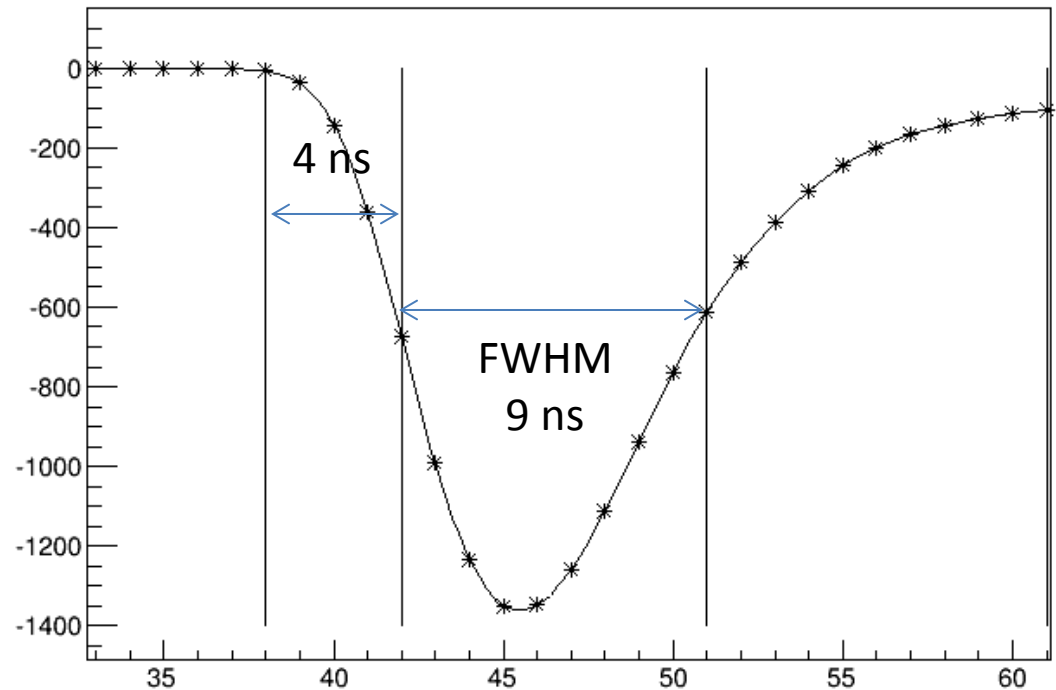
Typical calorimeter pulse recorded with 1 GHz Analog sampling electronics

Trigger test

- Test triggering
  - Triggering at interface of PbWO4 and PbF2 with calorimeter prototype
  - Useful to study effect of background on occupancy
  - Test clustering scheme
- Need VXS crate, CTP and 13 FADCs

Clustering HPS like

Start Frame 32 ns

Drop last 4 bits

17 bits Σ → 13 bits word + 3 bits time in frame → 16 bit per channel

17 bits Σ → 13 bits word + 3 bits time in frame → 16 bit per channel

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do for all 16 FADC channels

send 2 channels to CTP in one 32 bit word every 4 ns @ 8 Gbps

Hall A DVCS possible beam test
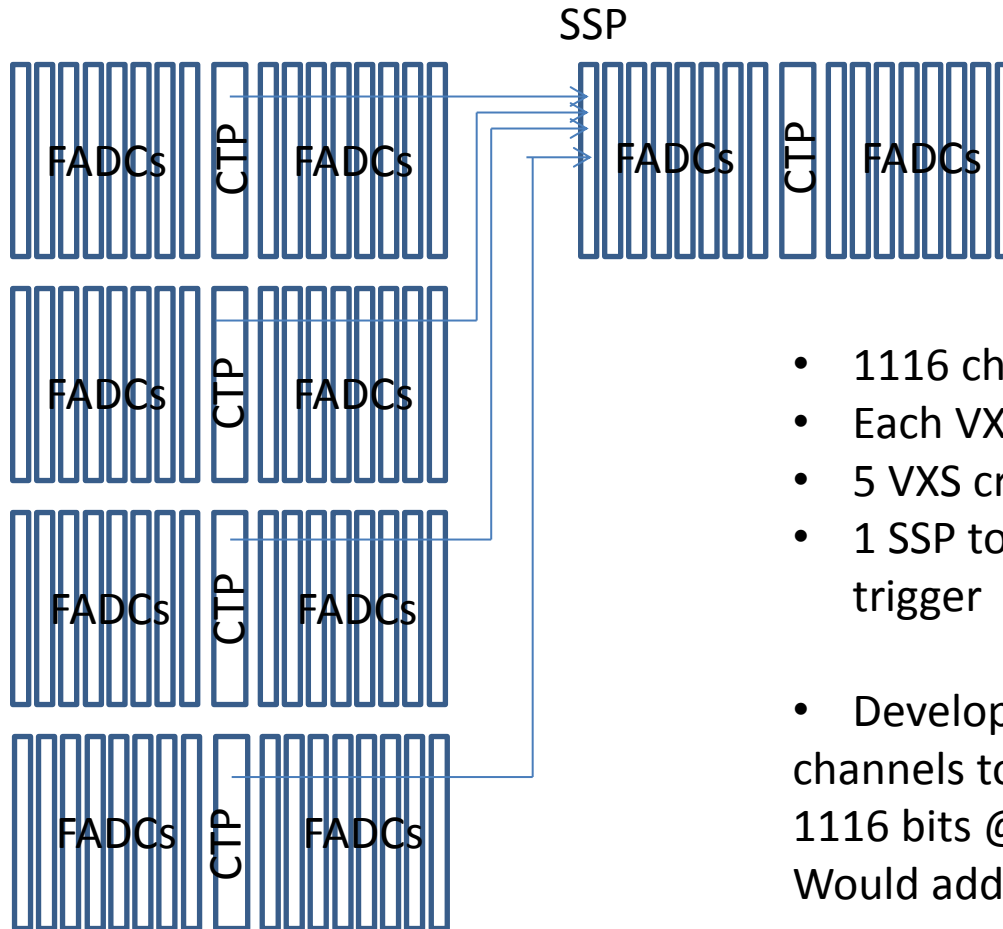
- Fall 2014 to ?
- Can test FADC in real beam condition
- Prototype PbF2 and PbWO$_4$
- If enough hardware possible dedicated test with full calorimeter to test trigger and FADC in full background
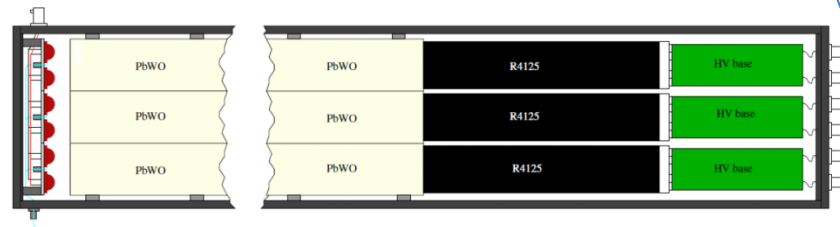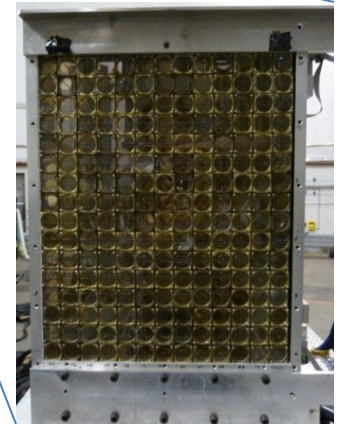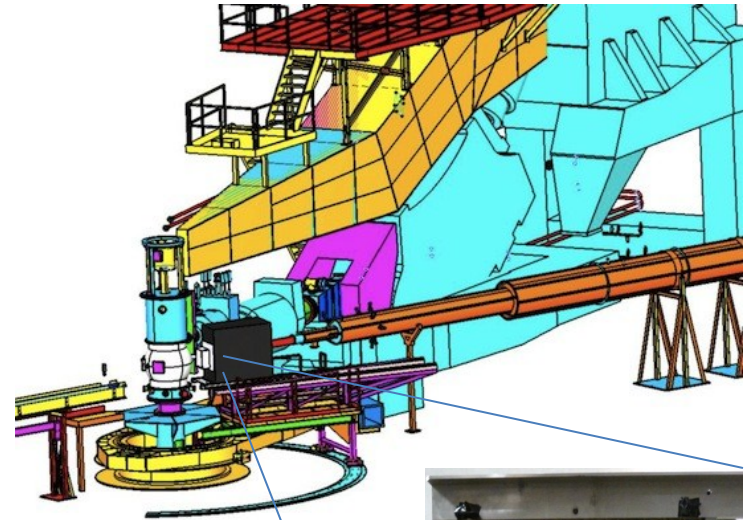
Full system layout

SSP

- 1116 channels
- Each VXS crate has 256 FADC channels
- 5 VXS crate
- 1 SSP to gather all signals and generate trigger

- Development to try to encode FADC channels to be read in trigger word
1116 bits @ 1 Gbps (upgrade possible ?)
Would add 1.116 us latency

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Possible development

- Readout depending on pulse "goodness"
  - Integral and time only if pulse looks standard
  - Full waveform

- Selective FADC channel readout : send bit pattern in trigger word to read out only FADC increase latency but could reduce data size in very noisy environment

FADC readout

- Only want to readout FADC channel in the cluster to reduce number of channels readout because of background

- CTP generates a 1116 bit pattern for channels to be read

- Send pattern to TI or FADC directly to trigger FADC

- Only channels from pattern are put in buffer

- Would introduce dead time but would be fine at low rate : 1116 assume 1 Gbit/s : 1.116 us additional latency (FADC max latency 3.2 us)

Conclusion

- Can start testing now with simple setup to check response of FADC with PbF2 signal and PbWO4

- If find VXS and CTP, can test triggering using Hall A DVCS calorimeter (cosmics and maybe in beam in Fall 2014) : would be useful to study effect of background

- New development of FADC capabilities could benefit NPS and future experiments