FDC On-Chamber Electronics – v3.0

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Abstract

This document details the layout and design choices for the on-chamber electronics. Specifically this write-up focusses on the component choices for the signal and high voltage boards for the wire planes.

The FDC system electrostatics are controlled by three potentials. The cathode planes at ground, the sense wires at 1650 V, and the field wires at -300 V. These settings are for the chamber operated in a gas environment of 90% argon - 10% CO_2. The maximum sense wire voltage will be no more than 2200 V if other gas mixtures are employed.

A schematic layout of the signal board (STB) and the high voltage board (HVTB) is shown in Fig. 1. The upper board represents the STB and the lower board represents the HVTB. The main issues with designing the circuit for the anode wires are the definitions of the decoupling capacitor and the coupling resistor. The main issue associated with the high voltage board is the design of the low-pass filters for the input high voltage lines.

Decoupling Capacitors

The decoupling capacitors go between the sense wires at positive high voltage and the preamplifiers mounted on the daughter board. The discussion in this section follows the reasoning laid out in Ref. [1]. The minimum size of the decoupling capacitor is set by the maximum signal loss allowed and any systematic errors that might occur due to tolerances of the capacitors. The capacitor should be no larger than required to minimize stored energy so that the preamplifiers are not damaged. Secondly, the capacitor should be as small as possible so as to differentiate sense wire noise pickup with the RC time constant of the circuit formed by the decoupling capacitor and the input impedance of the preamplifier which is assumed to be about 70 Ω. The chamber capacitance is about 20 pF (of which 10 pF is for the wire). The coupling capacitor must allow at least 90% of the signal charge to pass to the preamplifier. This sets the capacitance to be about 200 pF since the decoupling capacitor and the chamber form a charge divider. Therefore 220 pF is a good (and standard) choice. The capacitor should be an NPO type. Note that this is the same choice made for the Hall B drift chambers.

The tolerance of the decoupling capacitors is controlled by three factors:

- The capacitor cannot be calibrated once installed on the chambers,
- One should restrict the signal loss to 10%,

- The dE/dX requirements are such that channel-to-channel variation in gain due to the electronics (after calibration) should contribute a negligible increase in the resolution of the chamber [2]. Variation of the decoupling capacitor value will show up as a variation in the gain, scaled by the ratio of sense wire capacitance to the decoupling capacitor (roughly 20 pF/220 pF≈0.1). Thus a 20% variation in the decoupling capacitor value will appear as a 2% variation in the gain. Therefore a 20% specification is reasonable for these capacitors. The decoupling capacitor should be 220 pF ± 10% NPO.

As the maximum chamber voltage will be no more than 2200 V for any choice of gas mixtures, capacitors rated at 3 kV are an acceptable choice.

Coupling Resistors

The coupling resistors go between the sense wires and the positive high voltage bus. The sense wire coupling resistor design is as follows. First the resistor value should be as large as possible. The upper limit is set by the current drawn by the chamber. A reasonable requirement is that the cell voltage does not change by more than 0.1% for the maximum ionization level expected in the cell. The reason is that the chamber sensitivity to sense wire voltage is: $\Delta G/G \sim 20 \cdot \Delta V/V$. This translates to a 2% gain variation for a 0.1% voltage variation. This is reasonable for dE/dX measurements.

We expect that for the longest wires, which have the highest rates, that the maximum expected currents would be on the order of 100 nA. Therefore the series resistance would be $R = 0.1\% \cdot 1650\ V/100\ nA \approx 10$ MΩ. A value here of 1 MΩ is more than reasonable here.

The next design choice is the resistor power rating. The arguments given here follow those given in Ref. [3]. The RC time constant for a sense wire is approximately 1 MΩ · 220 pF = 220 μs. If we instantaneously raise the potential across the 1 MΩ resistor to 2000 V, there will be a current of 2 mA, which falls off exponentially with time constant RC. The power dissipated in the resistor is $P = P_0 e^{-2t/RC}$, where P_0 is 4 W. The power level is above 0.125 W for less than 400 μs. The total Joule heating dissipated in the 1 MΩ resistor (given by $I^2 R \delta t$) is about 1.5 mJ. For the Hall B design they found that a 100 mJ heat load can burn out a resistor which is already at maximum heat dissipation. So a 1.5 mJ heat load on an unloaded resistor will not cause any damage. Resistors rated at 1/8 W are acceptable here.

Finally we must consider voltage drooping effects. When an avalanche occurs about a sense wire, electrons are deposited on the sense wire surface, reducing the positive charge density on the wire, and its voltage. New charge is supplied to the wire in a time period of approximately RC. A minimum ionizing particle produces roughly 100 ion pairs (total) per cm of track length in an argon/CO_2 mixture. If we assume a 2 cm track length and a gas gain of a few times 10^5, then the charge of such an avalanche is about 10 pC (where $Q = 100$ ions/cm $\cdot$ 2 cm $\cdot\ q_e \cdot G$). The amount of charge on the wire is dominated by the size of the decoupling capacitor, which is 220 pF. So the charge of the wire and capacitor is 2000 V · 220 pF = 450 nC. So, one avalanche changes the charge, and hence the voltage by 10 pC/450 nC, or 0.04 V out of 2000 V. So, one hundred minimum ionizing particles per RC time constant will cause a 4 V droop of operating voltage. For a 1 MΩ resistor, RC=220 μs, so the maximum rate (per wire) should be less than 450 kHz to prevent a 4 V droop of

operating voltage. This argument also tells us that for a 10 MΩ resistor, the maximum rate (per wire) should be less than 45 kHz to prevent a 4 V droop of operating voltage. This potential rate limitation also dictates the choice of a 1 MΩ resistor.

Low-Pass Filters

The filters on the input high voltage lines represent low pass filters. The design used here mimics the design used on the Hall B chambers. These filters are designed to attenuate any noise on the DC power supply lines. The 3 dB point of the filter ($1/2\pi RC$) is about 0.1 Hz. The choice for the filtering capacitor is chosen to be the same as for the decoupling capacitor, namely 220 pF. The component values are not critical. The other purpose of this circuit is to bleed off the charge of the system upon a power off condition.

Circuit Protection

The final item on the STB that is included is a 10 kΩ resistor from each sense line to ground. This connection is included for safety to prevent damage to the board and the electronics in case of an intermittent (or bad) connection in the circuit. It provides a path to ground to bleed off any excess charge. The component choice here of 10kΩ will have minimal impact on the normal operation of the readout.

References

[1] D. Coupal and D. Nelson, BaBar Technical Design Note TNDC-97-73, (1996).

[2] Note that this discussion is only relevant if the FDC chambers are used for dE/dX measurements from the anode wires.

[3] M.D. Mestayer, private communication.

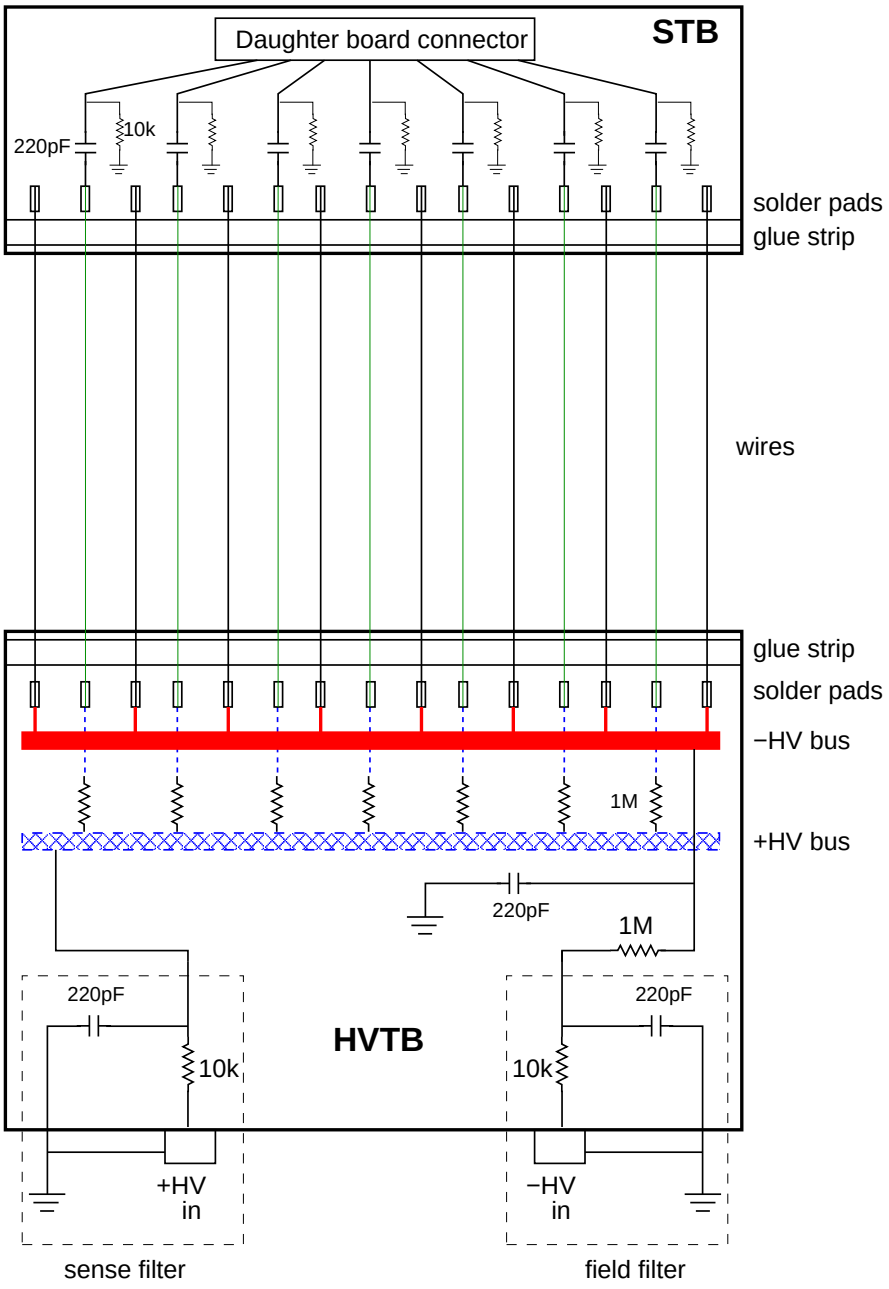

Figure 1: Schematic diagram showing the components and values for the FDC STB and HVTB boards.