Forward Drift Chamber Technical Design Report

Daniel S. Carman and Simon Taylor
Jefferson Laboratory, Newport News, VA 23606

February 20, 2007

Abstract

This report details the current design and status of the GlueX Forward Drift Chambers (FDCs). These chambers consist of a set of 24 planar drift chambers with cathode strip readout that is grouped into four identical packages of six chambers. Each active chamber layer should provide a position resolution of 200 μm. All aspects of the mechanical and electrical design are provided to justify the planned design. Results from our ongoing R&D program with a prototype cathode strip chamber are discussed to highlight the performance that has been achieved to date, and details related to the design and construction of a full-scale prototype chamber are provided. The goal is to construct a tracking detector that meets the required design specifications and has a long life time, a uniform and predictable response, a high efficiency, and is serviceable in case of component failure.

Contents

1 FDC Introduction

1.1 Overview

The Forward Drift Chamber (FDC) system in the GlueX detector in Hall D at Jefferson Lab (JLab) consists of a set of 24 planar drift chambers with cathode strip readout that is grouped into four identical packages of six chambers. This system is designed to track forward-going particles from the target ($1^\circ < \theta < 20^\circ$) in the 2-T magnetic field of the GlueX solenoid. A schematic picture of a single FDC package is shown in Fig. 1. The choice of cathode chambers with wire readout has been made for the FDC system in order to provide a three-dimensional space point from each active chamber layer. Due to the spiraling trajectories of the charged particles and the high multiplicity of charged tracks passing through the FDC, it is crucial for this system to be able to provide a sufficient number of measurements with appropriate redundancy to enable linking of the hits from the different tracks with high accuracy, while providing good spatial resolution with reasonable direction information. Fig. 2 shows the position of the FDC packages within the GlueX detector.

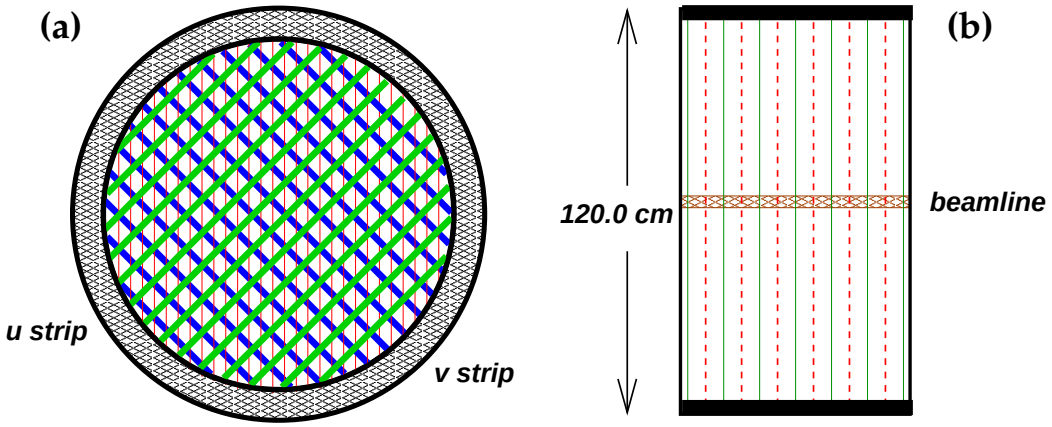

Figure 1: A front (a) and side (b) sketch of an FDC package. In (a) the wires are schematically indicated as the vertical lines. The U cathode strips are in front of the wires and the V cathode strips are behind the wires. In (b) is shown a side view of a six-chamber package. The wire planes are shown as the dashed lines, while the cathode planes are shown as the solid lines. Ground planes between adjacent chambers are not shown.

The primary development issues associated with the FDCs that must be addressed are factors affecting the intrinsic resolution of the chambers, along with the mechanical and electronics layout. The goal is to construct a tracking detector that meets the required design specifications and has a long life time, a uniform and predictable response, a high efficiency, and is serviceable in case of component failure.

Each chamber is 1.2 m in diameter and consists of a wire plane flanked on either side by cathode planes divided into thin strips as illustrated in Fig. 3. The strips are oriented at $\pm 45^\circ$ with respect to the wires and 90° with respect to each other. Neighboring chamber layers will be rotated by 60° with respect to each other in order to improve track reconstruction decisions on the corresponding left/right ambiguities in the wire planes, hence improving the overall

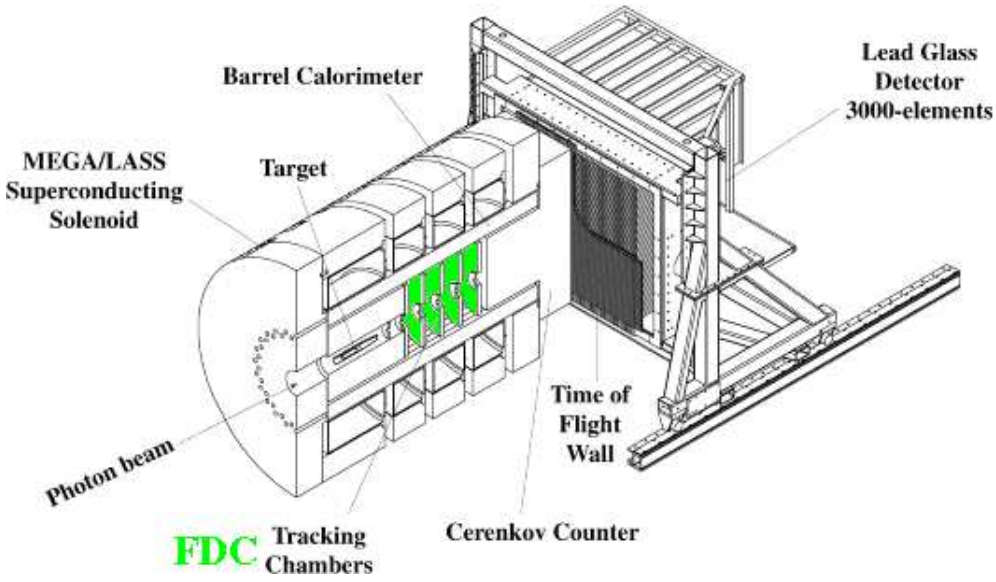

Figure 2: A schematic picture of the GlueX detector showing the location of the four FDC packages within the solenoid magnet and identifying the other detector subsystems.

resolution. By charge interpolation of the electron avalanche image charge in the cathode strip readout, spatial resolutions at the cathode planes should achieve the design goal for resolution of 200 μm. The purpose of crossing the strips is to provide redundant coordinate information, as well as to aid in pattern recognition in the background environment expected in the GlueX detector (see Section 1.2). The drift times from the wires will also be read out giving a precision coordinate in the dimension perpendicular to the wires that should meet the design goal of 200 μm. Fig. 4 shows a representation of a single FDC package from our three-dimensional CAD model of the design.

Additional information on the FDC system is included in the attached appendices. Appendix A contains the nominal FDC design parameters for the FDC detector system, Appendix B contains the construction schedule for these detectors, Appendix C includes information on the use of these chambers for particle identification by the dE/dX technique, and Appendix D provides an overview of the system construction budget.

1.2 Electrode Structure

Cathode strip chambers (CSC) are typically multiwire proportional chambers (MWPCs) with a symmetric drift cell in which the anode-cathode spacing d is equal to the anode wire pitch s (see Fig. 5). In these chambers the spatial resolution of the anode readout is limited to roughly $s/\sqrt{12}$ (RMS). In a CSC the precision coordinate is obtained by measuring the charge induced on a segmented cathode by the electron avalanche formed on the anode wire as shown in Fig. 6. However, CSCs can also be used to measure a three-dimensional space point on a track by rotating the opposing cathode plane strips at an angle with respect to each other. For the case of multiple tracks, a second segmented cathode can also help to reduce multi-hit ambiguities as shown in Fig. 7. The stereo technique is superior to the alternative of reading out only one cathode plane and a hit wire number in that multiple hits on a single wire may be resolved.

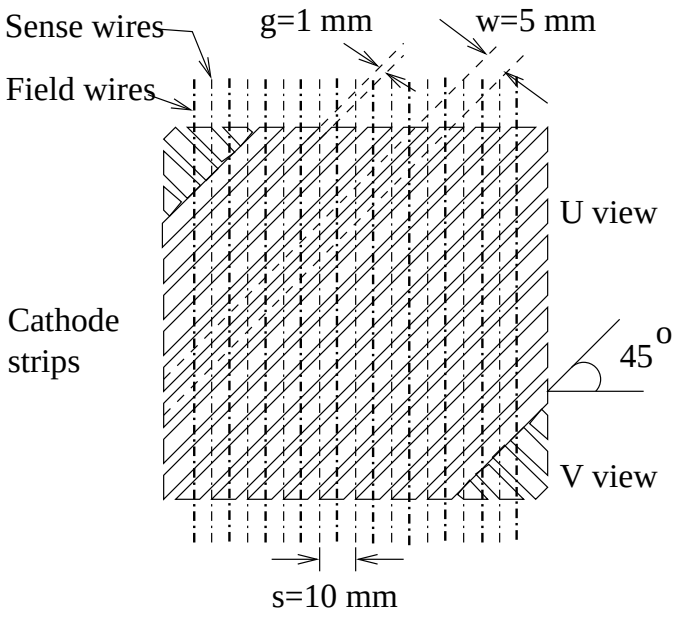

Figure 3: Schematic drawing of the orientation of the cathode strips flanking a given wire plane. The strip pitch w=5 mm and the strip-to-strip gap g=1 mm. The wire separation (sense wire to sense wire and field wire to field wire) is s=10 mm. The two cathode readout views are referred to as U and V.

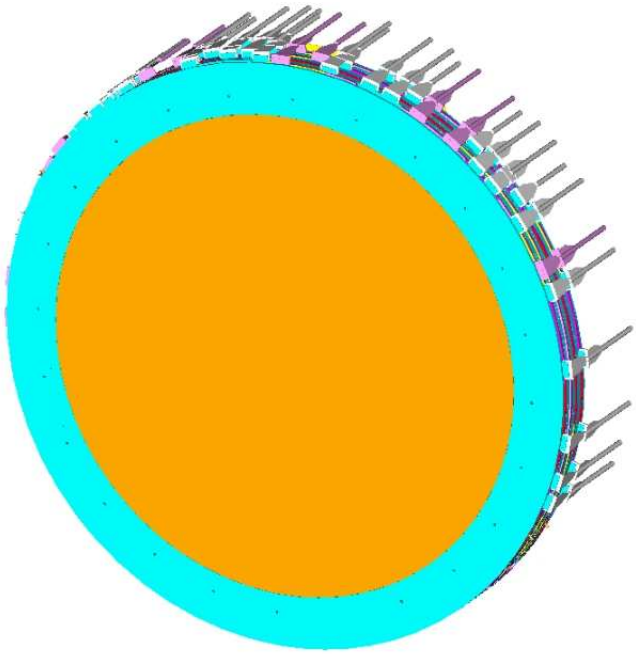

Figure 4: Three-dimensional CAD model of a single FDC package showing the positions and spacing of the readout cables on the package perimeter. The outer diameter of each package is 120 cm and the active area diameter of each package is 100 cm.

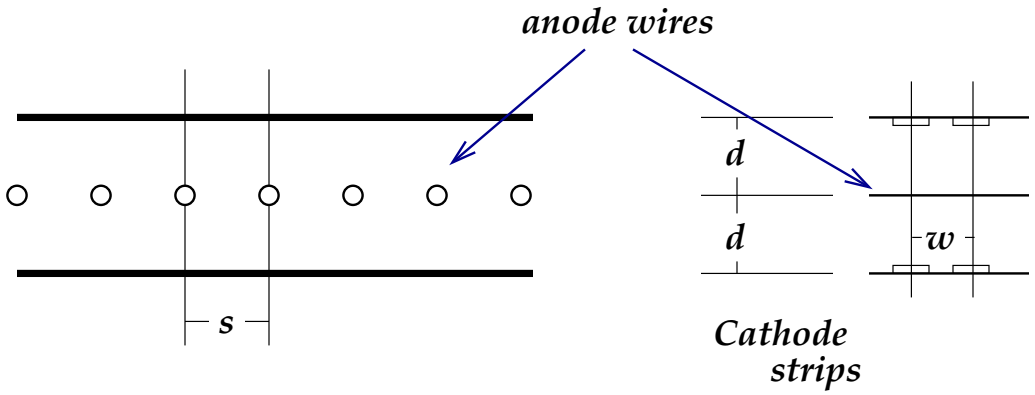

Figure 5: Schematic diagram of a generic cathode strip chamber defining the geometry described in the text.

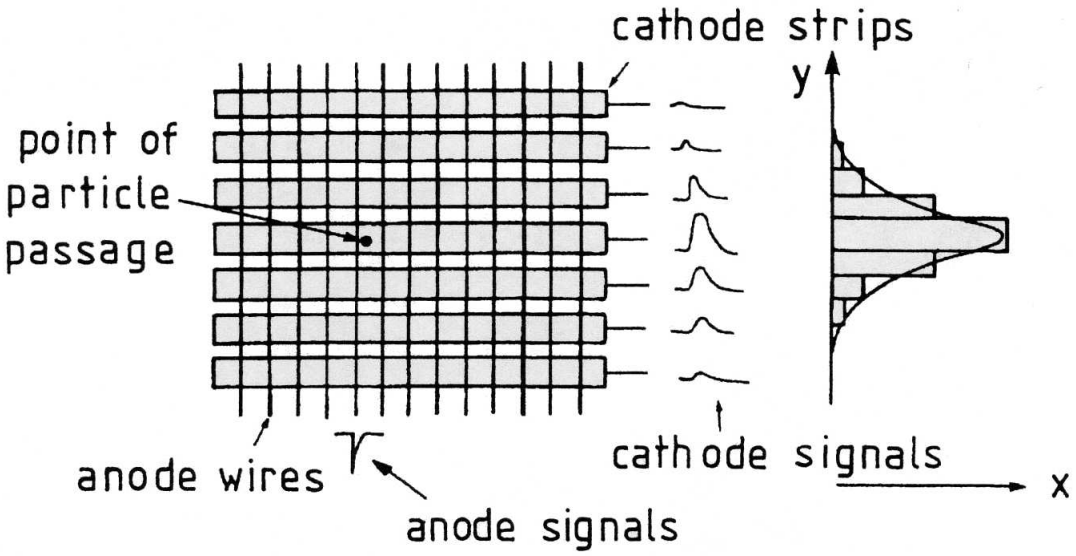

Figure 6: Illustration of the cathode readout in a typical MWPC.

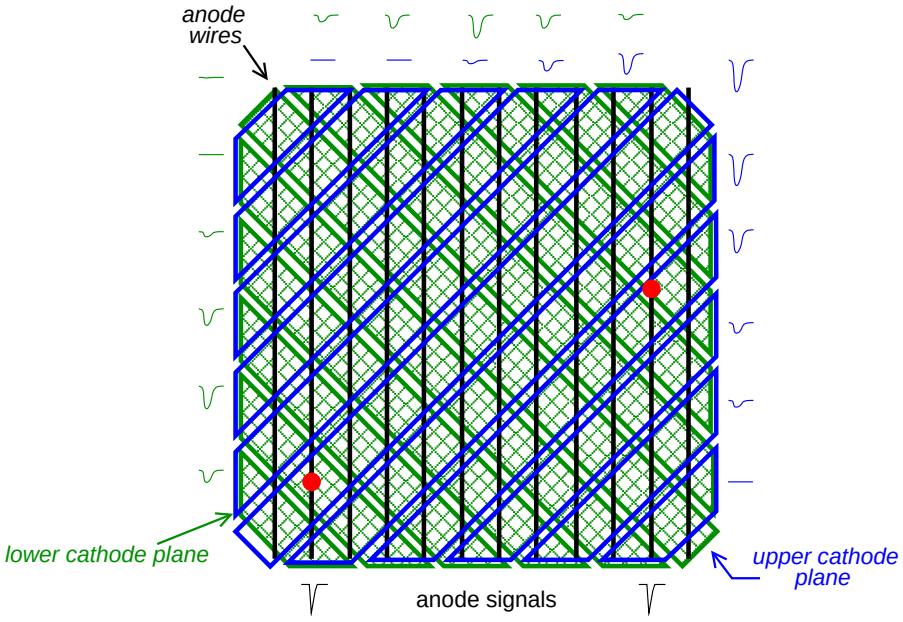

Figure 7: Illustration of the resolution of ambiguities within a CSC for two particle hits in a typical MWPC.

The optimum cathode readout pitch w is determined by the width of the induced charge distribution. It has been shown by several groups that minimal differential non-linearity ($\sim$1%) and optimal position resolution are achieved when $w/d \approx 1$ (e.g. Ref. [1]). This ratio is employed in the current FDC design.

An interesting question regarding cathode chambers regards the change in system resolution when they are also employed as drift chambers (MWDCs), specifically horizontal drift chambers. The principles of operation of a MWDC are such that the best position resolution is achieved when the first electrons that reach the anode wire drift along field lines in the plane of the wires. If we consider a GARFIELD calculation [2] of the field lines for a chamber with no field-shaping wires (see Fig. 8(a)), the first electrons to reach the anode wire will most certainly arise from other locations within the drift cell. This gives rise to non-linearities in the space-time correlation that strongly degrade the position resolution, especially in a strong magnetic field. In order to improve the field configuration for the MWDC operation, field-shaping wires can be included within the anode plane between each anode wire. This can clearly improve the field configuration as shown in Fig. 8(b). More details on the GARFIELD studies for the FDC chambers are given in Ref. [3].

One of the central questions that we have been investigating through our R&D program for the FDC system regards the optimal electrode structure in our cathode chambers. Specifically we are seeking to fully understand the trade-offs between timing resolution from the wire planes and spatial resolution from the cathode planes. The main question is how the inclusion of field-shaping wires affects the cathode position resolution. The results from our prototype studies (discussed in Section 7), indicate that there is no degradation of the cathode resolution when field-shaping wires are included in the design. This is a novel aspect of our chamber design.

The nominal design of our FDC drift cells is square, with a sense wire separation of

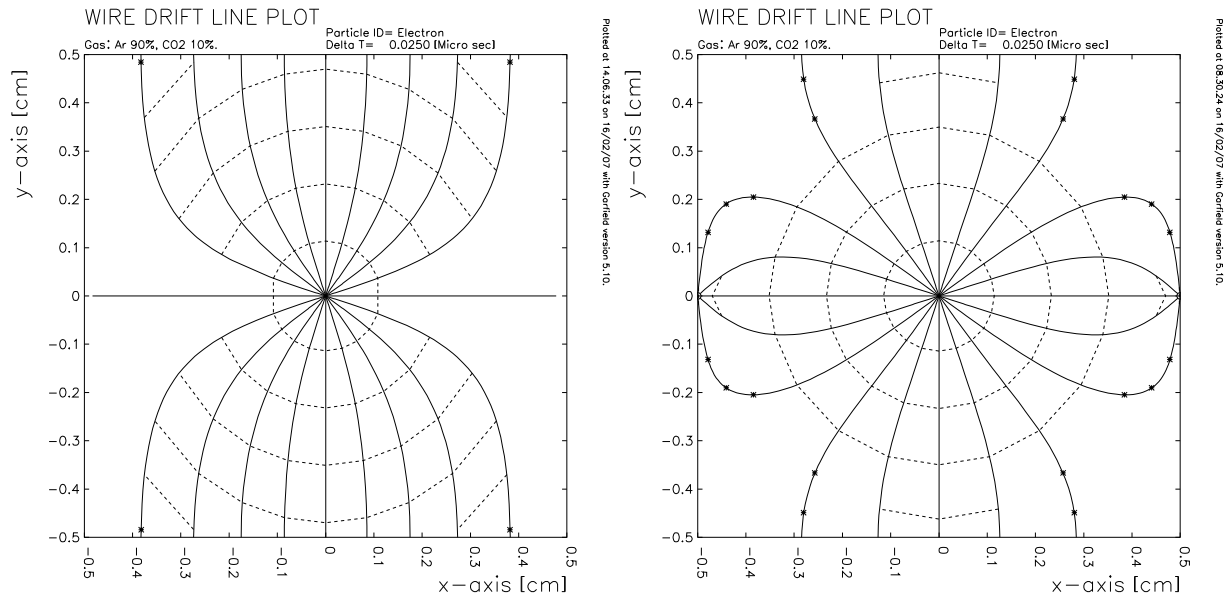

Figure 8: GARFIELD calculations of the electric field lines (for a B=0 field configuration) within a square drift cell for a 90% argon - 10% CO_2 gas mixture for electrode configurations without (left) and with (right) field-shaping wires.

10 mm and a field wire separation of 10 mm (sense wire to field wire separation is 5 mm). The chamber half gap (wire plane to cathode plane separation) is 5 mm. The 5 mm half gap is matched by a 5 mm cathode strip pitch. The geometrical parameters for the FDC electrodes are given in Table 1.2.

Parameter	**Value**
Sense wire separation	10 mm
Field wire separation	10 mm
Sense-to-field wire separation	5 mm
Half Gap	5 mm
Cathode strip pitch	5 mm
Cathode strip separation	1 mm

Table 1: Geometrical parameters for the electrode structure of the FDC system.

As mentioned above, the cathode strips flanking each wire layer have been oriented to $\pm 45°$ relative to the wire direction. This orientation has been chosen for two reasons. Firstly this allows the cathodes in each chamber layer to be calibrated without having to define an external track. This occurs as one coordinate of the strip information images the wire location. The design also allows for a straightforward technique to assign the cathode hits to the associated anode wires when multiple tracks and background hits are present in the chamber. Again this occurs as one coordinate of the strip charge information images the wire. The cathode hits on the U and V layers that are associated with a given wire must contain the same coordinate information (charge). The impact on the cathode resolution due

to this choice of angle needs additional study and the angle of rotation of the strips needs to be optimized to maximize the resolution on one hand, and to minimize multi-track hit ambiguities on the other hand. Studies of our prototype cathode chamber in a configuration with the strips oriented at 90° with respect to the wire are now getting underway.

1.3 Wire Plane Orientation

A current open issue in the design is the orientation and positioning of the neighboring wire layers within an FDC package. Our nominal design for the direction of the wires in each package is such that each wire plane is rotated by 60° relative to its neighbors as shown in Fig. 9. This design allows for a single wire plane board for all layers. The chamber frame has holes every 15° to allow for the different orientations. In this design the question of successful resolution of the left/right ambiguities in the wire plane is a potential issue. This design scheme thus requires resolution of the local ambiguities via a global track fit.

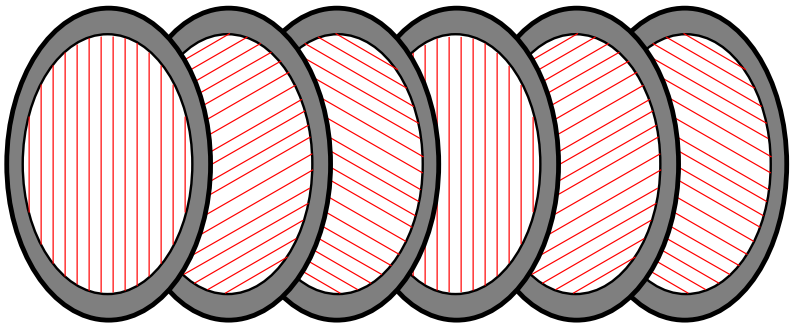

Figure 9: Schematic exploded view of the wire planes and their wire orientations in the nominal FDC design. Here each wire layer is rotated by 60° relative to neighboring layers.

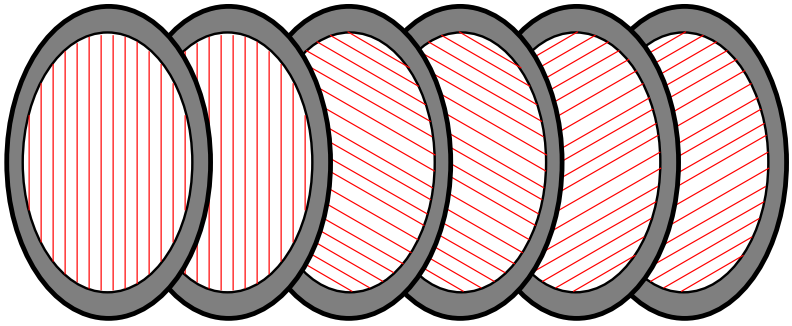

Figure 10: Schematic exploded view of the wire planes and their wire orientations in an alternative FDC design. Here sets of two wire planes are grouped together with wires running in the same direction but with a half-cell offset in the wires.

We have begun to consider a design that is more suitable to resolve left/right ambiguities in the wire plane locally. This design, shown in Fig. 10, places wire layers with the same orientation next to each other. These neighboring layers would then be designed with a half drift cell offset between them. This design would require two different types of anode circuit boards (leading to increased costs) and also has a potential problem with covering the full

active area of FDC as the sense wires must have a field wire on either side to provide for high efficiency and a linear time-to-distance relation. A half-cell offset would end the wire plane with a sense wire.

At the current point in time, it is not clear which design is optimal for tracking within GlueX. Simulation work is ongoing to allow us to more fully understand the issues involved. However we suspect that the second option above could allow for more flexibility in the track reconstruction algorithms, whether or not it leads to improved tracking resolution.

2 FDC Design

Each wire plane consists of alternating field and sense wires, with a sense to field wire separation of 5 mm and a wire plane to cathode plane separation of 5 mm. The nominal design for the cathode planes calls for a strip pitch of 5 mm and a strip-to-strip separation of 1 mm (see Fig. 11). The strips will lie on a 1-mil thick Kapton backing. The strips themselves will be copper with a thickness of 1/7 oz (5 μm) (this represents the thinnest practical choice for performance). A ground plane is included between neighboring cathode planes to ensure minimal signal cross-talk. The sense wires will be at a positive high voltage, the field wires at negative high voltage, and the cathode planes will be a ground. The number of sense wires on each wire plane is 96 and the number of field wires is 97. Each cathode plane consists of 192 cathode strips. The total number of anode wires per FDC package is 576 and the number of cathode strips per FDC package is 2304. The total number of readout channels for the full FDC system is 11520.

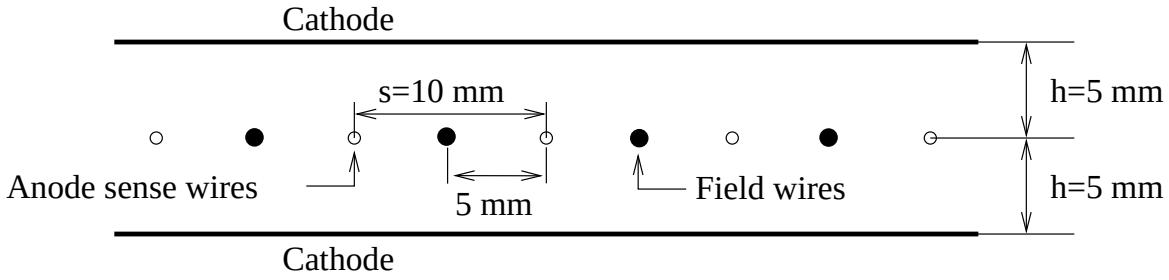

Figure 11: Schematic end view (wires projecting into and out of the plane of the page) defining the nominal electrode geometry of the FDC system.

The anode wire for the chambers will consist of 20-μm diameter gold-plated tungsten. The expected electronics gain and thresholds dictate that the gas gain be $\sim 10^5$. Under this condition, the electric field at the surface of the sense wires is $\approx$260 kV/cm. The field-wire diameter is chosen to ensure that the electric field at their surface remains below 20 kV/cm to minimize conditions causing cathode deposits [4, 5]. The field wires will be 80 μm diameter gold-plated copper-beryllium (Cu-Be).

The wires that cross through the beam line require special treatment to handle the otherwise unmanageable rates. The diameter of the sense wires will be increased within a radius of $\sim$3.5 cm by electroplating a few mils of additional copper onto the wire (a technique perfected at Fermilab). This reduces the surface electric field on this portion of the wire so the gain is reduced below the level necessary for the electron avalanche to be formed.

A side view of the basic sub-unit that makes up each FDC package is shown in Fig. 12. This schematic picture shows the wire plane and its two associated cathode planes. The present design of the FDC system employs Rohacell foam backing on each cathode to support it and to define its flatness. Minimization of the overall chamber thickness in the active area is important to reduce multiple scattering and energy loss effects that lead to worsened position resolution. Minimization of the overall package thickness in the inactive area (frames, electronics, circuit boards, cabling, supports, etc) is important to minimize photon absorption and to reduce impacts on the performance of the barrel calorimeter outside of

the FDCs. Table 2 provides a list of the materials in the active and inactive portions of the FDC system. The thickness of the materials in the active area of each package has been computed to be 0.33 gm/cm^2, roughly half of which is due to the Rohacell foam cathode supports. More details on the electronics and cables are given separately in Sections 6 and 6.5, respectively.

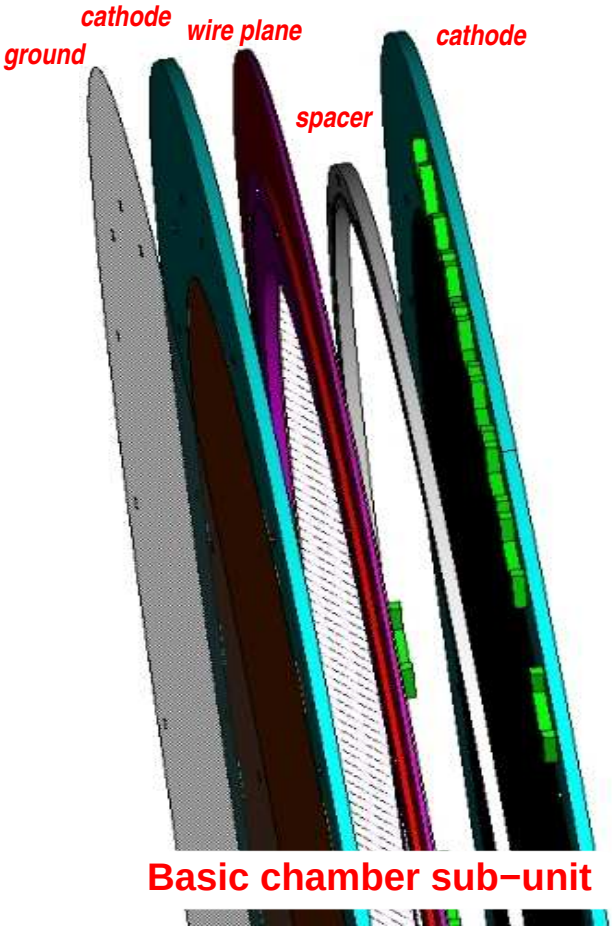

Figure 12: Side view of the basic FDC chamber sub-unit from our three-dimensional CAD model. Shown is a subunit that forms an active readout layer (wire plane and two cathodes). The ground plane that isolates neighboring layers is also shown. Each FDC package contains 6 of these subunits.

Active Area Materials	**Inactive Area Materials**
Sense wire: 20 μm Au-plated W	Wire frames: 5 mm g10
Field wire: 80 μm Au-plated Cu-Be	Cathode frames: 5 mm g10
Cathodes: 1 mil Kapton, 1/7 oz Cu	Spacers: 5 mm CH_2
Cathode Backing: 5 mm L.D. Rohacell foam	Cables
Ground Planes: 6.3 μm mylar	Electronics
Epoxy: 25 μm layers	Support frame

Table 2: A listing of the materials in the active and inactive portions of the FDC system.

3 Monte Carlo Studies

The initial specifications for the layout of the FDC system were studied within the framework of a fast parametric Monte Carlo (as the GEANT3 simulation was not advanced enough at the time of these studies). This simulation included a realistic representation of the FDC geometry and materials and a realistic magnetic field for the GlueX solenoid. Since that time detailed comparisons made between the fast Monte Carlo results and our GEANT3 simulation show good agreement for results.

The goals of the studies with the fast Monte Carlo were twofold. First the basic number of FDC chamber packages within the solenoid was considered, as well as the number of drift chamber layers within each package. For these studies, pions with momenta between 0.25 and 4.0 GeV were generated and the momentum uncertainty in the form of $\Delta p/p$ was studied as a function of momentum. Fig. 13 shows a typical result comparing a 3-package vs. a 4-package configuration (with packages equally spaced along the beam line). Here the preliminary results make it apparent that the single track resolution, if all cathode and anode positions can be resolved to 150 μm, has improved resolution with the 4-package configuration. Although the resolution becomes worse with increasing momentum, the resolution of the 4-package configuration does so at a slower rate than the 3-package configuration. The tracking system design parameters can be met with such a 4-package configuration. However, it is the redundancy that the fourth package provides that will be crucial in disentangling multiple charged particle hits and background within the readout time window. Note that these results are currently being verified with our GEANT3 simulation.

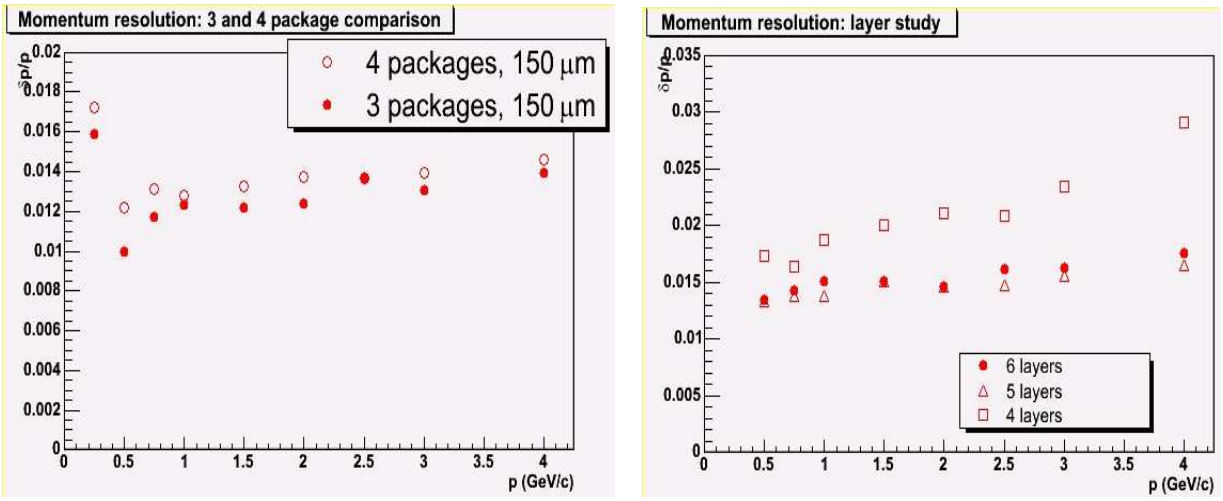

Figure 13: (Left) Monte Carlo studies comparing the FDC resolution in a configuration with three packages vs. four packages. (Right) Monte Carlo studies comparing the FDC resolution for four packages but varying the number of active layers in each package. These studies were performed assuming a position resolution in each layer of 150 μm and did not include the Rohacell backing material.

Fig. 13 shows a comparison of the Monte Carlo results for 4 FDC packages, but varying the number of active layers in each package. These studies show that a configuration with only 4 layers in each package is not acceptable. The 6-layer design can achieve our momentum resolution goal. The inclusion of the sixth active layer is essential to enable

pattern recognition for multiple tracks and background in the FDC system. The goal to optimize the position and momentum resolution is to resolve position ambiguities locally within each package and then to perform global track fits. Further information on these studies is provided in Refs. [6, 7].

The main GlueX simulation studies have been done using a full GEANT3 Monte Carlo simulation. The description of what is included in the simulation is contained in Ref. [8]. These simulations include a complete and realistic description of the FDC chambers, including the electrodes, chamber frames, and cables. The same reconstruction software that has been used to reconstruct the data from our small-scale prototype chamber is built into the simulation. Representative results from these simulations are included in Figs. 14-17 which show the momentum resolution ($\Delta p/p$) vs. momentum and angle and the angular resolution ($\Delta\theta/\theta$) vs. momentum and angle for the nominal chamber resolutions and for the case of infinitely good resolution. These studies motivate the position resolution specification of 200 μm for the FDC system.

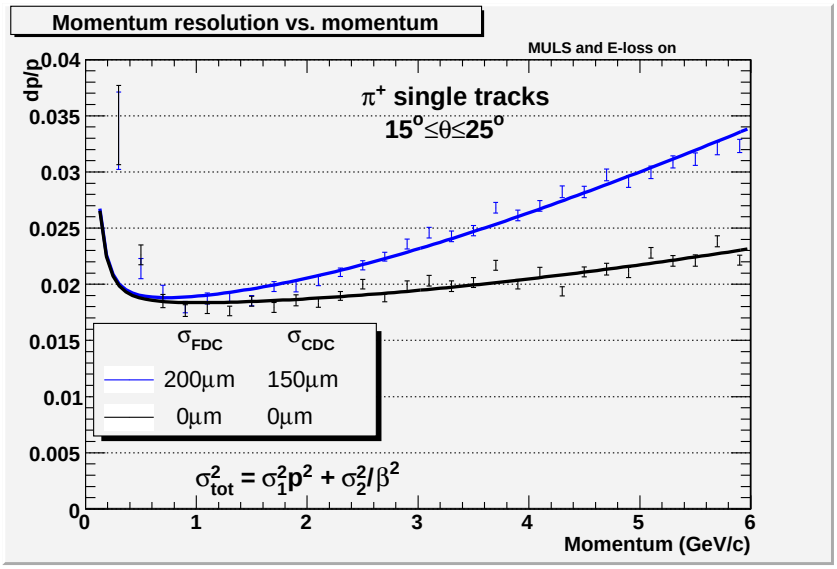

Figure 14: GEANT3 simulation results for the momentum resolution $\Delta p/p$ of GlueX vs. momentum for π^+ tracks between 15° and 25° for the nominal position resolutions and for the case where the resolutions are infinitely good.

The active area of the FDC will be limited by the requirement that the frames support the tension on the wires with minimal distortions. In addition, space must be left outside of the FDC for the signal, HV, and LV cables. The space about the perimeter of the FDC for cables is required to be 5 cm. The support frames have a radial thickness of 10 cm. A GEANT3 Monte Carlo study was performed to assess the effect on the acceptance on the active radii of the FDC packages. Single muon tracks were thrown at all angles with respect to the direction of the beam with momenta in the range 0–9 GeV. To be accepted, the primary track was required to create at least 8 hits in a tracking detector (FDC or CDC). Plots of the detector coverage for several choices of the active area of the FDC chambers are shown in Fig. 18. At an outer radius of about 49 cm and below, some events require hits in both the FDC and the CDC to be accepted because there is no longer an overlap between the two detectors. At an outer radius of 33 cm and below, holes in the acceptance start to

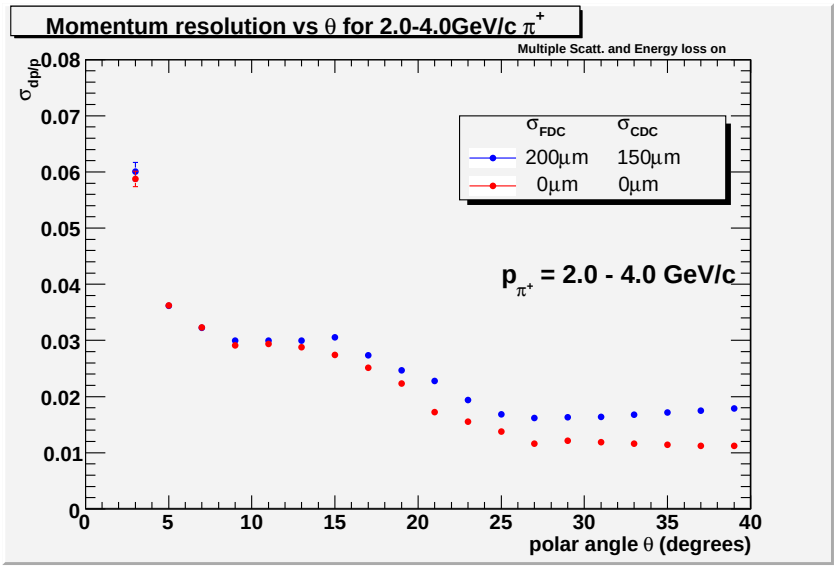

Figure 15: GEANT3 simulation results for the momentum resolution $\Delta p/p$ of GlueX vs. angle for π^+ tracks in the range from 2.0 to 4.0 GeV for the nominal position resolutions and for the case where the resolutions are infinitely good.

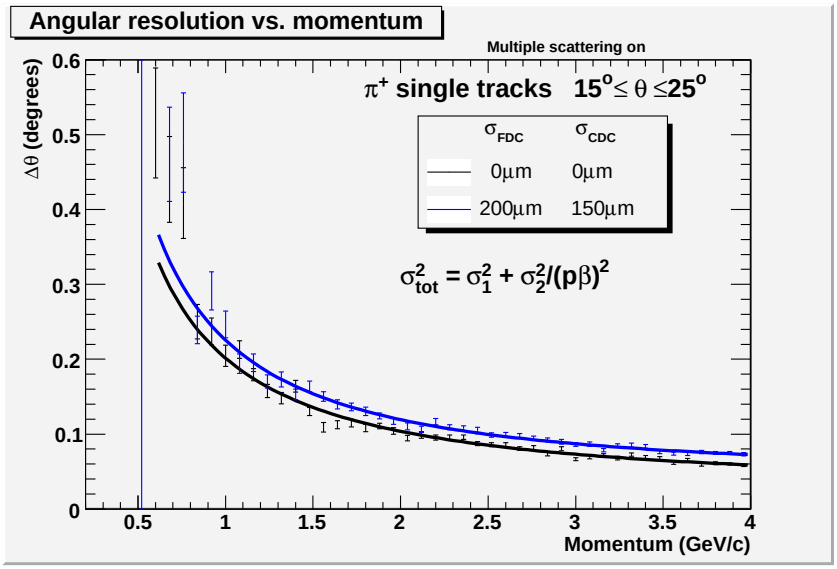

Figure 16: GEANT3 simulation results for the angular resolution $\Delta\theta/\theta$ of GlueX vs. momentum for π^+ tracks between 15° and 25° for the nominal position resolutions and for the case where the resolutions are infinitely good.

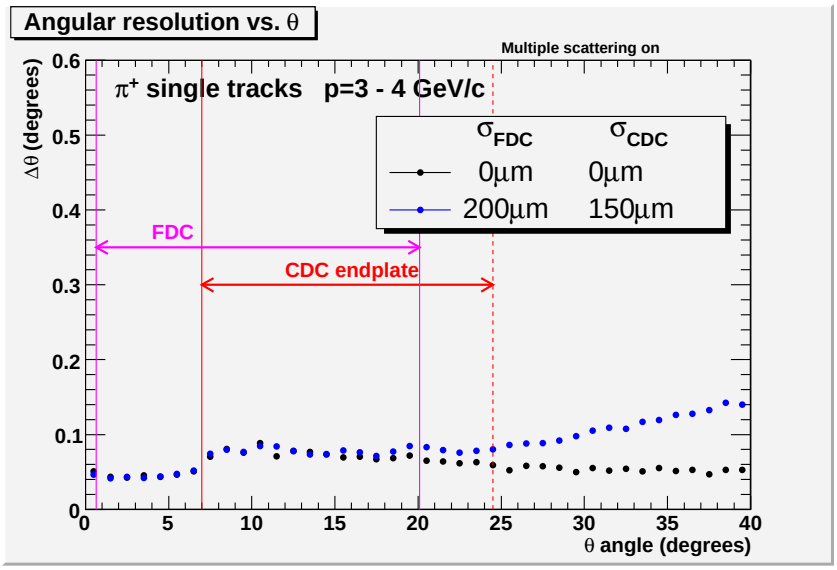

Figure 17: GEANT3 simulation results for the angular resolution $\Delta\theta/\theta$ of GlueX vs. angle for π^+ tracks in the range from 3.0 to 4.0 GeV for the nominal position resolutions and for the case where the resolutions are infinitely good.

appear. Thus the designed active area of the FDC (r=55 cm) is well matched to the GlueX hermiticity requirement.

The GlueX GEANT3 Monte Carlo is also being used to study the expected rates in each of the detector subsystems. An example of these calculations is shown in Fig. 19. Here the expected rates in the most upstream and most downstream FDC anode and cathode layers are shown as a function of the transverse dimension. Clearly indicated are the high rates near the central photon beam line. If this issue was not addressed in the FDC design, the chambers could not handle these rates. In the FDC chambers we will increase the diameter of the sense wires in the region of the beam line (to a radius of 3.5 cm) by electroplating several mils of copper on the wires to deaden them. The rate studies also indicate the expectations for chamber operation within the GlueX system at the expected operating flux of 10^8 photons/sec. We should expect a typical event to have 3-6 charged tracks with 1-2 background tracks, along with a cell occupancy of a few percent from photon conversions.

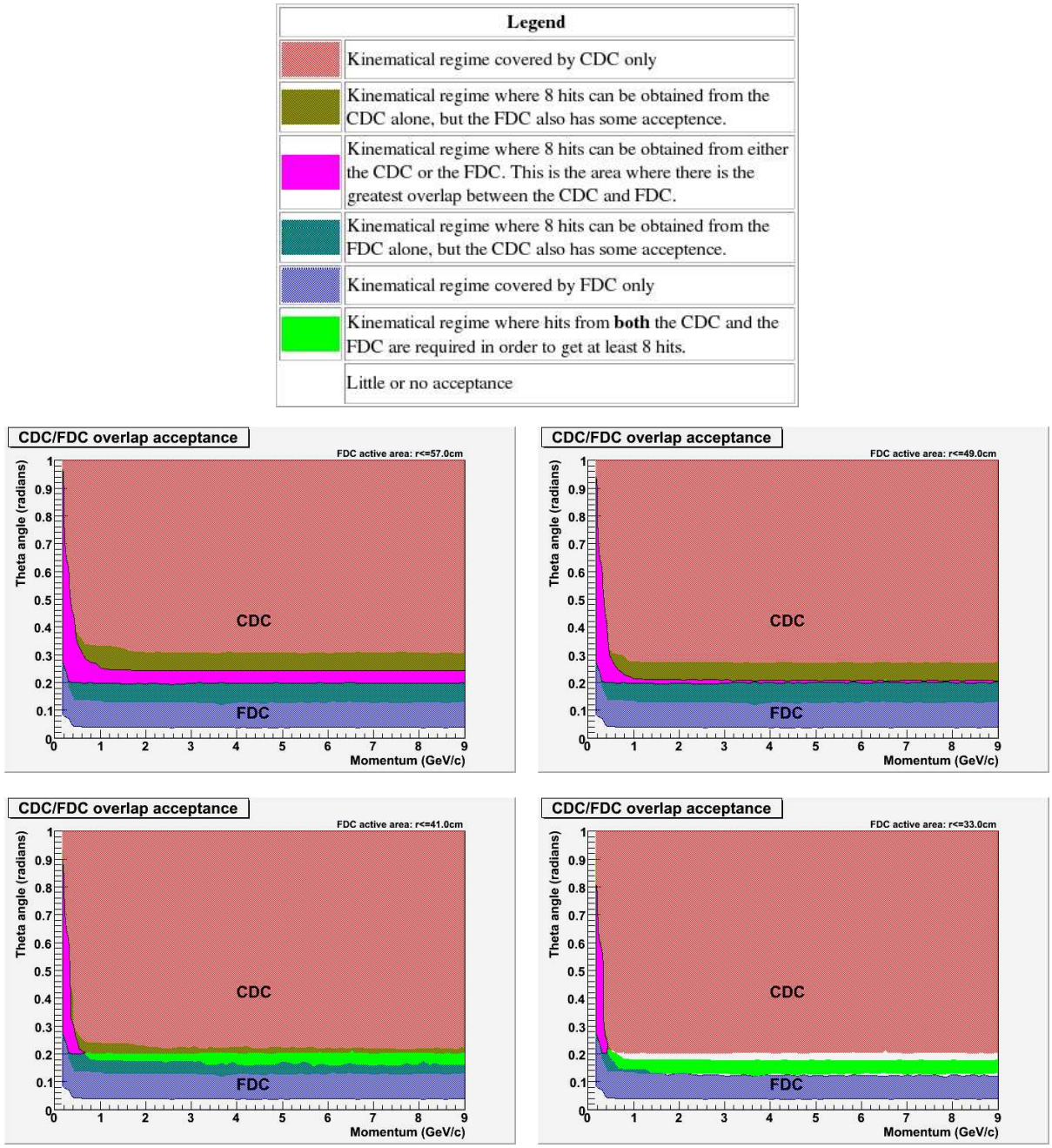

Figure 18: Acceptance as a function of momentum and angle for the FDC and CDC for FDC active area radii of r=57 cm (upper left), r=49 cm (upper right), r=41 cm (lower left), and r=33 cm (lower right).

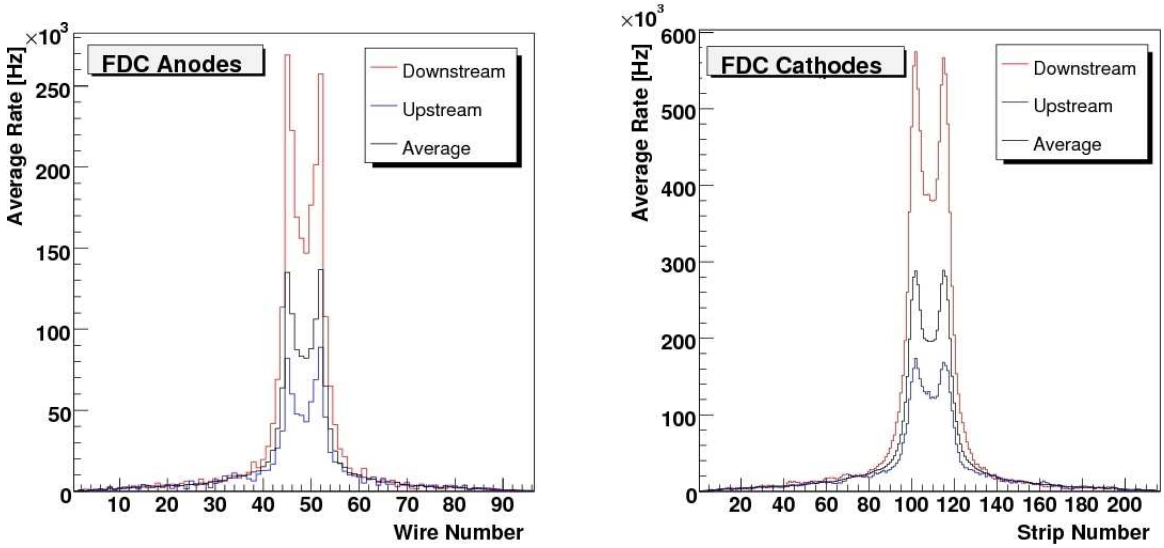

Figure 19: Expected total rates in the most upstream and most downstream FDC anode and cathode layers as a function of the transverse coordinate.

4 Wire Planes

A schematic picture of the basic wire plane layout is shown in Fig. 20. Each wire plane consists of 96 sense wires made from 20 μm diameter gold-plated tungsten alternated with 97 field wires made from 80 μm diameter gold-plated Cu-Be. The active area of each wire plane has a diameter of about 100 cm, such that the wire sense-to-field wire spacing is 5 mm. The frame is designed with the signal readout on one side of the frame (the signal side) and the HV connected to the other side (the HV side). Due to limitations in the size of the circuit boards that can be manufactured, the signal side of the wire plane consists of 3 separate multi-layer circuit boards (called signal translator boards – STBs) and the high-voltage side of the wire plane consists of 3 separate multi-layer circuit boards (called high voltage translator boards – HVTBs). These circuit boards will be made from g10 boards of thickness 1/32″ that will be laminated onto a g10 frame, giving an overall wire plane thickness of 5 mm.

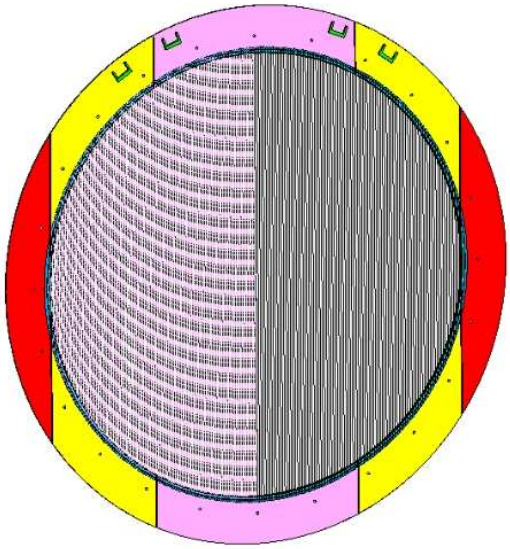

Figure 20: Schematic picture of a wire plane. In this view the upper portion of the board is the signal side that includes three STB boards and the connectors for the preamplifier daughter boards. The lower portion of the board contains three HVTB boards where the high voltage connections are made. The two side portions of the board contain the gas inlet and outlet connections for each plane.

The basic circuitry on each STB and HVTB is shown in Fig. 21. On the STB side the preamplifiers are isolated from the HV by 3kV-rated 220 pF blocking capacitors. Small 10k resistors are included on the preamplifier side of the wire to ground to prevent damage to the board and the electronics in case of an intermittent (or bad) connection in the circuit. These resistors provide a path to bleed off any excess charge. On the HVTB side we include a low pass filter on each supply line to attenuate noise. 1M coupling resistors from the HV buses to the sense are field wires define and limit the currents. The basic concepts for the FDC STB and HVTB circuit design are the same as those in the current CLAS drift chamber system. More details on the circuit layouts for the STB and HVTB boards is contained in Ref. [9].

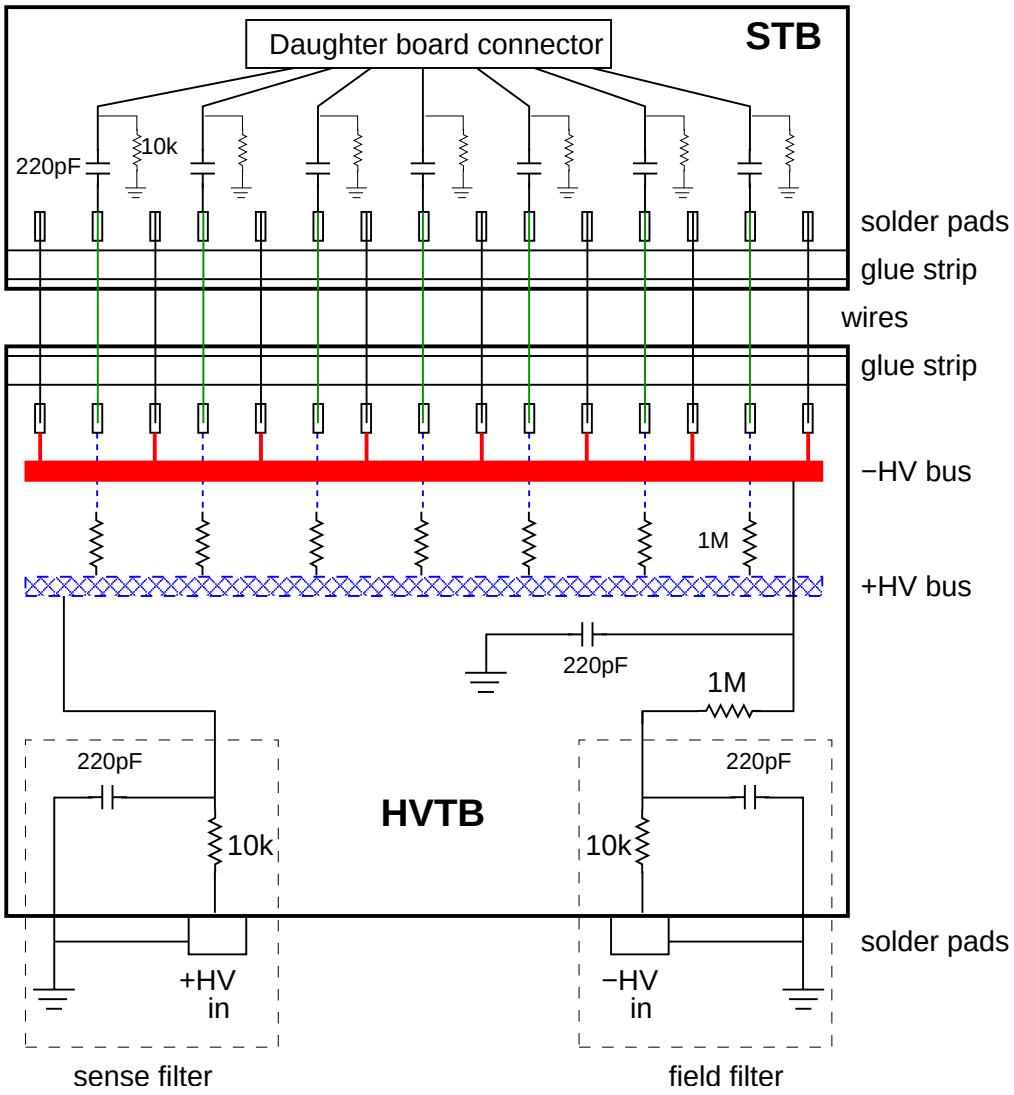

Figure 21: Layout of the basic circuitry on the STB and HVTB boards. While the geometry of the boards here is schematic, the circuits drawn show the STB and HVTB circuitry and component values that are planned.

A close up of the central STB is shown in Fig. 22. In this figure the trace layouts are schematic, however the remainder of the board reflects our current design. The board is planned to be a 4-layer design, and the traces shown were an initial attempt to ensure that there was sufficient real estate to place the traces and to define appropriate chamber grounds. The STB shows the solder pads for the sense and field wires. Inside of these pads is a 3-mm gap to lay down an epoxy glue strip that will hold the wire tensions before they are soldered into place. The capacitors shown are surface-mounted, and will actually be placed on the back side of the board due to their physical size. The traces from the capacitors to the readout board go on the back side of the board as the region between the capacitors and the resistors is an o-ring surface.

The preamplifiers, voltage regulation, and calibration circuitry will be incorporated on a separate daughter board. These boards plug into the connectors shown in Fig. 22 and

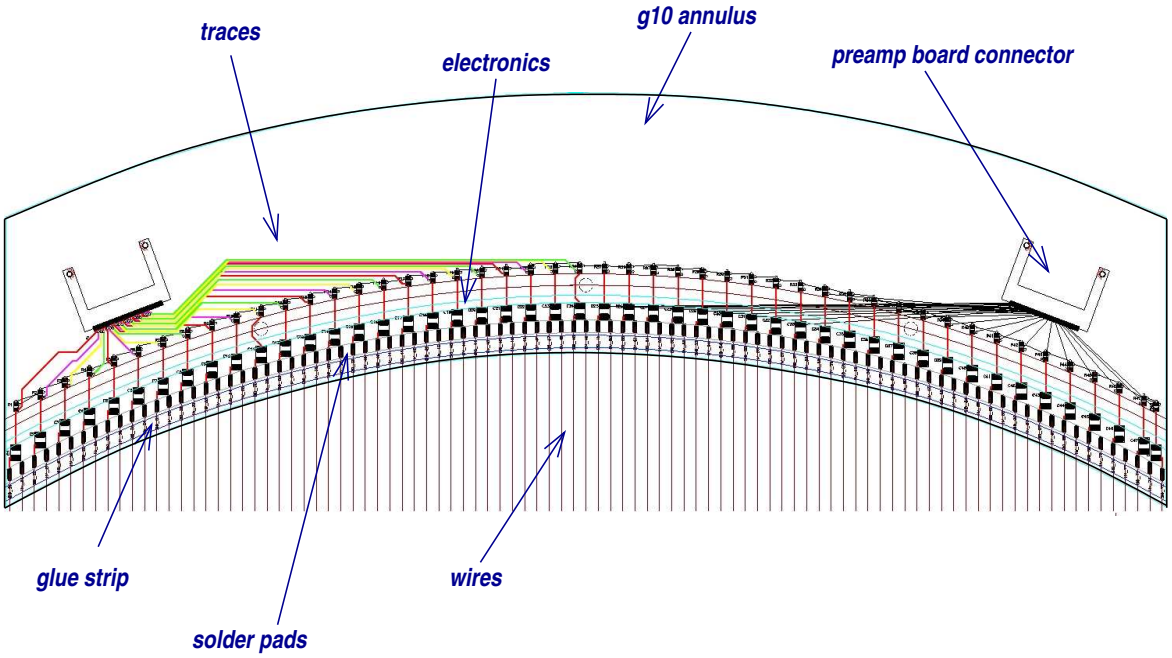

Figure 22: Schematic representation of the central STB board on our wire planes. While the trace layouts are schematic, the remainder of the board layout is our current planned design.

are removable and replaceable in case of failure. These boards are being designed by the JLab Fast Electronics Group. Additionally this group is designing the specifications for the electronics cooling system. Based on preliminary specifications, an initial design for a cooling system has been completed. The daughter boards and the chamber cooling system are discussed in more detail in Section 6.

4.1 Wire Tensions

Fig. 23 shows the sag at the center of each wire as a function of its length. Since the FDC geometry is circular, the center wires are the longest and the wire length decreases out to each edge. All sense wires will be strung with a tension of 20 gm and all field wires will be strung with a tension of 130 gm. This accounts for the mismatch of sag between the 20 μm diameter tungsten sense wires and the 80 μm diameter Cu-Be field wires. A tension of 20 gm puts the sense wire stress at about 40% of the yield strength. A tension of 130 gm puts the Be-Cu field wire stress at about 20% of the yield strength. The calculations here were done with the wires running horizontally where the effects of gravitation are the largest. The nominal design is to have the wires either running vertically, where there is no sag effect, or at $\pm 60^{\circ}$, where the sag effects are reduced.

At the current time we are strongly considering using 25 μm diameter sense wires instead of the 20 μm in our nominal design. This wire is significantly stronger and would reduce the probability of wire breakage. In addition this diameter wire is more readily available and as such, may have less issues associated with quality control [10]. The trade off is that the chamber will have to run at a higher voltages to achieve the same gain. In this configuration, the drift velocity will be larger than for the nominal configuration.

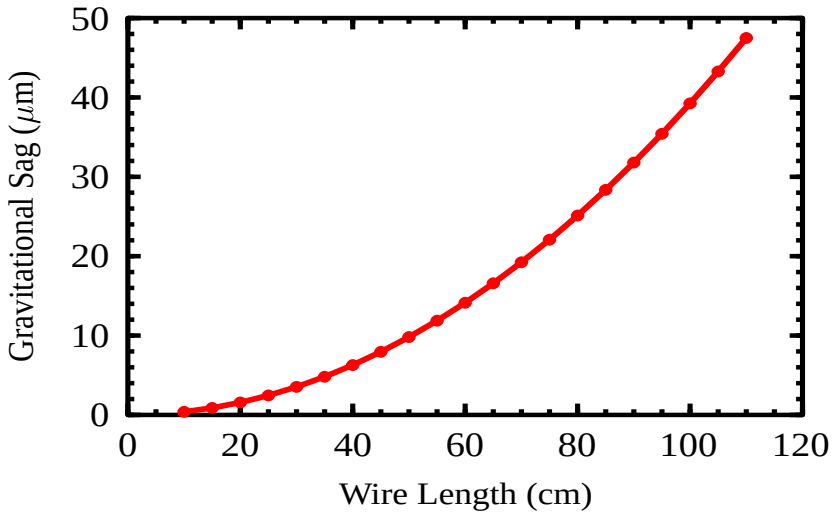

Figure 23: Plot showing the wire sag due to gravitation for wires running horizontally as a function of the wire length.

4.2 Wire Winding

Due to the lack of appropriate infrastructure for wire winding at JLab, we are in the process of developing an MOU with the wire chamber lab at Fermilab (FNAL). We visited FNAL in January 2007 for a full day meeting with Karen Kephart and discussed all aspects of the FDC design with her. We have a tentative agreement in place for FNAL to work with us to develop winding techniques that will meet our tolerance specification, beginning with the winding of several test planes this summer. At that point we will know if pretensioning of the wire planes is required and what winding jigs will be necessary. After these decisions are finalized, FNAL will go into a production mode of winding each of our wire planes.

After each plane is wound, FNAL will measure the tension of each wire and measure the position of each wire (measurements at each end). Any wires which are outside of our tolerance specifications will be replaced. FNAL will store the wound planes in environmentally controlled containers that we will provide until we are ready to get them for the construction phase.

5 Cathode Planes

The cathode planes are designed to see the image charge of the electron avalanche on the sense wires. In the plane perpendicular to the wires, the cathodes image the wire location. The strips also provide a precision coordinate in the direction along the wires. In the FDC chambers we have oriented the strips on either side of the wire plane at 90° relative to each other and at ±45° to the wire direction. Each cathode plane contains 192 strips with a pitch of 5 mm and a strip gap of 1 mm. The planes will include 1/7 oz of copper on a 25 μm (1 mil) Kapton backing. The strip pitch is chosen to match the chamber half gap to optimize the resolution (see discussion in Section 1.2). A schematic representation of a cathode board is shown in Fig. 24. Again the connectors shown accept the preamplifier daughter boards mentioned in Section 4.

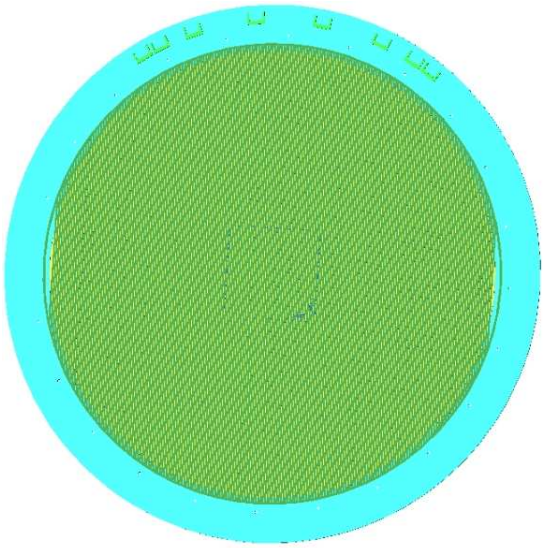

Figure 24: Schematic picture of a cathode plane. In this view the upper portion of the board contains the connectors for the preamplifier daughter boards.

The gain of the FDC chambers depends critically on the separation between the cathode planes and the wire plane (referred to as the "half-gap"). Our early cathode plane samples suffered from noticeable folds and wrinkles that lead to local variations in the half-gap and hence the gain. In our small-scale prototype we did not attempt to pretension the cathode planes before they were attached to their frames to remove the defects. Thus the resolution measurements reported in Section 7 should represent an upper limit from our design. We have been in contact with the circuit board manufacturers regarding the defects and they will able able to work with us to eliminate these problems.

Beyond local distortions in the cathode due to folds and wrinkles, there is another important distortion effect that must be considered in the design of the full-scale cathodes. When high voltage is applied to the wires, the grounded cathode planes are deflected toward the wires dues to electrostatic pressure as described in Ref. [11]. This distortion is largest at the center of the cathodes and uniformly decreases to zero at the perimeter. Kapton by itself offers little resistance to this deflection. In the small-scale prototype, given its small size,

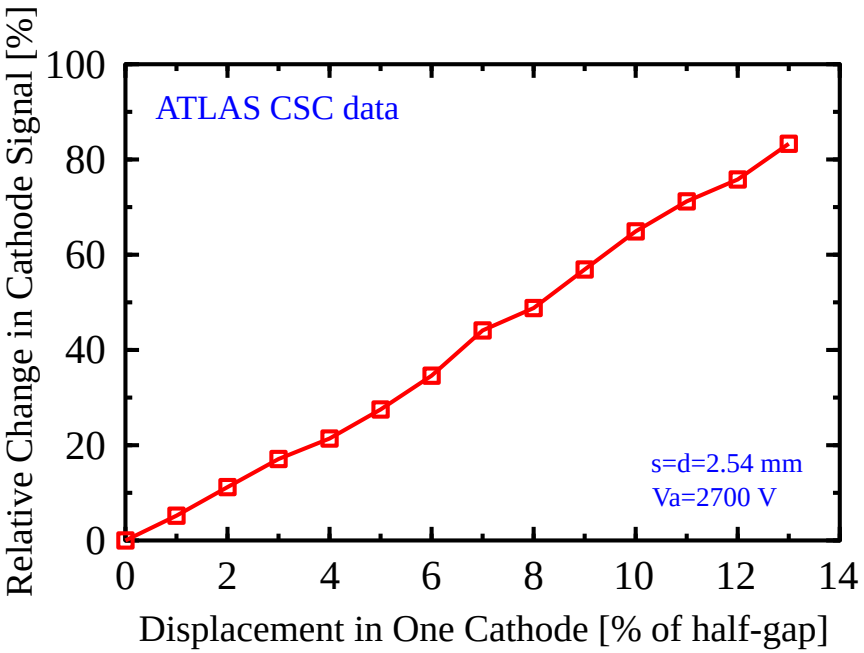

Figure 25: Cathode signal dependence on the half-gap from ATLAS CSC data. This figure is taken from Ref. [12].

this deflection does not present a serious problem. For the full-scale FDC system our design choice is to laminate the cathode board to a rigid Rohacell foam backing (although designs without a backing are also being explored). This will eliminate the electrostatic pressure issues for the cathodes.

The effect of decreasing the half-gap on the cathode signals was studied by the ATLAS group for a cathode strip chamber similar to our prototype. Fig. 25 shows the relative change of the cathode signals as a function of the change in the half-gap. Assuming these results can be generalized to our geometry, we have set a flatness goal of 100 μm ($\pm$50 μm), corresponding to a change in the cathode signals of $\pm$5%.

To illustrate the issue at hand, the gain $\mathcal{G}$ in a proportional counter is given by:

$$\mathcal{G} = Ke^{CV}. \tag{1}$$

For an operational voltage V, the gain is dependent on the capacitance of the detector C. Thus any variation on the flatness of the cathode plane changes the capacitance of the detector and hence the gain. It also creates field non-uniformities that affect the cathode position resolution. For gain variations of less than 10%, a rough calculation shows that the cathode plane must have less than a 100 μm flatness variation.

5.1 Cathode Plane Backing

In order to achieve the required flatness, each cathode plane will be constructed with a rigid 5-mm thick Rohacell foam backing sheet. Low density Rohacell foam (ρ=0.032 g/cm^3) has been chosen as the best compromise between cathode support and material thickness in the active region of the chamber. To enhance the rigidity of the chambers, neighboring cathode planes will be coupled together mechanically into a cathode "sandwich" design that includes

a isolation ground layer in the middle. A schematic picture of our cathode sandwich design is shown in Fig. 26.

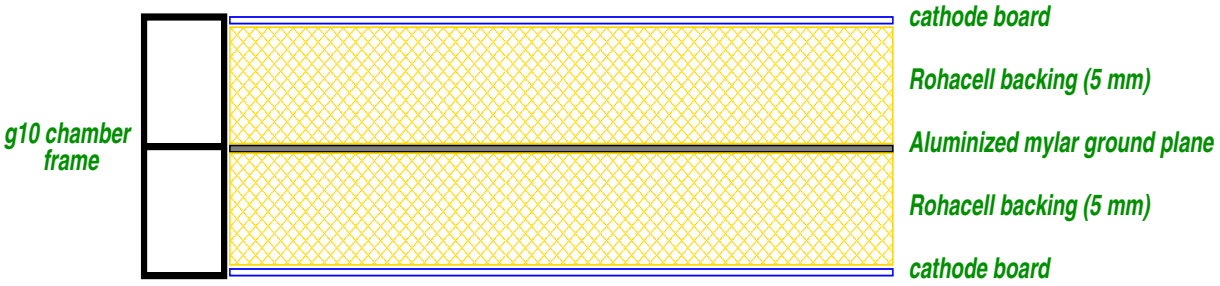

Figure 26: Schematic sketch of a side view of a cathode-sandwich that separates neighboring wire planes. Each cathode board is backed by a smooth sheet of Rohacell foam. Neighboring layers are isolated by a thin ground plane located in the middle of the sandwich.

5.2 Cathode Sandwich Assembly

The FDC cathode is a plane of copper strips printed on a 25 μm thick Kapton film stretched across an annular fiberglass ring with the center filled with Rohacell HF 31 rigid foam. In order to maintain the required "parallelness" to the anode wires, this plane must be extraordinarily flat. It must also be of as low mass as possible in the active area to minimize multiple scattering and energy loss.

The cathode is assembled on a granite surface plate to maximize flatness. Due to their large size, we have been unable to have the Kapton printed circuit boards (PCBs) made in one piece. At present, they are made in three separate pieces. The assembly sequence for a cathode sandwich is as follows:

1). A granite surface plate is cleaned with isopropyl alcohol.

2). The surface plate is wetted with a small amount of alcohol.

3). The center PCB is carefully floated on the alcohol to prevent wrinkles with the active face of the PCB down, against the surface plate.

4). The alcohol is gently rolled out from under the PCB toward the edges until the PCB wets the surface plate along the entire film using a semi-hard roller.

5). The two side PCBs are floated in the alcohol and gently brought in contact with the edge of the center PCB. The fiducial targets on the center and edge PCBs are aligned.

6). A low viscosity epoxy, Loctite Hysol RE2039 resin, is mixed at a 100:33 ratio with HD3561 hardener and is rolled onto the back (the exposed) surface of the Kapton PCB using a Teflon roller, using care not to lift the joint between center and edge PCBs. The glue layer should be as uniform as possible and approximately 25 μm thick.

7). The g10 fiberglass ring is positioned correctly on the three-piece PCBs.

8). A disk of Rohacell HF-31 is cut with a razor with an outer diameter that matches the inner diameter of the g10 ring. The Rohacell disk is placed inside the g10 ring.

9). A weight made from a thick aluminum tooling plate and of the same diameter as the g10 ring is placed on top of the g10 ring and Rohacell disk. This forces them into intimate contact with the epoxy on the back of the Kapton film. The epoxy is allowed to cure overnight.

10). The weight is lifted off the cathode sandwich. A thin bead of Scotchweld DP-190 structural adhesive is injected between the inner diameter of the g10 ring and the outer diameter of the Rohacell using a pipette filler. Any excess glue is removed with the edge of a single edge razor. This epoxy is allowed to cure overnight.

11). A sheet of 6.3 μm aluminized Mylar (MPI NRC-2-flat) is stretched on the FDC film stretcher. A thin bead of the same Hysol epoxy used above is run around the outer diameter of the stretched Mylar film. This epoxy is positioned to match the side of the g10 ring opposite the Kapton PCB. Another thin bead of epoxy is placed in a ring just outside the beam diameter (7 cm) to bond the Mylar to the back side of the Rohacell. The g10 ring must have holes in it to allow the air between the Rohacell and the Mylar film to escape when the two are placed together. The cathode sandwich is placed on the stretched Mylar and weighted with the tooling plate described above. The epoxy is allowed to cure overnight. The Mylar/cathode sandwich is cut from the film stretching tool.

12). A second cathode sandwich is glued to the Mylar on the back of the first sandwich using Hysol adhesive. The adhesive is spread in the area of the g10 ring and an additional thin ring just outside the 7 cm beam diameter area. This guarantees that the two halves of the cathode sandwich are structurally linked and support each other.

5.3 Cathode Flatness Measurements

So far we have constructed one complete full-scale cathode sandwich using blank Kapton sheets of the same dimensions as the cathode boards. We are awaiting delivery of realistic cathode boards and will repeat the procedure to understand the impact of the copper on the construction. In the process of making the first sandwich we were developing the details of the procedure as we went, and thus the flatness of the first sandwich represents our worst case scenario.

After construction of the sandwich we worked with the JLab Survey Group to measure the surface flatness using a Faro laser tracking system [13]. This device has a reported accuracy of 50 μm. The measurement technique involved placing a prism ball on the surface of the cathode layer and taking a laser measurement. The prism ball produced noticeable divots in the Rohacell that also affected the precision of the measurements. Our measurement plan involved taking 100 readings across the full surface of the cathode. These results are shown in Fig. 27. Already the results are very encouraging and have convinced us that we can easily meet the tolerance specification for the cathode surface flatness. Note that the use of the

contact laser tracking system was a stop-gap approach as we work to develop a non-contact measurement system for the production cathodes.

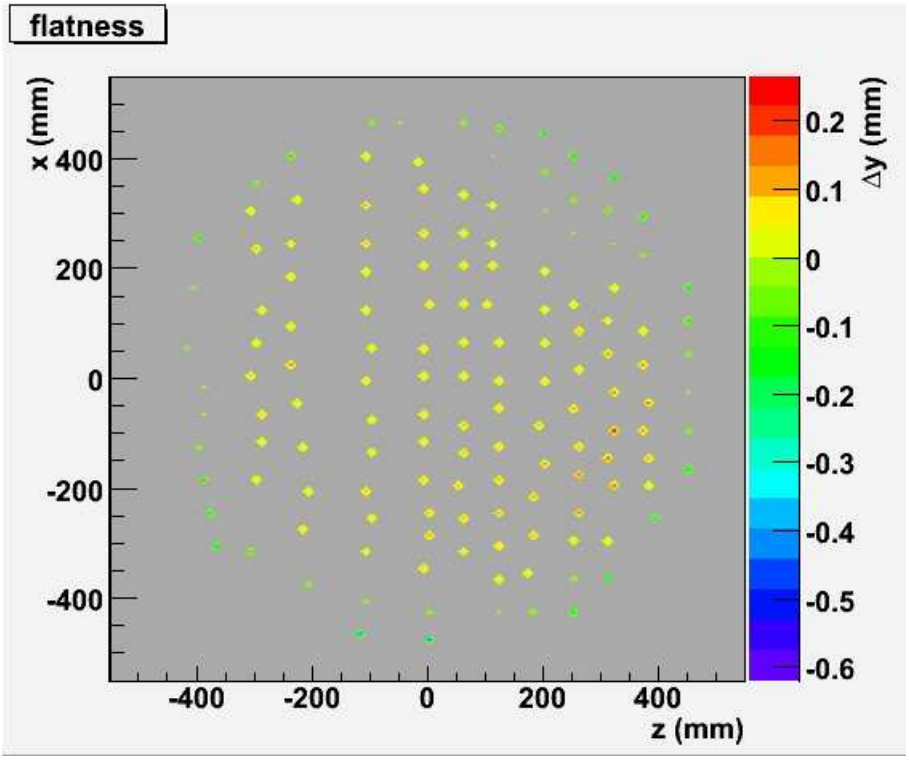

Figure 27: Results from the measurement of the flatness of our cathode sandwich prototype. The z scale gives the flatness in mm units. The problematic area along z=300 mm occurred due to an imperfection in the Kapton used. The problems apparent about the perimeter of the sandwich arose due to the fact that the g10 support frame and the Rohacell foam were not exactly the same thickness.

6 Readout

6.1 Overview

The FDC readout as presently planned will employ 125 ps F1 TDCs for the anode wire drift time readout and 100 MHz FADCs for the cathode readout. The 100 MHz flash ADCs that will be employed for the cathode readout have a sampling rate that corresponds to a 10 ns time bin. Time fitting algorithms matched to the chamber pulse shape can be employed to provide a time resolution of ∼2 to 3 ns (amounting to ∼20% of the time bin width). This timing information from the cathode signals would aid in pattern recognition of out-of-time tracks passing through the chamber volume. We are also exploring options with FADCs with slower clock rates. This could in principle reduce the electronics costs significantly if we can accept the poorer time resolution.

The readout of the full set of FDC detectors will require 2304 anode (sense wire) channels and 9216 cathode channels. The signals will be amplified at the detector using an 8-channel ASIC preamplifier/shaper chip based on the ASDBLR ASIC used to readout the ATLAS-TRT (see Fig. 28). The pulse shape will be chosen as a compromise between noise and pileup, both of which degrade the resolution. The electronics must also be designed to minimize cross-talk, particularly to non-adjacent channels.

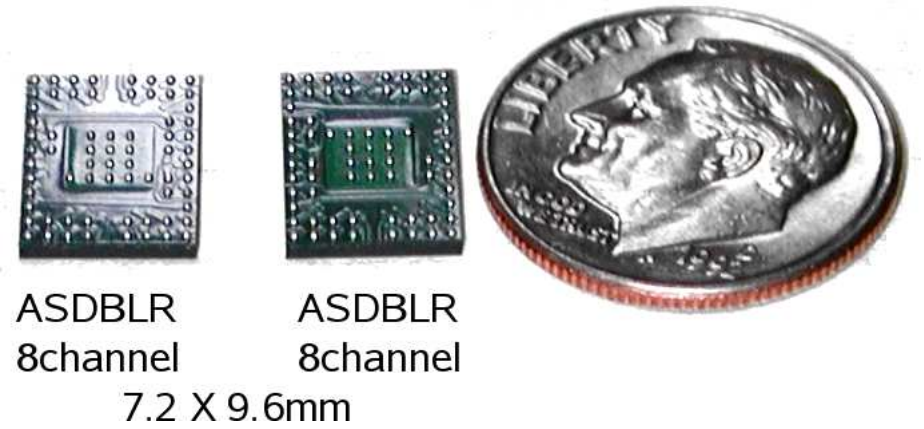

Figure 28: Photographs of two ASDBLR ASICs used in the ATLAS-TRT detector.

The primary design issue for the front-end electronics for the FDC system is to maintain a signal-to-noise ratio of better than 100:1 in the presence of a large detector capacitance. Capacitance measurements in detectors are very important because they serve to determine the performance of the detector in terms of the charges induced on the cathodes, gain variations, detector efficiency, etc. They also play an important role in determining the characteristics of the readout electronics. For the FDC chambers the dominant contribution to the capacitance seen by the preamplifiers will be the strip-to-strip capacitance. The capacitance between adjacent strips is given approximately by [14]:

$$C(pF/cm) = 0.12t/w + 0.09(1+k)log_{10}(1 + 2w/s + w^2/s^2), \quad (2)$$

where t is the strip thickness, w is the strip width, s is the strip separation, and k is the dielectric constant of the backing material (here it is envisioned to be Kapton). For the

FDC design that is presently considered, this capacitance is roughly 1 pF/cm. Accounting for the total capacitance of the system then forms a basic requirement for the input capacitance for the front-end electronics performance. An additional concern for this design is the coupling of the signals between adjacent strips. Studies of the PHENIX CSCs have shown that appropriate setting of the integration times of the electronics is important to decrease sensitivity to distortions in the induced charge distribution due to inter-strip coupling.

6.2 ASIC Development

The design of the GlueX ASIC is presently well underway and the first run of 50 ASICs should be delivered for testing by early summer 2007. The basic functional blocks of this device are shown in Fig. 29. The input protection circuitry protects the chips from discharge spikes. The preamplifier circuitry amplifies the signals from the FDC with minimal signal shaping. In the shaper portion, the ion tail is shortened by pole-zero filtering which improves the operation at higher rates. Finally the output driver allows for the signals to be sent over the 100 ft cables to the readout electronics with minimal distortions.

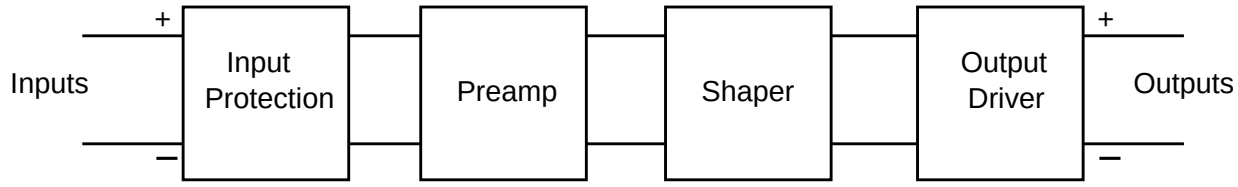

Figure 29: Schematic block diagram of the functional blocks of the ASIC preamplifier.

The preamplifiers are being designed to match the dynamic range for the FDC. The total signal charge from the FDC anodes will be in the range from 300 fC to 3 pC and that for the FDC cathodes is in the range from 10 fC to 1 pC. The ASIC has a high degree of linearity (to a few percent) over the full dynamic range. Fig. 30 provides the current specifications for the GlueX ASICs. The design of this component is being handled by Mitch Newcomer (UPenn) who was responsible for the design of the ATLAS ASIC.

The current ASIC design has a gain of 2 mV/fC. We are presently discussing if we want to consider different gain specifications for the ASICs on the anodes and cathodes (e.g. 2 mV/fC for the anodes and 10 mV/fC for the cathodes). This additional gain for the cathode could also be dealt with by an amplifier in the FADC itself. Later this year we will begin to work on the development of adding discriminators to the ASICS that readout the anode wires. Note that additional shaping of the signals will be done on the FADCs. This will be necessary to improve the tail cancellation, spread out the leading edge of the pulse for improved timing resolution, and to allow for compatibility with the input to the FADC.

6.3 Preamplifier Daughter Boards

The preamplifier chips will be mounted to a separate daughter board to enable easy access and replacement in case of component failure or poor performance. Due to the tight space constraints, the boards must be carefully laid out. The preamplifier daughter board is being designed by the JLab Fast Electronics Group and a schematic diagram is shown in Fig. 31.

Channels		8
Inputs	Type	Dual (+ and -)
	Impedance	80 Ohm
	Protection	Diode Protected
	C Range	10-100pF
Shaping	Peaking Time	11nS @ 10pF Cin Unipolar – [CR-RC^3]
Outputs	Type	Differential, Offset Bias
	Range	0-1000 mVp-p (-425mV to +575mV
Gain		2mV/fC
	Range	0-400 fC Impulse or Point Ionization
Noise	ENC	2500 e + 50 e/pF
Power Supply		+2.5V
Power		320 mW (40mW/Channel)
Process		0.25 µm CMOS TSMC
Die Size		2.4mm x 3.2mm
Packaging		QFN64 10x10 mm

Figure 30: Specifications for the GlueX ASICs.

This board is for our cathode readout and includes three 8-channel ASIC chips (two on the front, one on the back).

The daughter boards include the associated voltage regulator circuitry and calibration circuit. Our current plans are to employ the last connector pair on the readout cable to allow the distribution of a controlled charge pulse to each amplifier channel for calibration purposes. The design of this aspect of the daughter boards (and pulser distribution system in the FADCs and TDCs) is still in progress.

6.4 Chamber Cooling

The current design of the ASIC chip dissipates 40 mW/channel. In the tight space confines of the FDC chamber, cooling of these chips is essential. For the nearly 500 preamplifier cards in the system, the total power dissipated is nearly 600 W. Our present design for the chamber cooling system relies on heat conduction from the daughter boards to the FDC cooling system. The design is shown in Fig. 32, where the card is in thermal contact with a large surface area radiator (an aluminum mesh ring extending between each FDC chamber package). The radiator will be cooled either with forced air or, more likely, water. Heat load calculations and thermal simulations are in progress. The final system will likely include forced dry air no matter what decision is made as this air supply will reduce the humidity level in the FDC chamber environment and lead to lower leakage currents on the electronics. Note also that our thermal calculations show that temperature variations of $\pm 35^\circ$ increases the stresses on the wires by only about 10%.

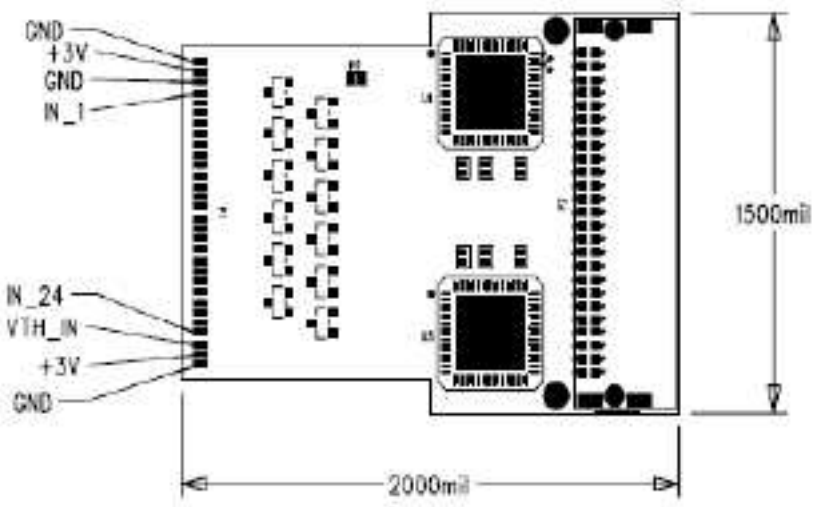

Figure 31: Schematic diagram of the cathode preamplifier daughter board.

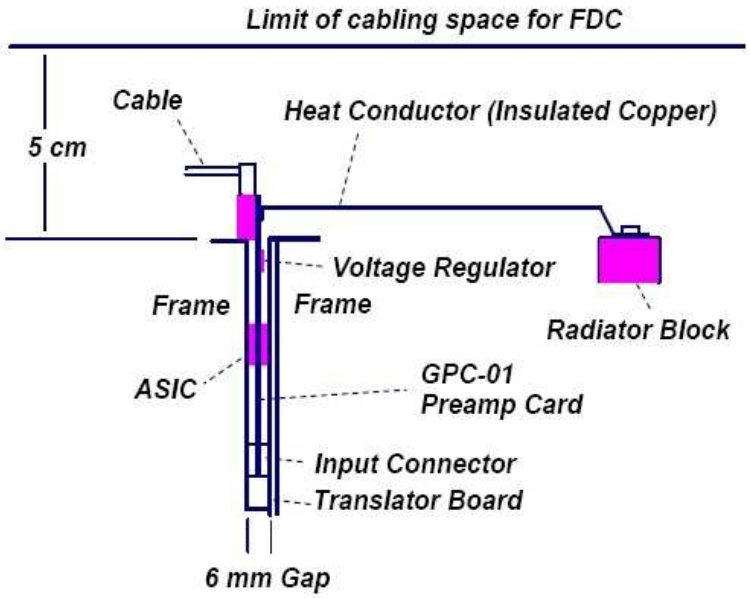

Figure 32: Schematic diagram of the FDC electronics cooling system.

6.5 Power Supplies and Cabling

The layout of the high voltage and low voltage systems for the FDC chambers have followed the current design employed for the CLAS drift chambers. The HV system will be sufficient to allow for reasonable granularity for the distribution to limit currents and to ensure that chamber HV disconnects affect as small a portion of the system as possible. The LV system is being designed to protect the chambers from overvoltage and overcurrent problems through the use of a distributed fuse system. This system will include fusing down to the level of 0.5 to 1.0 A. The HV and LV systems will be monitored continuously in the counting house and alarms will notify operators of any problems with the systems.

We are currently making decisions on the signal and HV cables that will be used for the FDC system. For the HV cables, we plan on employing the same HV cables that are currently in use for the CLAS drift chambers in Hall B. These cables consist of a PVC-jacketed "mother" cable with contains 12 "baby" cables. Each baby cable is wrapped in tefzel insulation and is rated for 5 kV. Our current plans are to allow for 6 positive HV and 6 negative HV lines per wire plane. Thus each FDC package will be serviced with 6 HV mother cables. This defines the HV granularity of the system. For the signal cables we will be using low-profile round-jacket shielded flat cables. There are a number of distributors that we are in contact with.

A schematic overview drawing of the cabling layout for a single FDC layer is given in Fig. 33. The present design includes 8 signal cables (25 pair cables) for the cathode readout and 4 signal cables for the anode readout. The signal cables will be roughly 100 ft long in order to reach the readout electronics. In addition, the cabling layout will have to enable the FDC system to be cabled up outside of the solenoid and then to be inserted into position. We are currently working on the design of the FDC cable layout. This design is initially focusing on the required cable-packing scheme that will allow all cables to fit in the 5-cm annulus surrounding the FDC system. After this work is completed, the design will then begin to focus on the required scheme for cable support and stringing to the electronics.

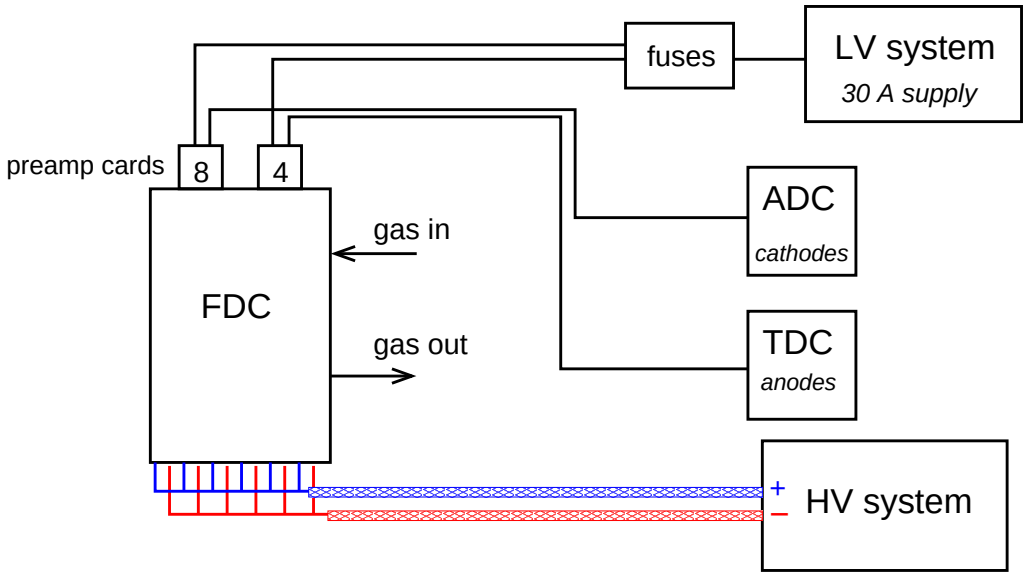

Figure 33: Schematic overview of the cable layout for each FDC chamber layer.

7 Small-Scale FDC Prototype Chamber

A small-scale prototype cathode chamber has been designed and constructed to optimize and design the FDC chambers. The prototype chamber has also provided us with general experience with cathode strip chambers. Through detailed study of this prototype we have been able to make design decisions on which electrode structure and layout will fulfill the design requirements for the final FDC chambers. The prototype has also provided important insights into the mechanical design, tolerances, construction and assembly techniques, noise immunity, and calibrations that will be important for the final FDC detector design. Some of the elements of the FDC prototype design have descended from the cathode chambers employed in the original LASS spectrometer [15]. Details on the FDC prototype studies and design work is contained on the FDC web page [16].

A schematic of the FDC prototype chamber is shown in an exploded view in Fig. 34. The basic chamber layout consists of two cathode planes with strips oriented at $\pm 45^\circ$ sandwiching a single wire plane. The gas volume is defined by two outer aluminum frames that each include an aluminized mylar window. The active area of the prototype chamber is roughly 20 cm $\times$ 20 cm, and the chamber is about 8 cm thick.

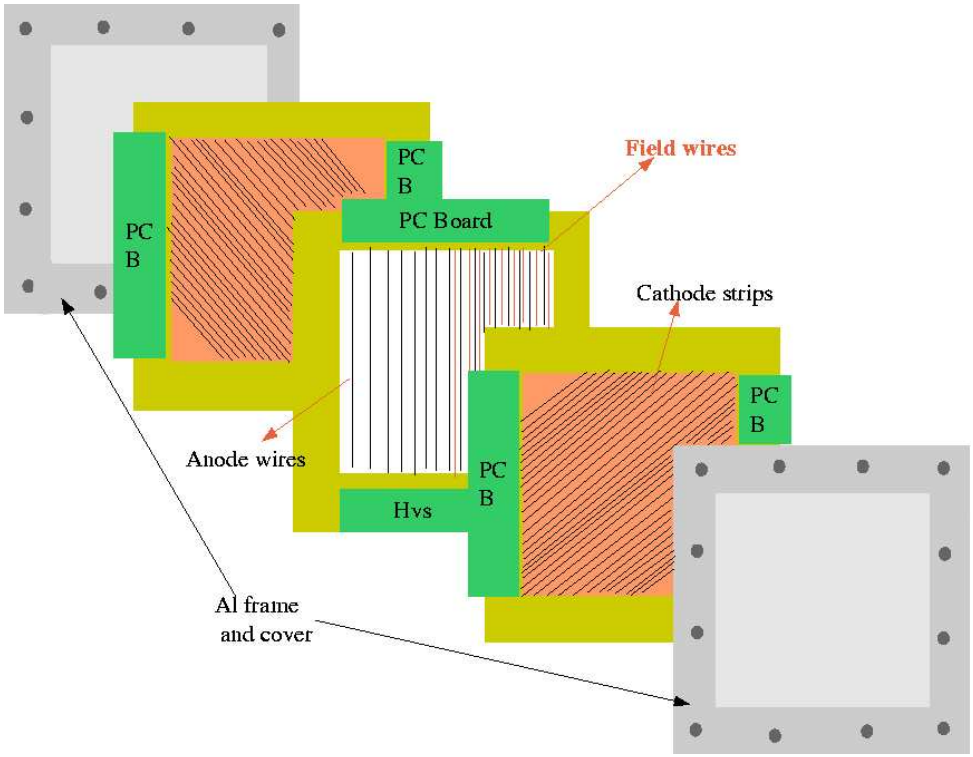

Figure 34: Schematic representation of the FDC prototype chamber in an exploded view showing the wire plane, two cathode planes, and the two aluminum window frames.

The test chamber has been designed to act as a test bed for any number of electrode configurations. So far we have tested wire planes consisting only of anode wires and planes consisting of alternating anode and field-shaping wires. We have also designed cathode planes of varying rotation angle and varying cathode strip separations. Each configuration

has been studied in order to come to an understanding of the optimal electrode structure for our purposes.

The U and V cathode planes are mirror symmetric with respect to each other. The cathode planes are copper-clad Kapton sheets ($\sim$2 mil thickness) mounted onto 5-mm thick g10 frames. The chamber is designed to operate with the anode wires at positive high voltage, the field wires at negative high voltage, and the cathode strips at ground. Small signal routing circuit boards attach to the output connectors on the wire and cathode circuit boards, and contain the preamplifiers for each readout channel. The output connects to a shielded twisted-pair line that routes the signals to the readout electronics. The signal readout boards used for the cathode readout are different than those for the wire readout in order to account for the polarity difference in these signals.

Each readout channel has its own associated "SIP" preamplifier. These single-channel transimpedance preamplifiers were originally designed for the Hall B CLAS detector. They have complementary outputs designed to amplify signals by a factor of 2.25 mV/μA. Besides high gain, characteristics of the SIPs include: fast rise and fall times (3 to 4 ns), wide frequency bandwidth, wide dynamic range, and low noise and power dissipation (65 mW). The power requirement for a single SIP is 5 VDC at 13 mA, and is supplied by a low-voltage power supply.

In total the chamber includes 16 sense wires, separated by 1 cm. The cathode planes are located 5 mm away from the wire plane. They each include 32 copper strips with a pitch of 5 mm. Three different sets of U and V cathode planes have been designed with strip separations of 0.25 mm, 0.50 mm, and 0.75 mm to allow for the optimal configuration to be determined. Studies from the prototype chamber indicate no differences in cathode resolution or noise levels among the different configurations. Our nominal strip gap choice is 1 mm. Presently the chamber is operating with a 90% argon - 10% CO_2 gas mixture. Photographs of the prototype cathode chamber and the cathode plane itself are shown in Fig. 35.

This prototype chamber has been in operation for three years. A photograph of the test setup is shown in Fig. 36. This setup includes external chambers to define an incident charged particle track through the prototype FDC chamber. These external chambers provide two x and two y coordinates above the FDC chamber and another pair of each coordinate below. A scintillator hodoscope has been set up above and below the test chamber to define the incident angle of the tracks. This hodoscope has not been employed to this point and triggering is accomplished using a small set of scintillators placed above and below the prototype that limit the incident rays to near-normal angles ($\theta < 10^{\circ}$).

7.1 Chamber Resolution Studies

In this section we present an overview of the results from our studies with the small-scale FDC prototype chamber. To date our studies have not employed tracks defined by the external cosmic ray chambers in our test set up. We have instead relied on the fact that our U and V strip orientation provides an image of the wire location in one dimension. This image should be a δ-function if our resolution was infinitely good. We are quantifying our cathode position resolution as the width of the reconstructed coordinate in the plane perpendicular to the wires.

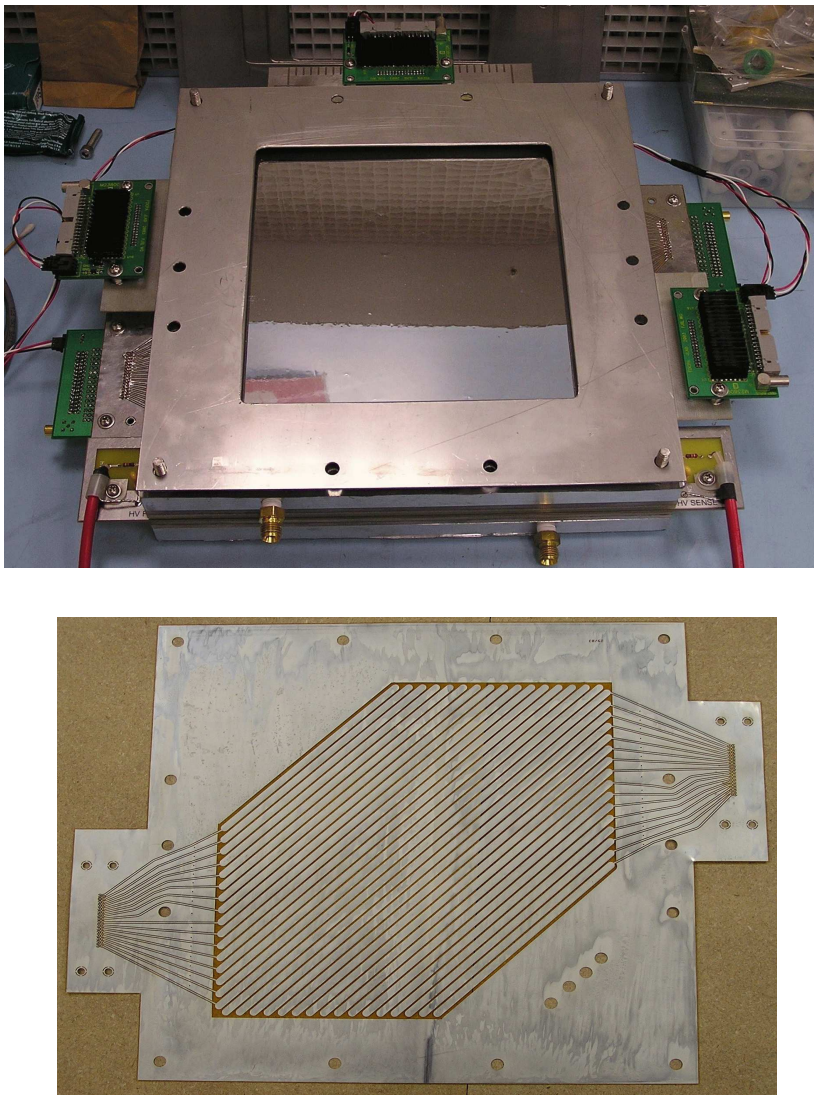

Figure 35: (Top) Photograph of the prototype FDC cathode chamber constructed to optimize the chamber structures. (Bottom) Photograph of a cathode plane showing the cathode strips.

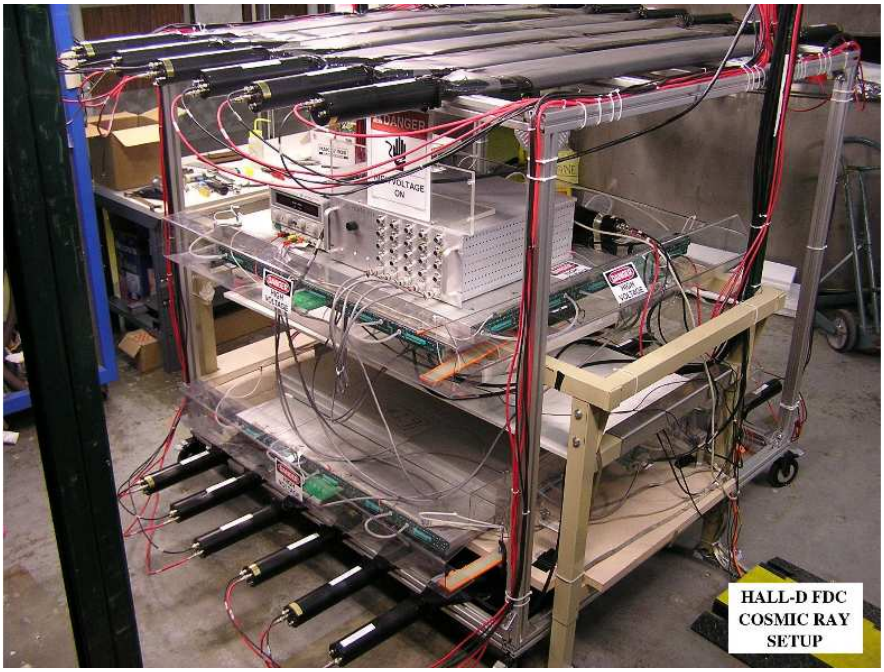

Figure 36: Photograph of the cosmic ray test stand set up at JLab to study resolution characteristics of the FDC cathode strip chambers.

The extraction of the cathode position relies on using a semi-empirical form of Mathieson [17] to determine the distribution of the induced charge on the cathode planes. This form for the charge distribution across the strips $\rho(\lambda)$ is given by:

$$\frac{\rho(\lambda)}{q_a} = k_1 \left(\frac{1 - \tanh^2(k_2\lambda)}{1 + k_3 \tanh^2(k_2\lambda)} \right), \tag{3}$$

where,

$$k_2 = \frac{\pi}{2}\left(1 - \frac{\sqrt{k_3}}{2}\right) \quad \text{and} \quad k_1 = \frac{k_2\sqrt{k_3}}{4\tan^{-1}\sqrt{k_3}}. \tag{4}$$

Here $\lambda = u/h$, u is the coordinate transverse to the strips relative to the center of the distribution, h is the anode-cathode gap, and q_a is the net anode charge. This functional form depends on only one parameter (k_3). A typical fit to our data, using the Newton-Raphson method [18], is shown in Fig. 37. As seen here, it is the case that most of the charge in an event is distributed over 3-5 cathode strips. Therefore the resolution depends on the number of strips used. Monte Carlo simulations and operational experience from different groups have shown that the optimum number lies between three and five strips. The position resolution is poor when only one or two strips are present as there is not enough information, while it increases slowly when more than five strips are used. The resolution function in this case also includes the additional electronic noise from each strip. Here there must be an optimization of chamber resolution factoring in the desire to minimize the number of readout channels to contain costs.

The first wire configuration we studied was wound with just the sense wires. The best results were obtained at an operating voltage of +1750 V on the wires and the cathodes at

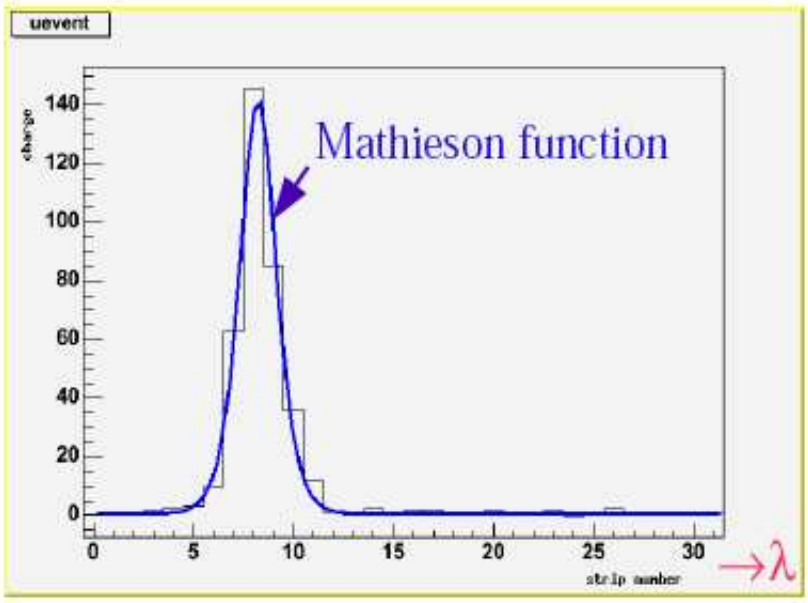

Figure 37: Sample prototype charge data showing the form of the Mathieson fit function as a function of the strip coordinate.

ground. Fig. 38 shows the measurements of the cathode resolution for the chamber in this configuration. The wires that were imaged in this distribution correspond to where we had overlap of the U and V cathode strips and the trigger scintillators. The average cathode coordinate resolution in this configuration was measured to be 179.6±3.9 μm.

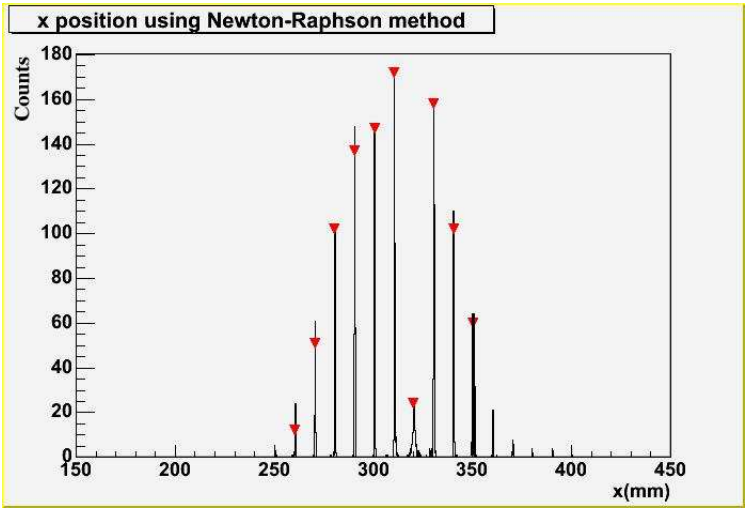

Figure 38: Wire positions computed from the cathode strip centroids for the sense-wire-only configuration (V_s=1750 V).

The second wire configuration included both sense and field wires and corresponds to our nominal cell configuration. Fig. 39 shows the relative wire plane efficiency (plateau curve) in a 90% argon - 10% CO_2 gas environment as a function of the voltage applied to the sense wires, with the field wires at zero potential. The efficiency is defined to be the ratio of the number of events that have one peak in each cathode view matched to a sense wire relative to the number of triggers. A narrow plateau occurs above about 1600 V. The setting we used for normal operation was 1650 V. Fig. 39 shows the anode charge (deduced from the cathode

strip data) as a function of the sense wire high voltage. The trend is well-characterized by Sauli's gain function (eq.31 in Ref. [19]).

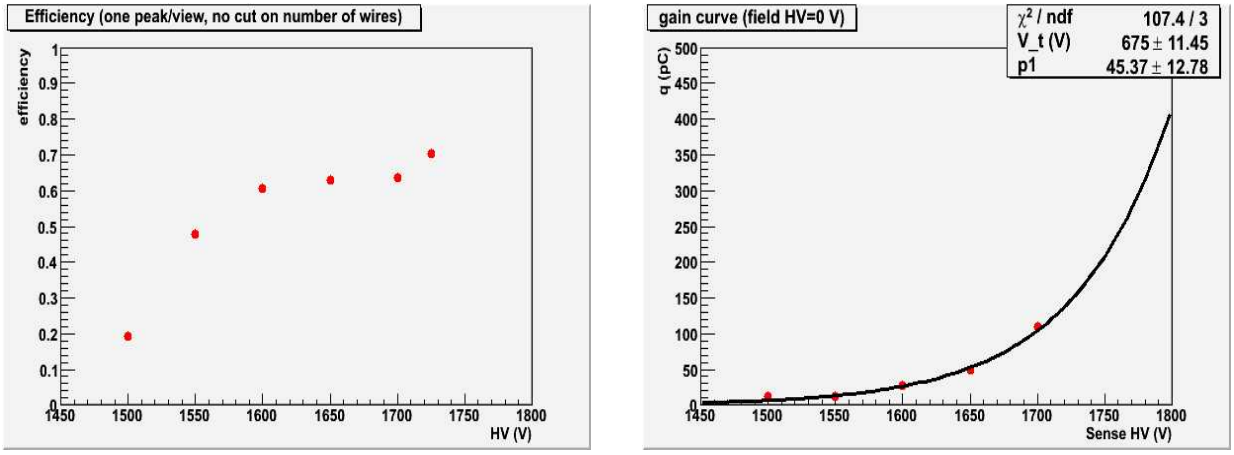

Figure 39: (Left) Plateau curve for the prototype chamber with both sense and field wires, showing the relative efficiency as a function of sense wire high voltage with the field wires at ground potential. (Right) Chamber gain as a function of sense wire voltage with the field wires at zero potential.

Fig. 40 illustrates that the long-time edge of the drift time distribution is poorly defined when the field wires are absent but the distribution becomes sharper when the field wires are present, especially when the magnitude of the voltage on the field wires is increased.

Fig. 41 demonstrates that the position resolution improves with increasing sense wire voltage (and hence gain). It is not feasible to run the chamber with the sense wires at 1700 V because the wires start drawing too much current. However, with the sense wires set at 1650 V, the good resolution obtained at 1700 V can be recovered by increasing the magnitude of the voltage on the field wires, as demonstrated in Fig. 41.

A plot of the wire positions reconstructed from the cathode data when the sense wires are at +1650 V and the field wires are at -300 V is shown in Fig. 42. This configuration corresponds to our nominal settings and corresponds to a gas gain of about 8×10^4. The average coordinate position resolution under these conditions was 158.2±3.1 μm. This agrees with the typical resolution of 182.6 μm obtained with the sense wire only configuration [20]. This is an important comparison and gives clear evidence that our cathode chamber performance is not degraded by the inclusion of the field-shaping wires. These resolution studies are for normally incident tracks and with zero magnetic field are quite encouraging. Additional results of these studies can also be found in Refs. [21, 22].

The cathode resolution as a function of x and y is shown in Fig. 43. Even with the relatively poor statistics in this study (acquired in a week–long run with incident cosmic ray muons), there is no indication of any strong dependence of cathode resolution on strip length. More detailed studies of the small-scale prototype are underway to better quantify the cathode resolution as a function of cathode strip length. In the full-scale chamber, the lengths of the cathode strips will vary from ∼10 cm to 1.2 m. The variation of the chamber resolution with strip length must be minimized.

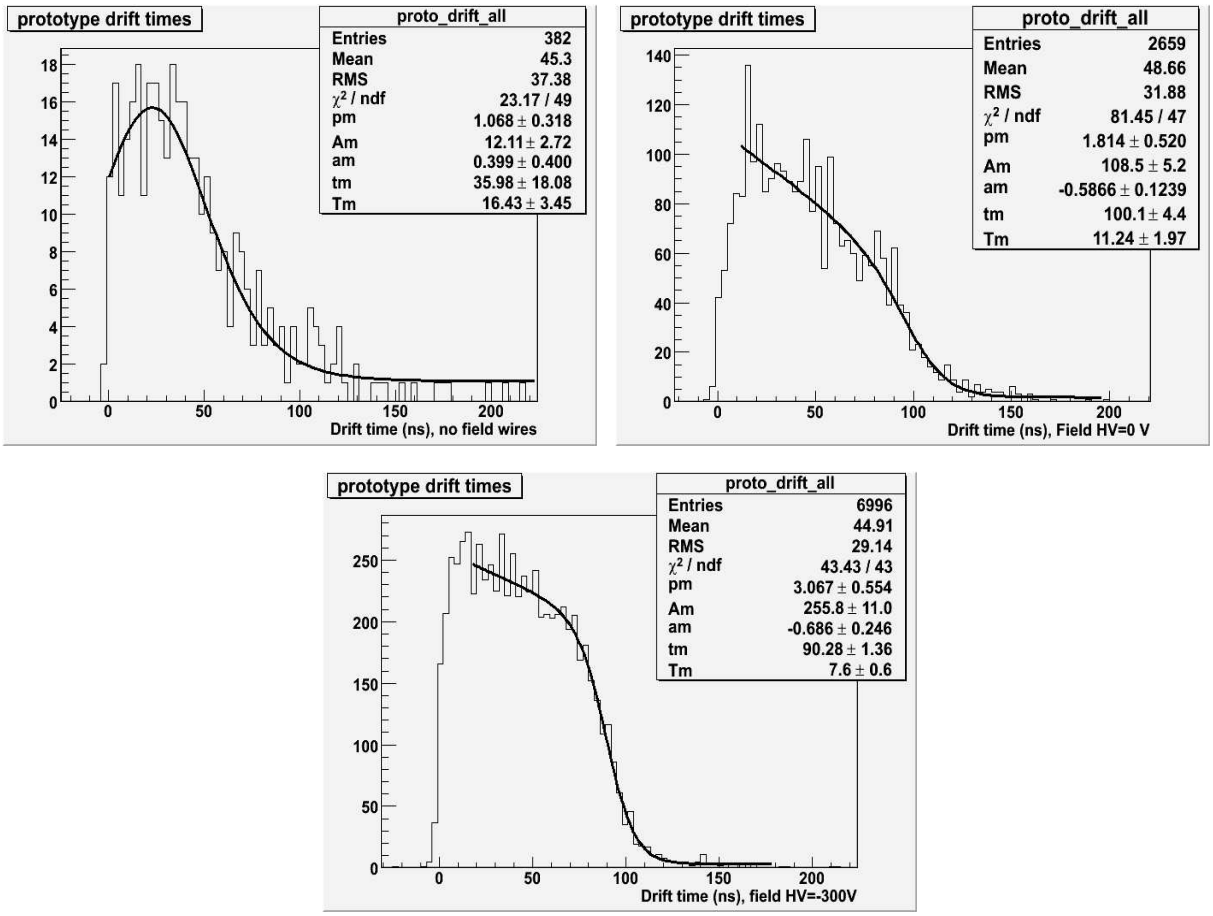

Figure 40: FDC prototype drift distributions for the sense wire only plane with the sense wires at +1750 V (top left), the field+sense wire plane with the field wires at zero potential and the sense wires at 1650 V, (top right), and the field+sense wire plane with the field wires at -300 V and the sense wires at 1650 V (bottom).

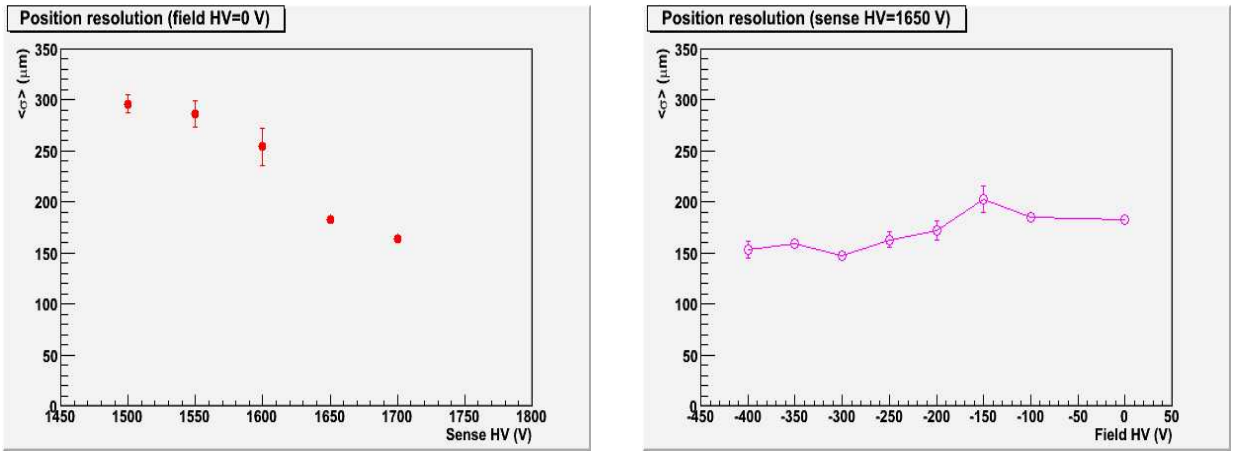

Figure 41: (Left) Position resolution as a function of sense wire voltage with the field wires at zero potential. (Right) Position resolution as a function of field wire voltage with the sense wires at 1650 V.

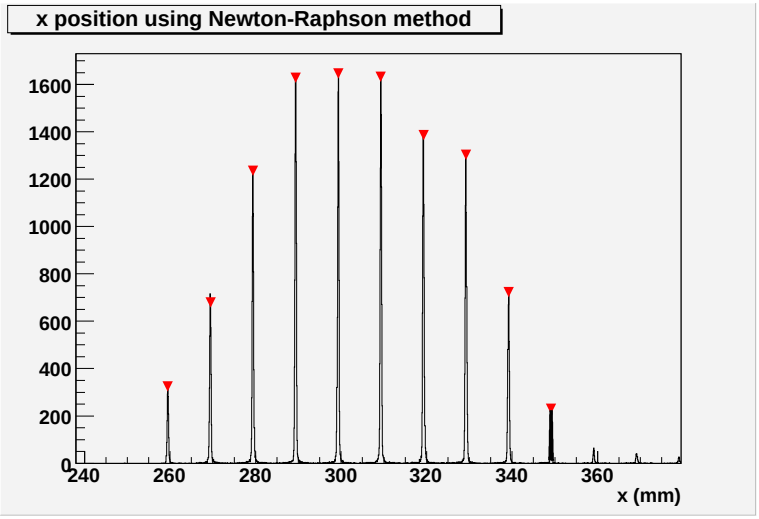

Figure 42: Wire position from cathode data for sense HV=1650 V, field HV=-300 V. The average cathode coordinate resolution from these data is 158.2±3.1 μm.

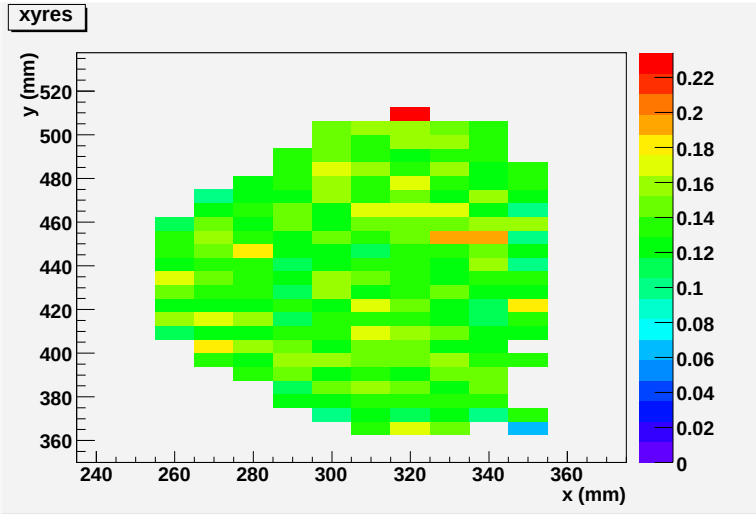

Figure 43: Position resolution as function of position for sense HV=1650 V, field HV=-300 V.

7.2 Gain Calibration

Because the cathode measurement relies on computing centroids based on signals on a few adjacent strips, good strip-to-strip gain calibration is essential. We perform special gain-calibration runs by injecting known amounts of charge into the test input of the preamplifier boards. The test input fires every channel at the same time, and we assume that the test pulse input is perfectly matched for all channels. The data are analyzed with the same code as for the regular trigger. A third-order polynomial is fit to the series of calibration peaks for each channel. As shown in Fig. 44, the gain variations from channel-to-channel for uncalibrated data are on the order of ±10-15%. After the calibration, the position resolution improves significantly (from ∼320 μm to ∼180 μm for this sample run).

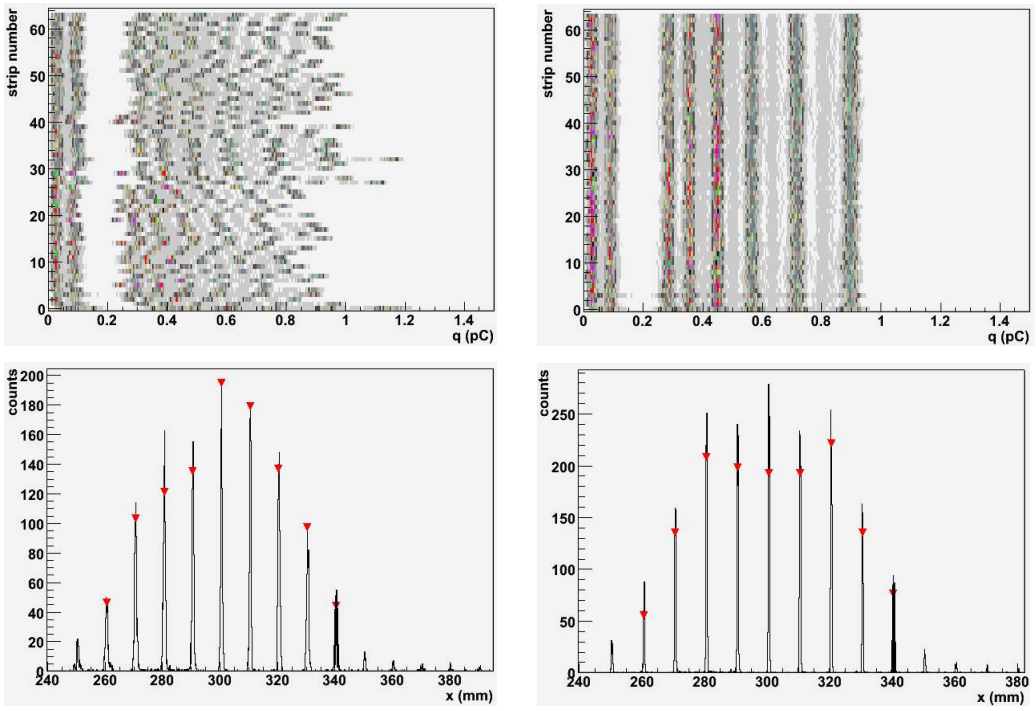

Figure 44: Effect of strip-to-strip gain calibration. The top left histogram shows peaks from the pulser data for each strip in the prototype before any gain calibration is applied; the top right histogram is after the calibration is applied. The bottom plots show the reconstructed wire positions before (left) and after (right) the calibration is applied; a marked improvement in the resolution is apparent after the calibration.

7.3 FADC Timing Resolution

In the final detector the FDC cathodes will be read out with FADCs. In order to suppress accidentals we need to extract the time from the sampled data. We read out a set of adjacent strips in the small-scale prototype with a commercial FADC unit from Struck running at a sampling rate of 100 MHz. Since the rise time of the pulses is on the order of 20 ns, there are typically only 2 or 3 samples on the rising edge, as illustrated in Fig. 45.

To find the drift time we used a linear extrapolation to the intersection with the base line. We used the strip with the most charge in the group of strips in the event. We compared

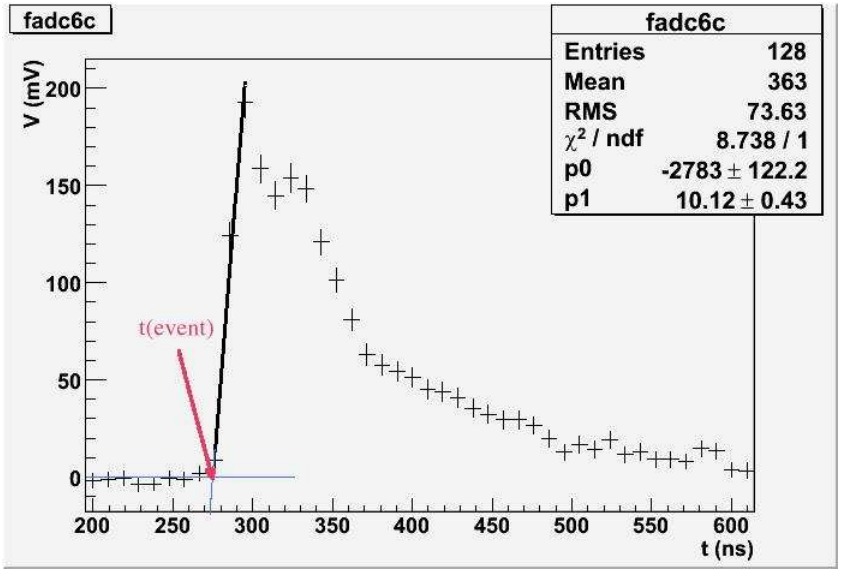

Figure 45: Sample cathode signal as measured by the Struck 100 MHz Flash ADC. The linear extrapolation to the base-line is superimposed.

this drift time with the time on the wire that caused the avalanche. The wire signal was discriminated with a CAMAC leading-edge discriminator and digitized with an F1 TDC. The time difference between the TDC measurement on the wire and the FADC measurement on the strip is shown in Fig. 46. The resolution in the difference is about 4.5 ns, which would be sufficient for suppressing out-of-time accidentals but not good enough to determine the coordinate of a track away from the wire. With more sophisticated pulse-shape models the resolution can be marginally improved[20]. The design specification for timing resolution from the cathodes is 5 ns.

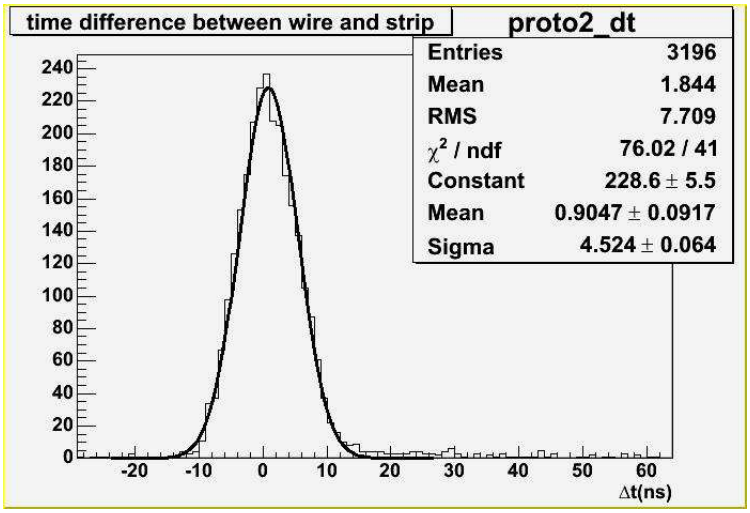

Figure 46: Time difference between the strip with the maximum charge and the anode wire whose avalanche produces the image charge seen by the strips. This result is for the sense-wire-only configuration with V_s=1750 V.

7.3.1 Pulse Shaping

In order to make any significant advances in improving the accuracy of the timing measurement from the FADC, the leading edge needs to be slowed down (shaped) with respect to the sampling clock rate. For the FDC system this pulse shaping will be accomplished in both the ASIC preamplifiers as well as the FADC units themselves. At the current time we are optimizing the shaping characteristics of the prototype chamber pulses (i.e. peaking time and tail cancellation) using a shaper board that was designed by Gerard Visser from IUCF. This board is shown in Fig. 47. Note that the improvement in the timing resolution of the signals is really not necessary for the FDC system, however the GlueX Central Drift Chamber (CDC) will be using the same ASIC preamplifiers and FADC boards and the timing resolution required for this system is 2 to 3 ns. The shaper board was delivered for testing with the small-scale prototype in late January 2007 and studies are currently underway.

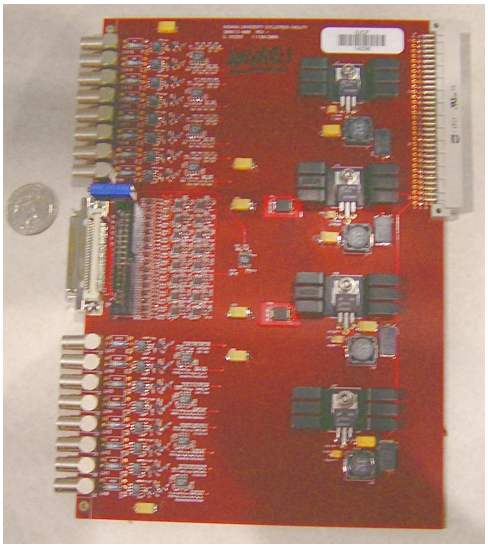

Figure 47: Photograph of the VME shaper board developed for the FDC readout to improve the timing resolution.

A sample shaped pulse is shown in Fig. 48. The blue curve is the result of a fit using the following functional form:

$$V(t) = V_b + (V_{max} - V_b)\left(\frac{t - t_0}{p\tau}\right)^p e^{p-(t-t_0)/\tau}, \tag{5}$$

where V_b is a background term (assumed flat), V_{max} is the peak height, t_0 is the time of the first electron, and p and τ are determined by the shaper circuitry.

7.4 Drift Time Resolution

Studies of the drift time resolution are now underway. However this aspect of the chamber performance is not expected to pose any serious issues due to the straightforward nature

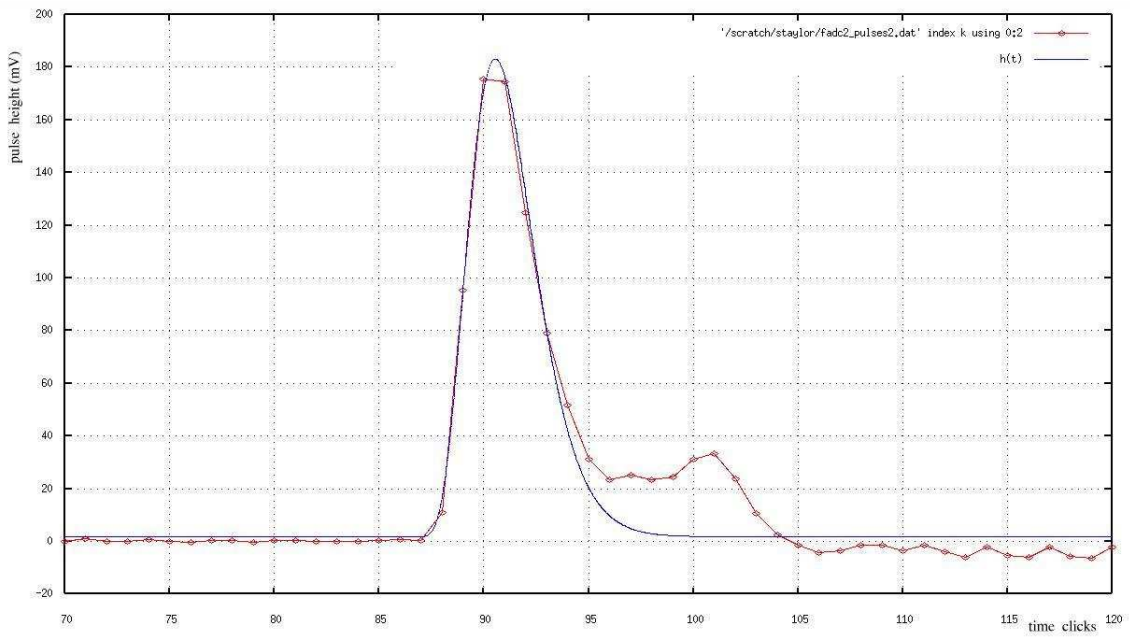

Figure 48: Sample pulse after the amplifier-shaper module. The red points are the flash-ADC data. The result of a fit using a model for the pulse shape is superimposed.

of the design. Fig. 49 shows a typical drift time distribution measured with the small-scale prototype using the F1 TDC. To measure the position resolution from the wire plane measurements, we have performed crude calibrations for our external cosmic ray tracking chambers to define a cosmic ray track through the FDC chamber. The position resolution is currently limited by our crude time-to-distance calibration for the external tracking chambers (see Fig. 50). Currently comparisons of the coordinate measured by the external tracking chambers to that measured from the FDC prototype from the wire plane show a position resolution of about 1 mm. Clearly this is not a true representation of the FDC resolution. Work is currently underway to optimize the calibrations.

7.5 Resolution Limitations

Groups at PHENIX, ATLAS, CMS (and others) have constructed cathode chambers with a similar cell size to that planned for the FDC chambers. Each of these groups has been able to achieve coordinate resolutions closer to 100 μm (see e.g. [14, 23, 28]) in bench test studies. Our resolution is currently limited to roughly 160 to 180 μm for at least four reasons:

1). Our choice of a $\pm 45^\circ$ rotation angle for the prototype (which was motivated in Section 1.2) leads to a worsened resolution. Using the information from both cathode planes in this configuration is equivalent to a measurement using one plane at 90° with respect to the wire. Thus, we could potentially gain an improvement factor if we placed one of our cathode planes such that its strips were perpendicular to the wires. In order to retain the self-calibrating aspect of the chamber, we would still want to have crossing strips, but better resolution may be obtained by making the relative stereo angle of the strips much shallower. A design incorporating a stereo angle will be important to improve pattern recognition (assigning the cathode hits to the associated wires in a multi-track environment). The limit on the

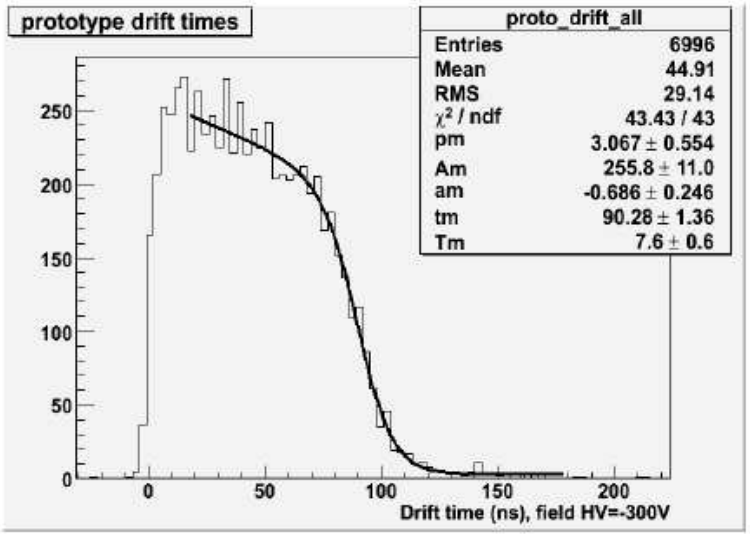

Figure 49: Drift time distribution measured in the small-scale FDC prototype read out with an F1 TDC.

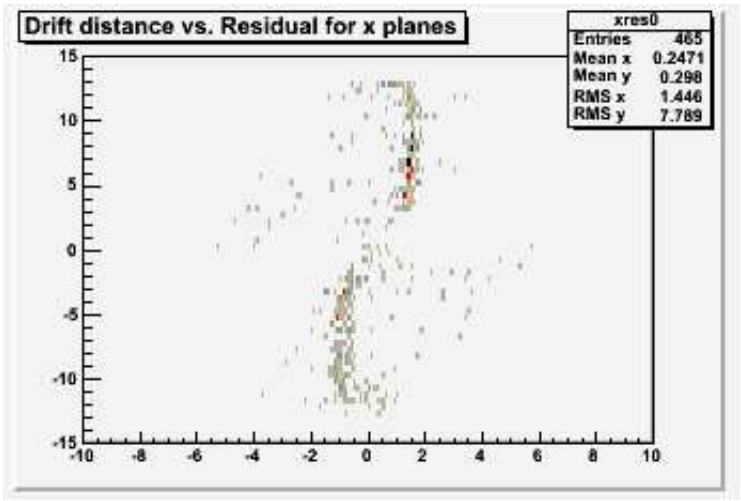

Figure 50: Plot of drift distance vs. fit residual for one of the 4 x-chambers in our cosmic ray test stand showing the current level of the time-to-distance calibrations.

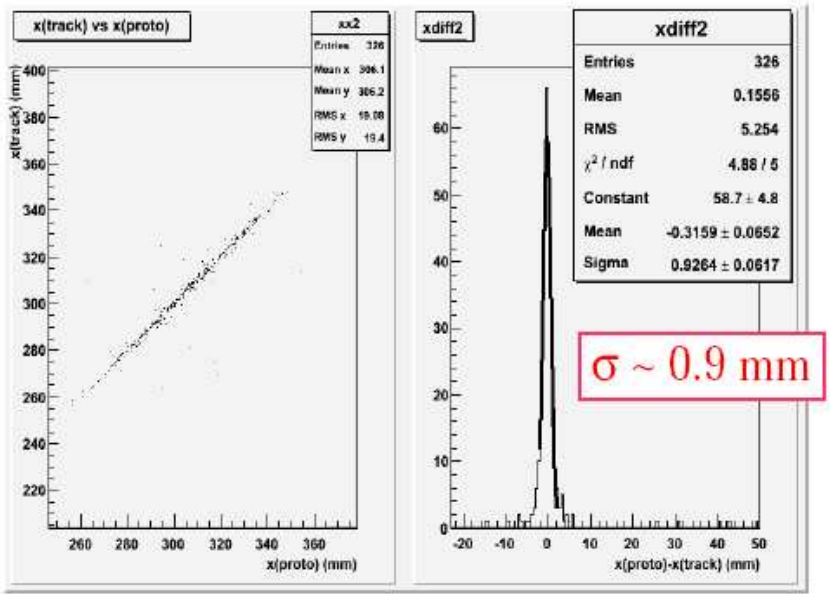

Figure 51: (Left) Correlation of the x-coordinate at the location of the FDC measured from the external tracking chambers to that measured in the FDC drift time measurement. (Right) Current resolution achieved in the FDC wire plane coordinate measurement.

resolution increase is expected to be a factor of $\sqrt{2}$. At the current time we are investigating a configuration of our chamber with such a configuration to access its impact factor on the resolution. Note that the semi-empirical form that we are employing for our fits (see Eq. 3) was derived for the case where the wires are either parallel or perpendicular to the strips [17]. Since we are looking at a projection onto a plane at another angle, the form may not be the appropriate approximation for our geometry due to the associated skewing.

2). Preliminary studies of our prototype chamber data with the Hall B SIP preamplifiers and post-amplifiers indicates that noise levels are not optimized. We anticipate that with the ASIC preamplifiers we should expect slightly improved signal-to-noise performance.

3). Our channel-to-channel gain calibrations (discussed in Section 7.2) are rather crude and we expect that with more precise calibrations the resolution of our cathode coordinate measurement will improve.

4). Recently we have reworked the grounding scheme for our prototype chamber and have witnessed significantly reduced noise levels on the anode and cathode readout. Studies are now underway to quantify the resolutions of the chamber in this new configuration.

8 Gas System

There are several basic requirements that need to be met by the chamber gas that will be used for the FDC system. These include a high drift velocity, low Lorentz angle, and for safety, we much prefer a non-flammable mixture. It is important to understand that the performance of a cathode chamber in terms of cathode position resolution is reasonably insensitive to the exact values of the gas parameters. Here variations of the drift velocity or non-uniform drift velocities as a function of E/p (i.e. electric field/pressure) are relatively unimportant. For the same reason, the cathode readout operation is immune to modest variations of temperature and pressure. Variations in gas gain on the order of 20% do not strongly affect the cathode resolution since a relative charge measurement in adjacent strips is involved. However, for operation of the drift chambers, more precise controls are essential. Our nominal choice of gas for the FDC chambers is a mixture of 90% argon with 10% carbon dioxide. This is the gas mixture that we have been employing in our prototype chamber. We have plans to do performance tests of the chamber with a variety of mixtures to make our final choice. The only constraint that we are imposing at the current time is that the mixture be non-flammable.

The current layout for the FDC gas system is shown in Fig. 52. The proposed gas system will be split into several separate sections to satisfy JLab safety regulations and for space and cost reasons. The first section will be a fenced, outdoor gas bottle corral for off-line gas inventory and empty bottle storage. This will be positioned adjacent to both the gas shed and the driveway for truck access. On an exterior wall of the gas shed, but under a roof, will be the on-line gas bottles. There will be two bottles of each gas type used, connected to an automatic change-over gas bottle manifold system. This will guarantee uninterrupted gas flow. As required by the JLab Flammable Gas Standard, an excess flow valve will be installed downstream from the bottle regulators as close as possible to the penetration into the gas shed. It is intended though, that these chambers will be operated with mixtures of non-flammable gases. Inside the gas shed will be the mixing and flow control stations. It is intended that this gas system be completely autonomous and not be dependent on outside networks for operation. The proposed controller does allow for exterior control, but historically that has created problems. The gas shed is part of the counting house on a wall adjacent to the experimental hall. A short underground penetration will go from the gas shed to the hall. This will protect the gas lines from temperature extremes. The planned controller for this unit is the MKS 647B mass flow control and 8 proportional flow control valves. There are several of these units in use in the existing JLab experimental halls and they have demonstrated long-term reliability and ease of use. An uninterruptible power supply will power the 647 to protect the controller from power failures and guarantee a continuous gas supply. The 647 can control up to eight mass flow control valves. It is intended that each of the four FDC packages will have independent control of the flow rate. This will allow two flow channels per FDC package. Each of the individual layers within each package will be fed in series.

Gas studies will be done to select the optimal gas mix for these chambers with the small prototype drift chamber. Silicone oil filled bubblers will be installed upstream in parallel and downstream in series from the chamber sections to protect the chambers from over pressure. A Panametric oxygen and water monitor will be set up in a sampling mode in the four

chamber effluent lines. This will read each of the four chamber vent lines in sequence and report to the Hall D slow controls system. These monitoring systems will have sensitivity at the parts per million level. The chamber effluent lines will vent through a central hall vent stack to the outdoors. The system is being designed to allow for 3 to 5 volume exchanges per day.

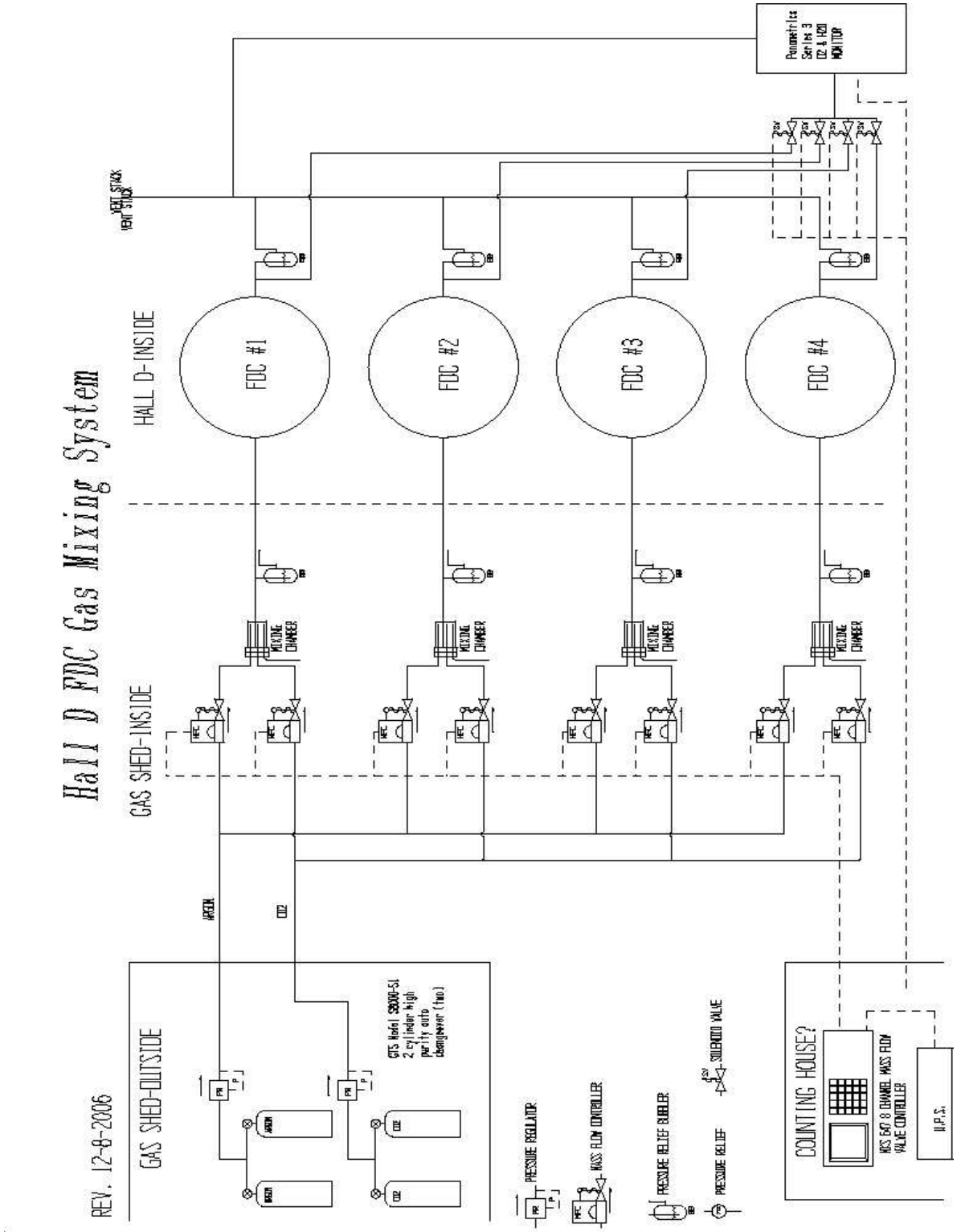

Figure 52: Schematic layout of the planned FDC gas system. The gas mixing system will include MKS mass-flow controllers. The chambers within a given package will be connected together in series. The exhaust of each package will be monitored for oxygen and water contamination at the part per million level. The system does not employ recirculation and designed to handle a non-flammable gas mixture.

9 Failure Modes and Mitigation

An important aspect of the design of the FDC system is to consider possible failure modes of the system in order to understand its impact on chamber operation. Our goal is to take all of these failure modes into consideration within the design and planning to minimize their potential impact. The list of failure modes that we have considered comes from 10 years of operational experience with the CLAS drift chambers in Hall B at JLab. An important aspect of our considerations is to allow access to critical detector components.

In the remainder of this section we provide the list of failure modes that we have considered and how we have affected the design to mitigate each of these items.

- **Broken Wires:** Broken wires are not expected to be a frequent occurrence in the FDC system. However due to the fact that we have suitable redundancy in the system and reasonably fine HV granularity, these affected chamber areas can be turned off and the impact on the tracking efficiency should be minimal. Given the modularity of the system, the chamber can be relatively easily disassembled and the wires can be replaced using standard techniques.

- **Blown Fuses:** Blown fuses in the LV system will cause an alarm to indicate which fuse has blown. With the design of the LV system, these fuses can be easily accessed and replaced.

- **HV or LV Disconnect:** If HV or LV disconnects occur at the chamber end, the design of the system allows for relatively easy access to the full perimeter of the chamber. The jumpers to the STB for the LV and to the HVTB for the HV will be robust connections and access to these connectors will be possible for all chamber layers.

- **Regulator Failure, Circuit Board Shorts, Preamp Corrosion:** A key aspect of the FDC design is that we have designed the system with preamplifier daughter boards that can be accessed and easily replaced with spares.

- **Pinched Gas Line, Gas Leak:** Pinched gas lines and gas leaks will be detectable for each package due to the output bubblers on each package. We have designed the system to allow access and visual inspection of all gas lines. Gas leaks can be detected relatively quickly in a given chamber packages by removing individual layers from the series gas connection in a given package. Once the affected layer has been determined, we have sufficient access to the chamber perimeter to make temporary repairs. For larger problems we have the ability to take the chamber apart to affect repairs.

- **Swapped Cables:** Swapped cable problems will be mitigated using visual inspection of the chambers as they are cabled. Additionally any cable swaps in the system can be determined using calibration data (cosmic rays) before the chambers are installed in the solenoid.

- **Cable Disconnects:** We plan on having a robust strain relief system at both the chamber end and the electronics end. We will design the chambers to include locking connectors for all signal cables.

- **High Current Draw, Increased Noise, Internal Chamber Short:** To reduce problems of this sort we will employ chamber-safe materials and practices at all stages of chamber construction. Problems on the STB boards are expected to be minimized due to the fact that the preamplifier daughter boards are removable. We will also study a variety of dielectric materials for our circuit boards to ensure that they are quiet. Any internal chamber problems can be studied relatively easily as the modular chambers can be disassembled.

10 Installation & Survey

The installation of the FDC is illustrated schematically in Fig. 53. the FDC system will be placed on a hydraulic table with a set of aligned rails that ultimately will couple to the rails inside the solenoid (mounted on the inside face of the BCAL system). The hydraulic table will be raised up to enable the rails on the installation table to mate with those inside the solenoid. The survey and cabling of the system will then proceed before insertion into the solenoid.

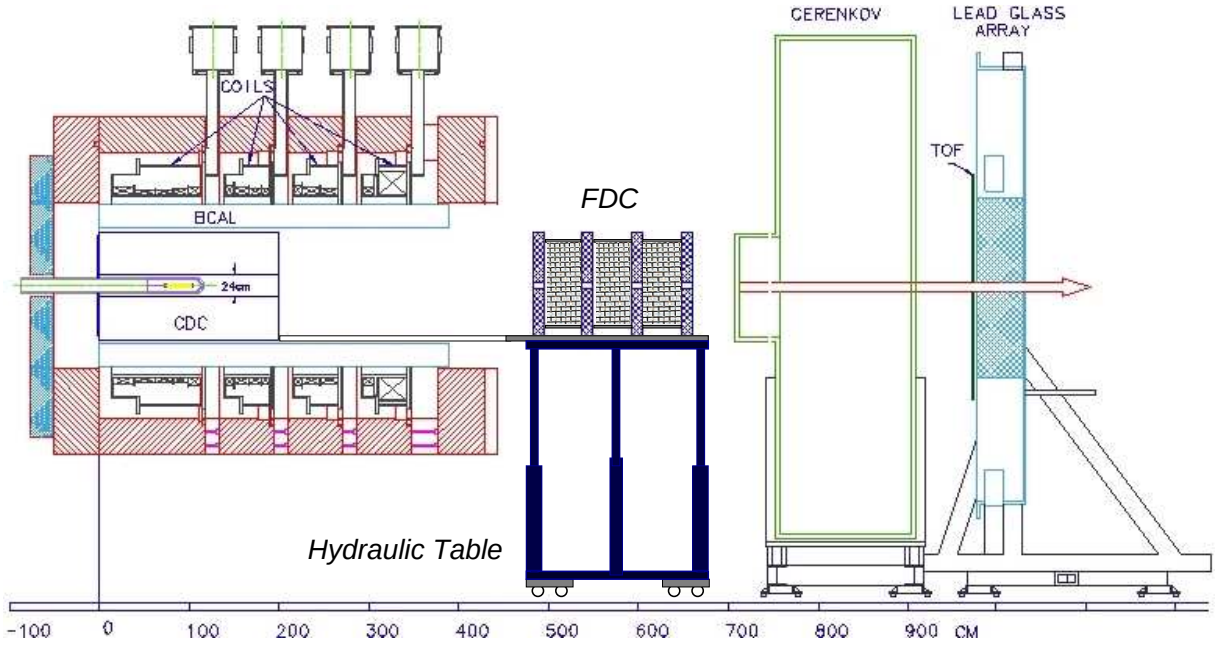

Figure 53: Schematic representation of the FDC system on its installation cart prior to insertion into the solenoid.

The survey and alignment plans for the FDC are based on ongoing discussions with the JLab survey group. At the present time we plan on outfitting each chamber package with tooling balls/sighting flags about its perimeter. The individual packages will be surveyed on their support table before cabling. Fiducializing will take place relative to survey monuments in the Hall and on the solenoid magnet. The chambers will then be surveyed again after cabling is complete. The survey will define the plane of each chamber package in space. The final step of the survey is to sight the downstream end of the FDC system after installation in the magnet.

The chamber system will have some degree of alignment adjustability through the adjustment of the feet that attach to the rail system. However we foresee that this will only be used for gross adjustments and the survey results, coupled with information from data runs with the solenoid magnetic off, will be used to set the parameters in the reconstruction software.

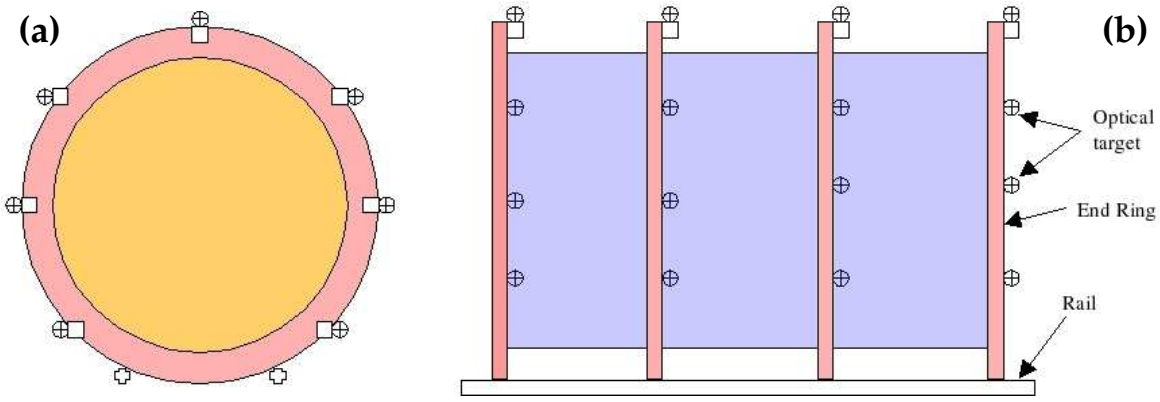

Figure 54: Front view (a) and side view (b) of the FDC system highlighting the location of the survey fiducials that will be included.

11 Future Prototyping

The small-scale prototype discussed in Section 7 has been the work horse of our R&D program on the FDCs to this point in time. We still have a long list of plans for this detector. However we are currently working on the design of a full-scale FDC prototype chamber that will allow us to finalize the design and construction techniques for the final FDC chamber system. The full-scale prototype should be completed by the end of 2007. This chamber, after undergoing a sizable test plan on the bench, will also be used for chamber beam tests and studies in a magnetic field.

The main areas of study and development with the full-scale prototype chamber include the following:

- Finalizing the mechanical design of the chamber frames.
- Finalizing the layout of the cathode strips.
- Developing a technique to mount the cathodes within our flatness specifications.
- Finalizing the layout of the wire plane including the STB and HVTB circuit boards. This work includes detailed optimization of the ground definitions in the chamber.
- Finalizing the assembly procedures for an FDC package.
- Studies of noise levels and current draw.
- Studies of pulse characteristics to finalize the design of the preamplifiers and the associated shaper circuits.
- Studies of the uniformity of the chamber response and edge affects.
- Development of final algorithms for fast cathode position reconstruction and time-to-distance calibration procedures.
- Development of the chamber support and mounting system.
- Development and testing of the chamber cooling system.

In addition to this work, we are also considering construction of full scale mock-ups of the FDC system to develop chamber mounting and alignment schemes, testing installation and handling procedures, and finalizing the cable layout and support scheme.

12 Chamber Resolution Effects

Resolution degradation of cathode chambers comes primarily from two sources, tracks inclined from the normal to the face of the chamber and Lorentz angle effects. In both cases the spatial resolution is degraded because the avalanche charge is distributed non-uniformly along the anode wire due to the energy loss fluctuations in the gas. The cathode position resolution is optimum when the avalanche is formed at a single point along the wire. A finite spatial extent of the anode charge results in a resolution degradation $\mathcal{D}$. Studies of the PHENIX cathode chamber [14] have shown that $\mathcal{D}$ goes as:

$$\mathcal{D} = 0.16 d \tan\theta, \tag{6}$$

where d is the anode-to-cathode spacing and θ is the angle from the normal to the face of the chamber. This functional form is shown in Fig. 55 and indicates a linear dependence of the degradation for incident angles below roughly 30°. Another result from CMS studies of a cathode strip chamber with a similar cell geometry to ours is shown in Fig. 55 [23]. The range of incident track angles on the FDC is below 20° as shown in Fig. 56.

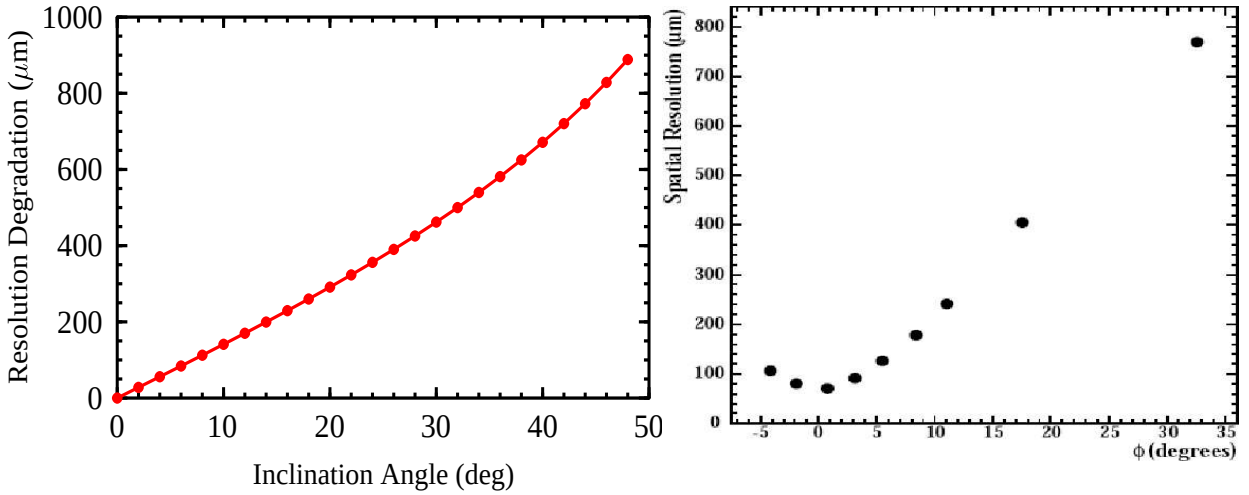

Figure 55: (Left) Plot of the resolution degradation vs. track incidence angle from the PHENIX cathode chamber [14] from eq.(6). (Right) Plot of the measured resolution in the CMS cathode chamber as a function of track incidence angle [23].

The degradation of cathode coordinate resolution with increasing track incidence angle is inescapable, but the level of the smearing intimately depends on the chamber design and field configuration. These effects will be quantified with our FDC prototypes in the near future. To date our studies with the prototype chamber have focused on normally incident tracks ($\theta < 10°$).

Skewed or non-local charge distributions along the anode wire can also be caused by a Lorentz force on the drifting electrons from the presence of magnetic field components that are not collinear with the electric field of the chambers. The force causes a deflection of the drifting electrons characterized by the Lorentz angle θ_L, where

$$\tan\theta_L \approx \frac{\left|\vec{v}_D \times \vec{B}\right|}{\left|\vec{E}\right|}, \tag{7}$$

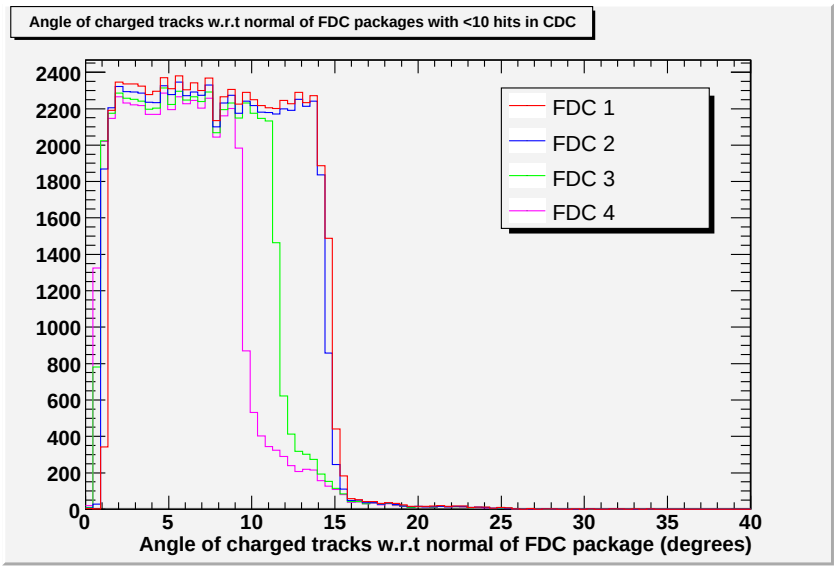

Figure 56: GEANT simulation result showing the range of incident angles on each FDC package.

with drift velocity $\vec{v}_D$, electric field $\vec{E}$, and magnetic field $\vec{B}$. The Lorentz angle for our nominal detector cell configuration is shown in Fig. 57. For our geometry the Lorentz effect results in a systematic shift of the avalanche along the wire relative to the B=0 case, depending on the location of the ionization events within a chamber cell, as illustrated schematically in Fig. 58. It also results in a degradation of the resolution because of the spread of the charge along the wire.

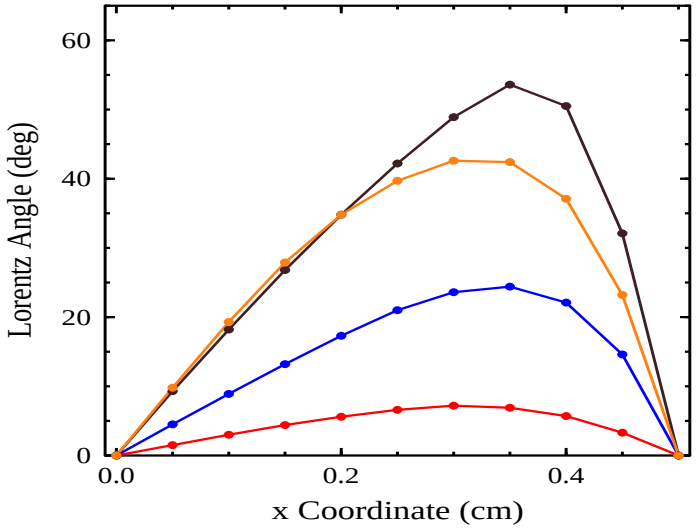

Figure 57: GARFIELD computation of the Lorentz angle in the FDC chamber. Here the sense wire is at x=0 and the field wire is at x=0.5. The different curves correspond to different perpendicular distances from the wire plane (0.05 cm to 0.45 cm).

GARFIELD calculations with the 2 T longitudinal field turned on are shown in Fig. 59 for our nominal cell geometry. These calculations show that the time-to-distance calibration for the wire readout will be affected due to the Lorentz-angle effect. The effective drift velocity in the 90-10 Ar/CO_2 gas reduces from 50 μm/ns to 35 μm/ns. The effect on the

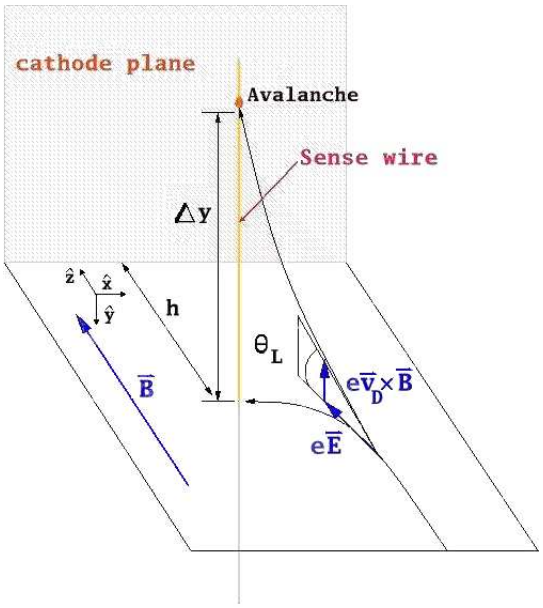

Figure 58: Deflection of drifting electrons due to the Lorentz force.

cathode resolution is more significant. Fig. 60 shows how the resolutions in a large pitch cathode chamber from CMS [23] were affected by the magnetic field. Again the expected effect on the resolution is closely tied to the chamber design. At the current time, all of our prototype studies have been performed with no magnetic field. Studies of the chamber performance as a function of magnetic field will be performed in the near future.

Fig. 61 shows the magnetic field at the location of each FDC chamber. Currently the chambers are positioned in the solenoid with an equal spacing of 63 cm between each package. This positioning has not yet been optimized, however it is clear that the calibrations for each chamber will be quite different and this needs to be properly accounted for in our simulations to understand the full impact to the track reconstructions. It is seen that the most downstream package is affected least by the Lorentz angle effect and the most upstream package has the largest affect.

The final effect that should be mentioned is the efficiency for recording track hits and the cathode strip and drift coordinate resolutions near the edge of the chamber active area. Due to the circular shape of our chambers, the electric field will be non-uniform near the perimeter of the active area due to the different wire lengths (see Fig. 62). This effect will be studied with the full-scale prototype system that is presently being designed. In order to acquire precision data with suitable statistics, this study will have to be performed in-beam.

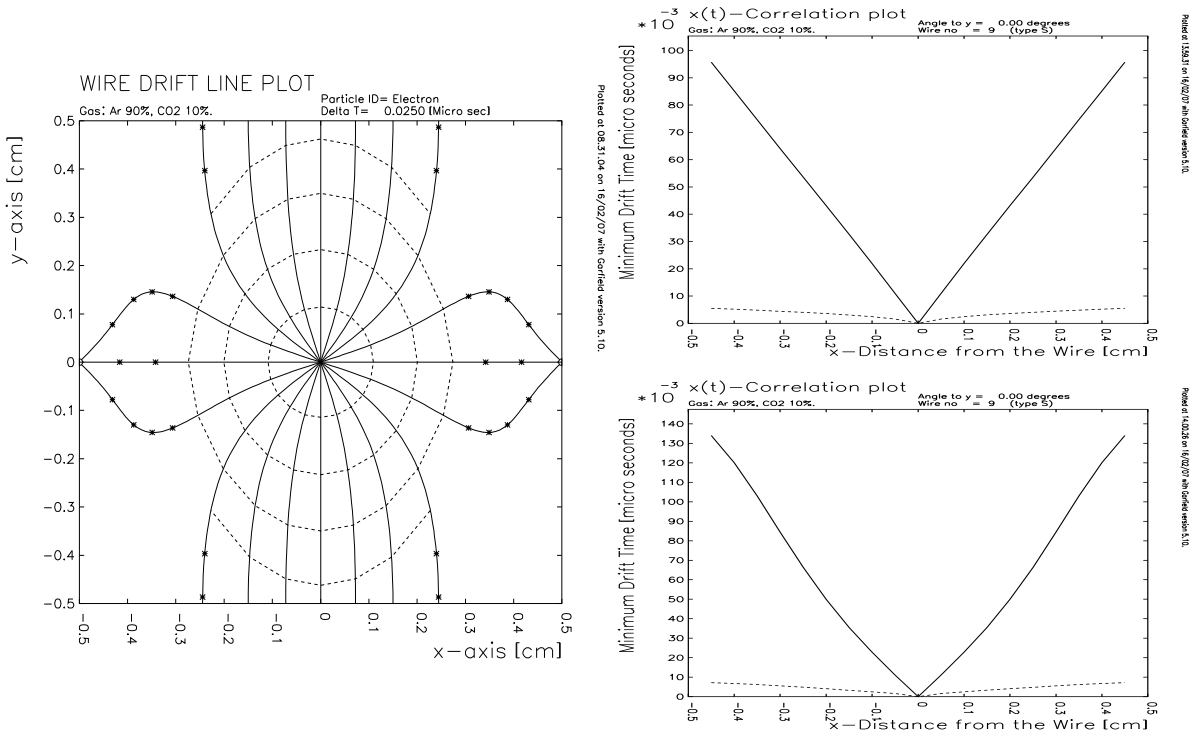

Figure 59: (Left) GARFIELD calculations of the electric field lines for our nominal cell design and gas mixture with the 2 T magnetic field turned on. (Right) GARFIELD calculations of the drift time without (top) and with (bottom) the magnetic field turned on.

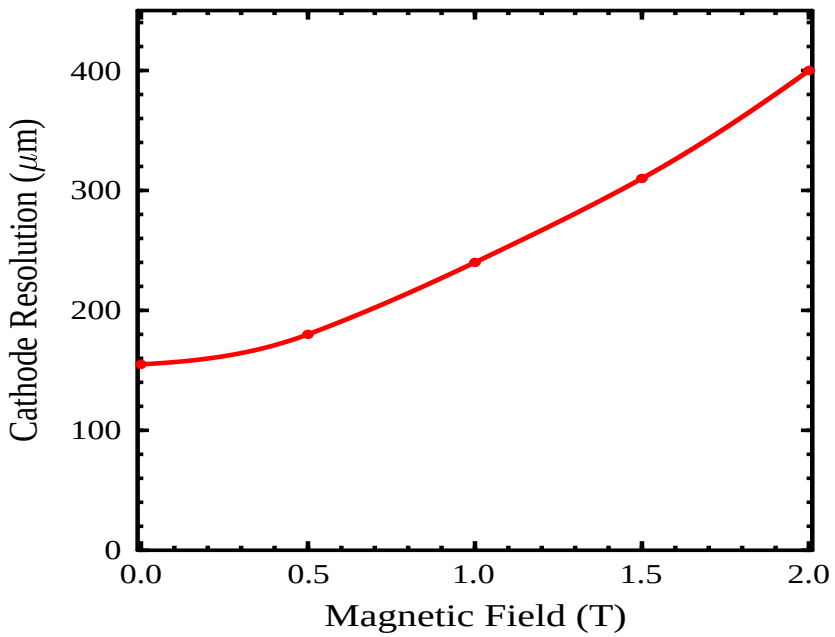

Figure 60: CMS results showing the effect of magnetic field on the resolution of their large-pitch cathode chambers. Here the field orientation is longitudinal through the chamber (the same as the GlueX field configuration).

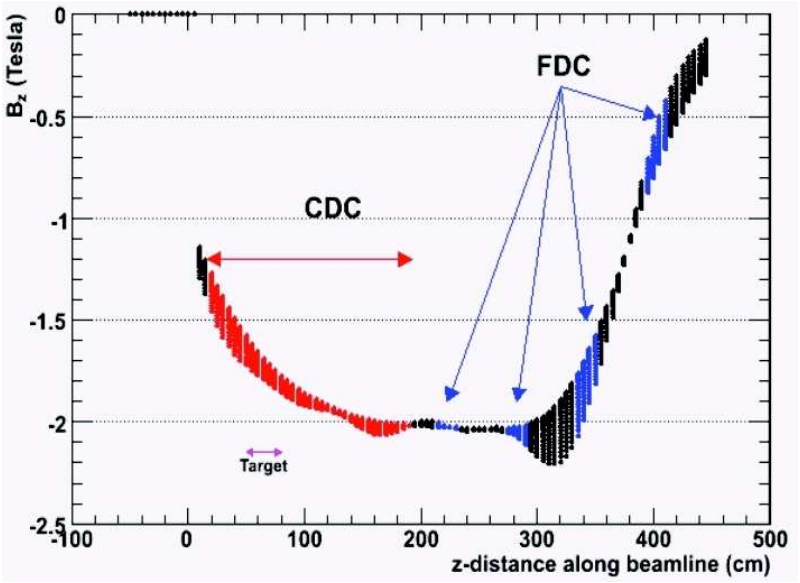

Figure 61: TOSCA calculation of the z-component of the magnetic field in the GlueX solenoid vs. the z coordinate. The figure shows the locations of the GlueX tracking chambers in this field. The vertical extent of each point shows the variation in the field at a given z location as a function of the radial coordinate.

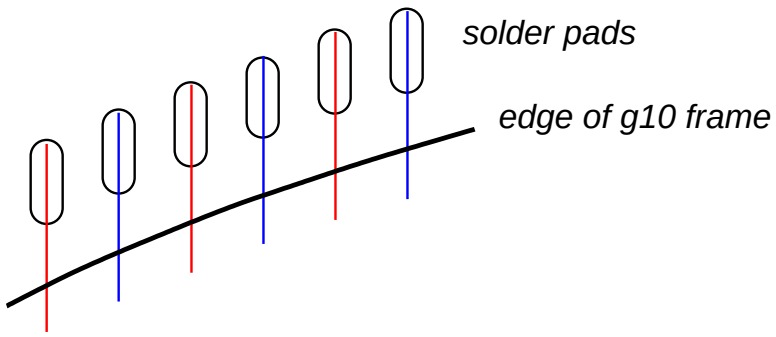

Figure 62: Schematic close-up view of a portion of the STB showing the variation in wire lengths along the perimeter of the chamber that will give rise to a non-uniform electric field.

13 Safety

We have identified four main safety issues in the design of the FDC system. These include:

- Gas System
- High Voltage System
- Low Voltage System
- Chamber Cooling System

Our design has attempted to address the possible safety issues in each of these areas. For the gas system, we plan from the start on employing only non-flammable gas mixtures. Our gas system (see Section 52) is designed to provide for both underpressure and overpressure protection. The gas outlet of each FDC package will also be monitored for oxygen content.

Both the high voltage and low voltage systems will incorporate overvoltage and overcurrent protection. The systems will include monitoring and alarms if these parameters go outside of a defined specification. The low voltage system includes the further protections of a fuse on each low voltage line to the chamber.

The chamber cooling system is being designed to provide a safe and constant operating temperature for the on-chamber electronics, as well as the chambers themselves. The low voltage will power off on an overtemperature condition. We will plan on including multiple thermistors on each FDC package to continuously monitor the temperature.

A FDC Nominal Design Parameters

Parameter	Value
Wire spacing s	10 mm (anode-anode) 5 mm (anode-field)
Anode-cathode distance, d	5.0 mm
Cathode readout pitch, w	5.0 mm
Gap between cathode strips, w_g	1.0 mm
Width of cathode strips	4.0 mm
Capacitance between strips	0.6 pF/cm
Resistance between strips	$\sim$20 MΩ
Anode wire radius, r_a	0.010 mm
Wire capacitance per unit length, C_0	$\sim$9 pF/m
Gas gain	8×10^4
Operating voltage at nominal gain	ΔV_{sf}=1950 V
Electric field at cathode, E_c	<1 kV/cm
Electric field on anode wire surface	260 kV/cm
Field-shaping wire radius	0.040 mm
Electric field on field-shaping wire surface	16 kV/cm
Positive ion mobility, μ^+	1.3 cm^2/V/s
Total ion pairs	100/cm
Minimum wire tension	20 gm
Total charge collected	$\sim$1 pC
Charge collected in 30 ns (%)	$\sim$20%

B FDC Construction Time Line

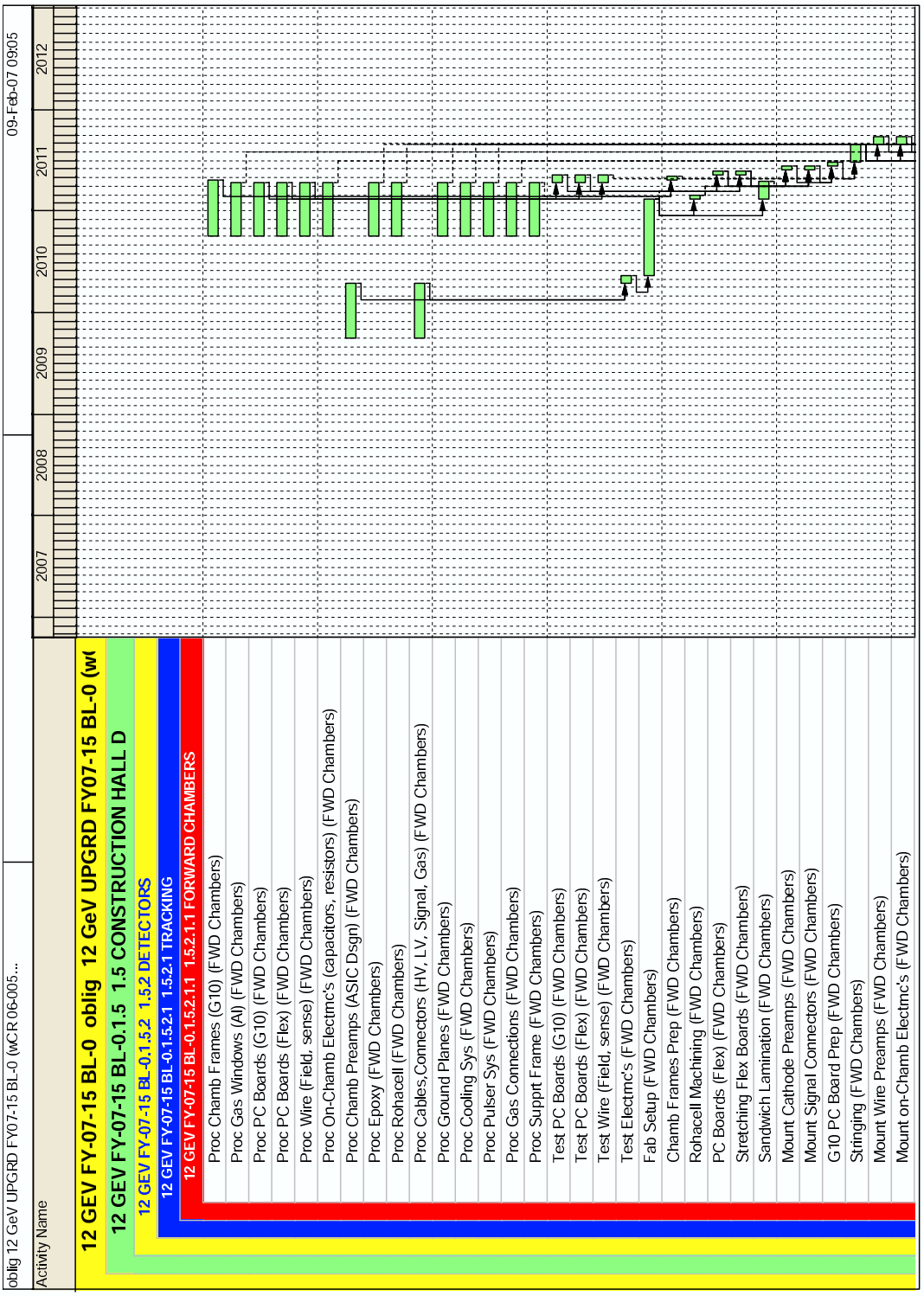

Figure 63: FDC construction time line to begin after completion of R&D phase (part 1).

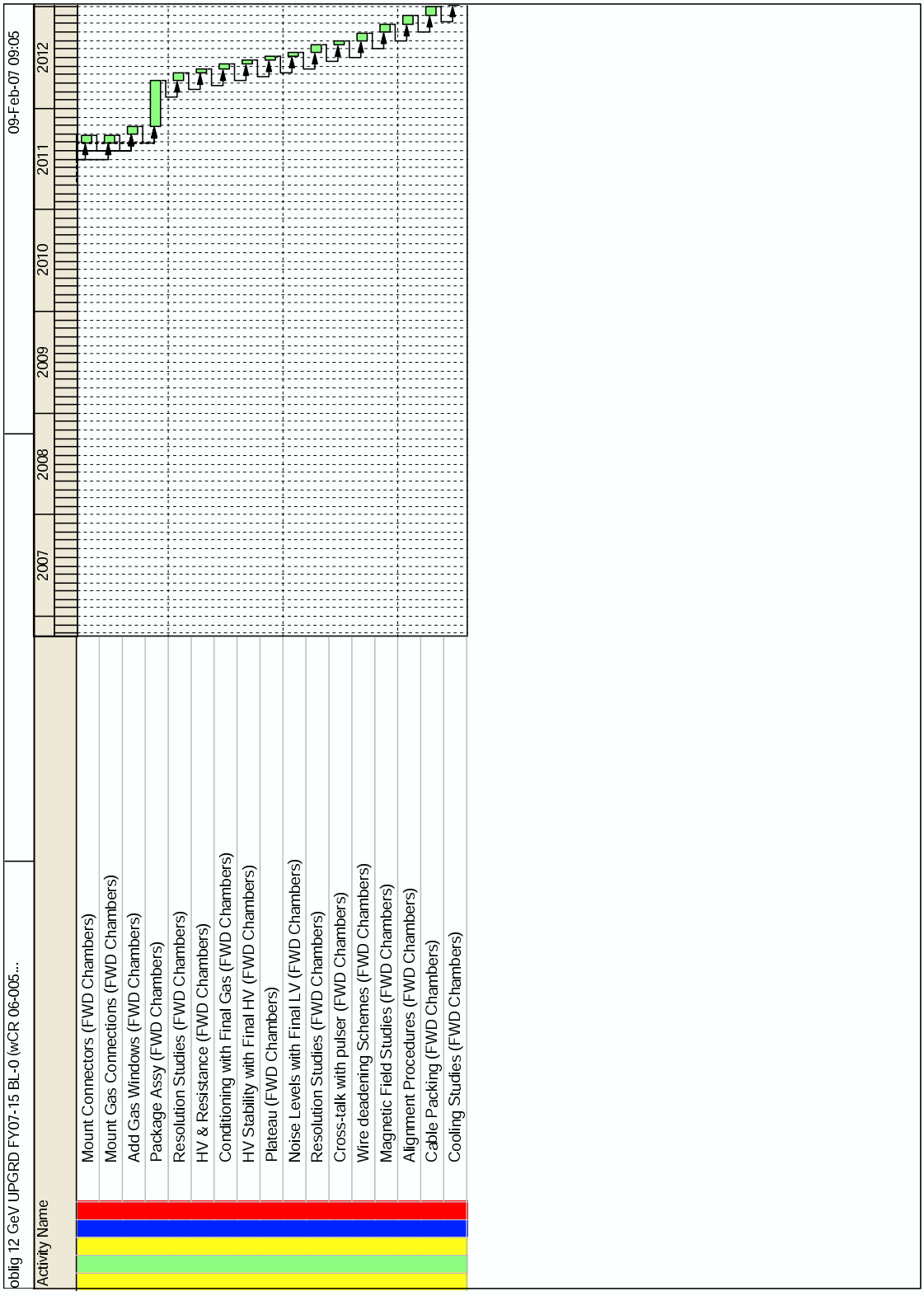

Figure 64: FDC construction time line to begin after completion of R&D phase (part 2).

C dE/dX Capabilities

This section explores some issues related to employing the GlueX Forward Drift Chambers (FDCs) as a system for charged particle identification. The primary method considered here is to measure the specific ionization (dE/dX) to separate charged hadrons (pions, kaons, and protons) by utilizing the fact that different particles can be identified in a drift chamber because of the special relationship between dE/dX and $\beta\gamma$ (the relativistic generalization of velocity) or between dE/dX and momentum P.

The issue of employing the FDC system as a particle identification device (or even to provide supplementary or complementary particle identification information) has arisen due to the present difficulties with the planning for the downstream Cerenkov detector in the GlueX detector system. However, at the current time, dE/dX is *not* a requirement for the FDC system. The information given in this section is explained in much more detail in Ref. [24].

The dE/dX resolution of a drift chamber system (or a gas-sampling device in general) has been determined empirically to obey the relation [25, 26]:

$$\sigma_{dE/dX} = 0.41 n^{-0.43} (x\mathcal{P})^{-0.32}, \tag{8}$$

where n is the number of dE/dX measurements made (which here is given by the number of anode layers in the FDC system, i.e. 24), x is the sampling thickness (or the thickness of a single FDC chamber layer, i.e. 1 cm), and $\mathcal{P}$ is the pressure of the system (here the FDC is assumed to operate at $\mathcal{P}$=1 atm). Using the Bethe-Block formula and the form of the dE/dX resolution in eq.(8), one can predict the separation of two particles with masses M_1 and M_2 in terms of the number of standard deviations via:

$$\mathcal{R} = \frac{dE/dX(M_1) - dE/dX(M_2)}{\sigma_{dE/dX}}. \tag{9}$$

Of interest for the current design of the FDC system is the region in momentum over which pions and kaons, as well as kaons and protons, can be separated. A typical guesstimate is that separation of the different hadron species can be achieved as long as $\mathcal{R} > 2\sigma$. This assumption is used here as our guide.

The main results of this study are shown in Fig. 65 which plots $\mathcal{R}$ vs. momentum P highlighting where K/π and K/p separation is possible within the current FDC system. For these calculations only the chamber gas medium is considered. The mixtures considered here are Argon/CO_2 (90%-10%) and Argon/CH_4 (50%-50%) at 1 atm. Note that resolution considering 24 FDC layers of 1 cm thickness is 10.45%. The main results of Fig. 65 indicate that with the current FDC system design K/π separation is possible below 0.7 GeV/c and above 1.3 GeV/c. As well, K/p separation can be achieved below 1.5 GeV/c.

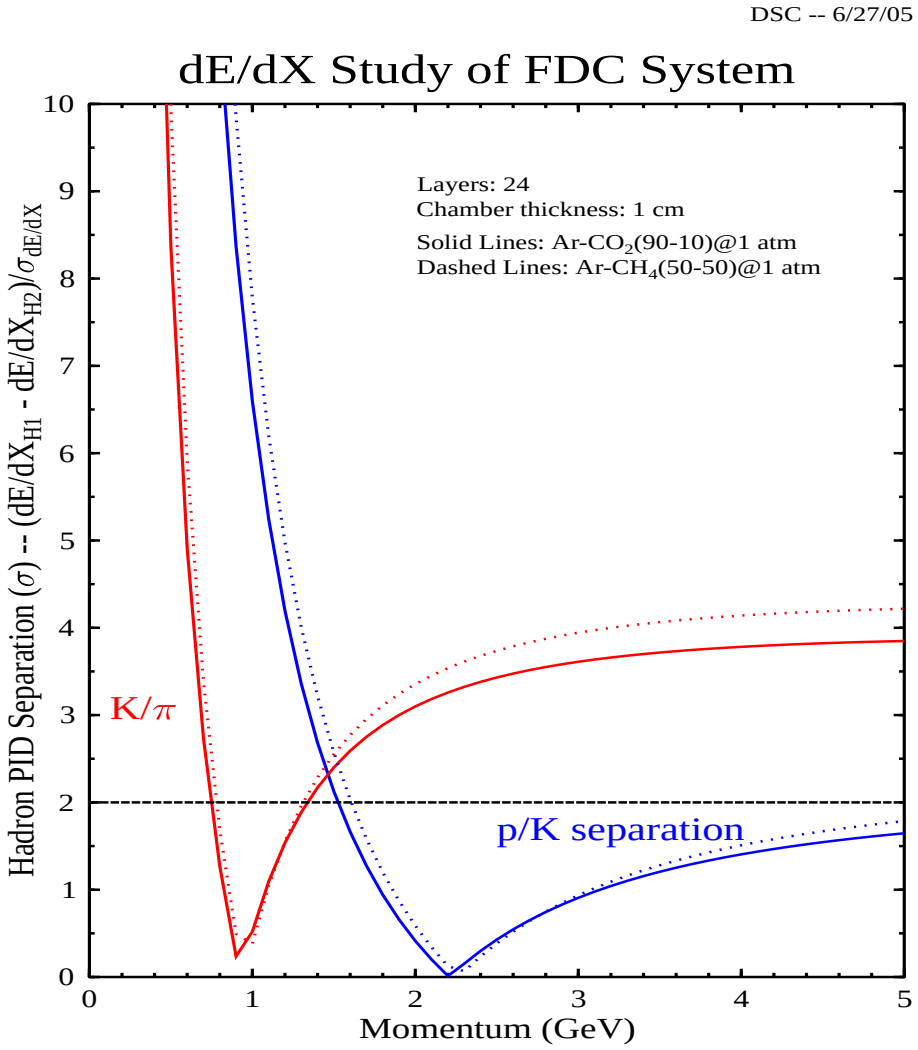

Figure 65: Calculation of the separation (in σ) from eq.(9) between different particle species vs. momentum. The calculations are shown for two different gas mixtures with the current FDC system geometry design assuming all 24 layers are used in the measurement.

D Budget Overview

	Category	Budget Amount
1.	Chamber Wire	\$13k
2.	High Voltage Cables	\$11k
3.	Signal Cables	\$105k
4.	Printed Circuit Boards	\$48k
5.	Cathode Boards	\$125k
6.	Preamplifiers	\$45k
7.	Preamplifier Daughter Boards	\$61k
8.	Low Voltage System	\$11k
9.	Chamber Frames	\$66k
10.	Cathode Backing	\$15k
11.	Ground Planes	\$5k
12.	Mounting and Support System	\$60k
13.	Gas System	\$50k
14.	Chamber Cooling System	\$15k
15.	Components	\$20k
16.	Chamber Stringing	\$100k
17.	Monitoring System	\$15k
	Total	\$765k

Table 3: Budget overview for construction of the FDC system as of Dec. 2006. The full FDC construction budget is contained in Ref. [27].

References

[1] H. Fenker *et al.*, Nucl. Inst. and Meth. A **367**, 285 (1999).

[2] GARFIELD has been developed at the University of Mainz by R. Veenhof and revised by M. Guckes and K. Peters. See HELIOS-note 154, (1986).

[3] D. S. Carman, "FDC Garfield Studies v1.0", (http://www.jlab.org/Hall-D/detector/fdc/design/garfield_study.ps).

[4] J.A. Kadyk, Nucl. Inst. and Methods A **300**, 436 (1991).

[5] S.B. Christo and M.D. Mestayer, "Minimizing Cathode Emission in Drift Chambers", CLAS-Note 92-016, (1992).

[6] S. Taylor, *"Further HDFast simulations of the FDC"*, GlueX-doc–514-v1.

[7] S. Taylor, *"HDFast Simulation Study of the FDC"*, GlueX-doc-418-v2.

[8] R. Jones, *"Detector Models for GlueX Monte Carlo Simulation: the CD2 Baseline"*, GlueX-doc-732-v4.

[9] D.S. Carman, *"FDC On-Chamber Electronics"*, GlueX-doc-753-v1.

[10] Karen Kephart (FNAL), private communication.

[11] S. Taylor, *"Deflections of Cathode Planes Due to Electrostatic Pressure"*, GlueX-doc-668-v1.

[12] Figure taken from talk by Paul O'Connor.

[13] Faro Laser Tracking Systems, http://www.faro.com/.

[14] *PHENIX Collaboration*, PHENIX Internal Note PN125.

[15] D. Aston *et al. (The LASS Collaboration)*, SLAC Internal Note SLAC-298.

[16] GlueX FDC homepage: http://www.jlab.org/Hall-D/detector/fdc/.

[17] E. Mathieson, Nucl. Inst. Meth. A **270**, 602 (1988).

[18] The Newton-Raphson method is an efficient algorithm for finding approximations to the zeros (or roots) of a real-valued function. It is used to find the maximum of the charge distribution by finding a zero in the function's first derivative.

[19] F. Sauli, "Principles of Operation of Multiwire Proportional and Drift Chambers", CERN Internal Report 77-09.

[20] S. Taylor and D.S. Carman, *"Update on FDC Algorithm Development"*, GlueX-doc-601-v2.

[21] S. Taylor and D.S. Carman, *"Update on Studies of the FDC Prototype and Test Stand Setup"*, GlueX-doc-526-v1.

[22] S. Taylor and D.S. Carman, *"FDC Prototype Studies"*, GlueX-doc-453-v1.

[23] M.M. Baarmand *et al.*, Nucl. Inst. Meth. **402**, 36 (1998), from CMS Note 1997/078.

[24] D.S. Carman, "FDC Particle Identification Via dE/dX", GlueX Note 417, (2004).

[25] H. Yamamoto, "dE/dX Particle Identification For Collider Detectors", hep-ex/9912024, (1999).

[26] A.H. Walenta *et al.*, Nucl. Inst. and Meth. **161**, 45 (1979).

[27] D.S. Carman, *"Hall D Forward Drift Chamber Budget"*, GlueX-doc-735-v1.

[28] *ATLAS Collaboration*, ATLAS Technical Design Report, Chapter 6, June 1997.