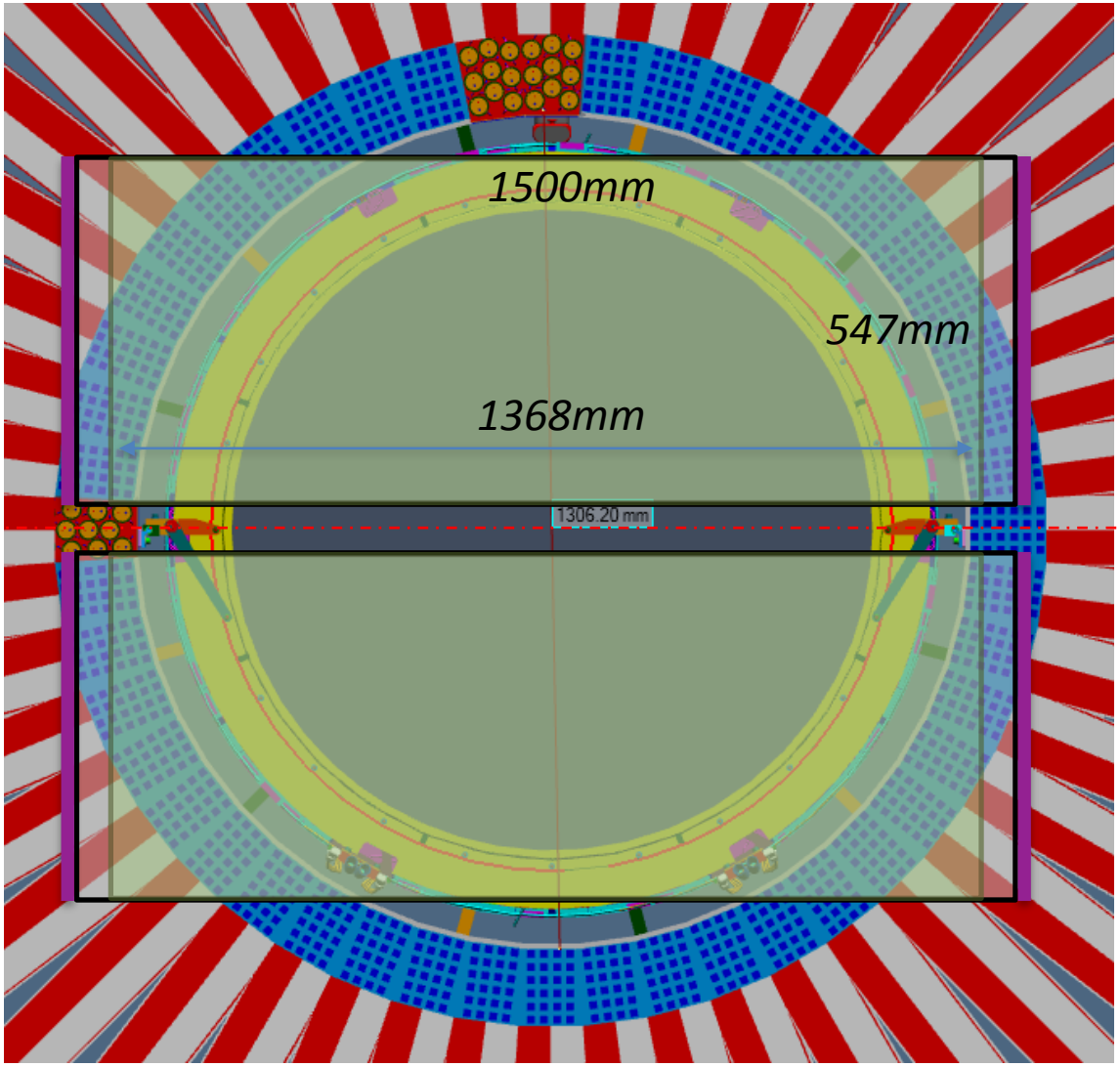
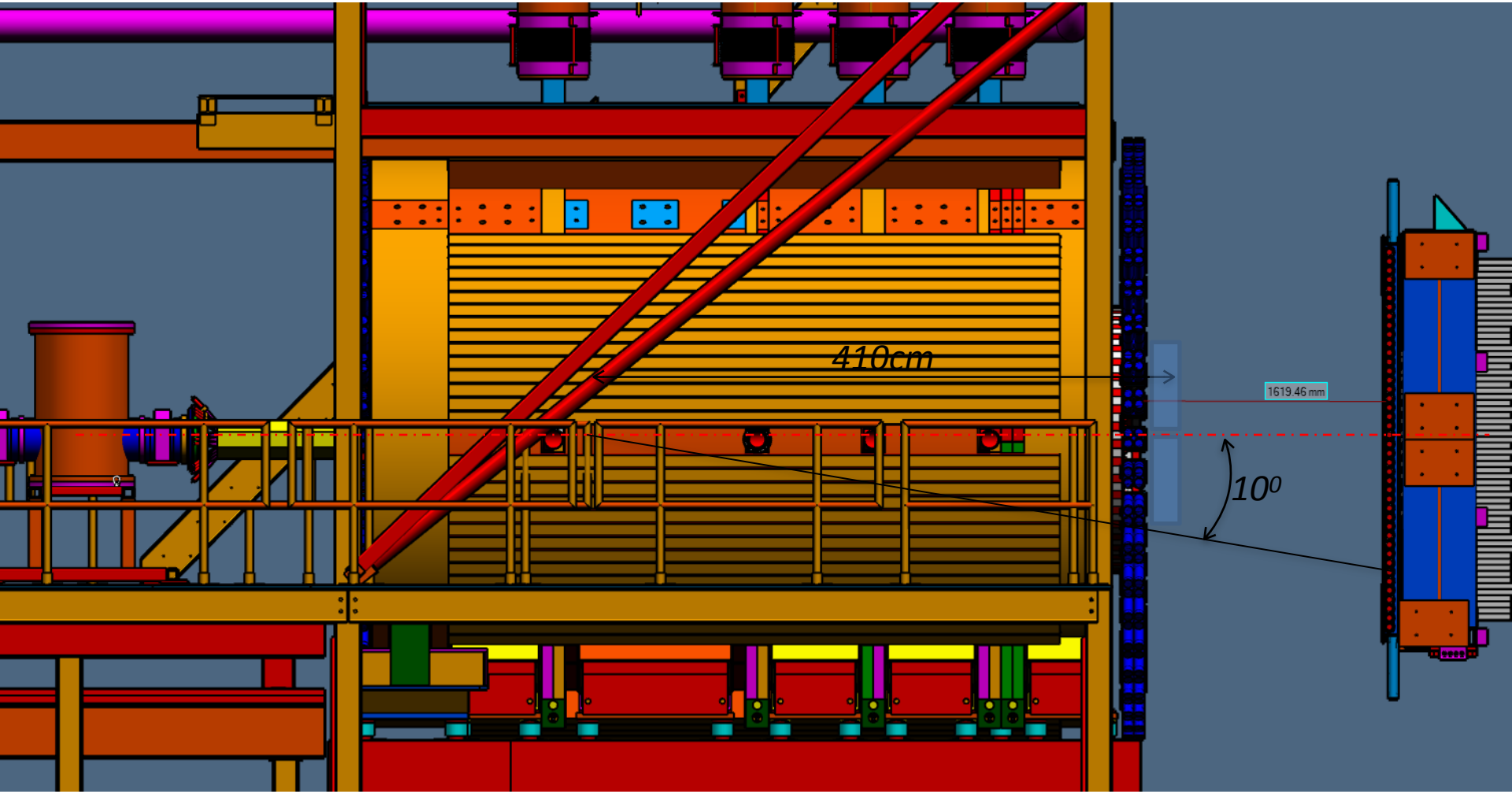
# Option 1

547x 1368 $mm^2$ sensitive area

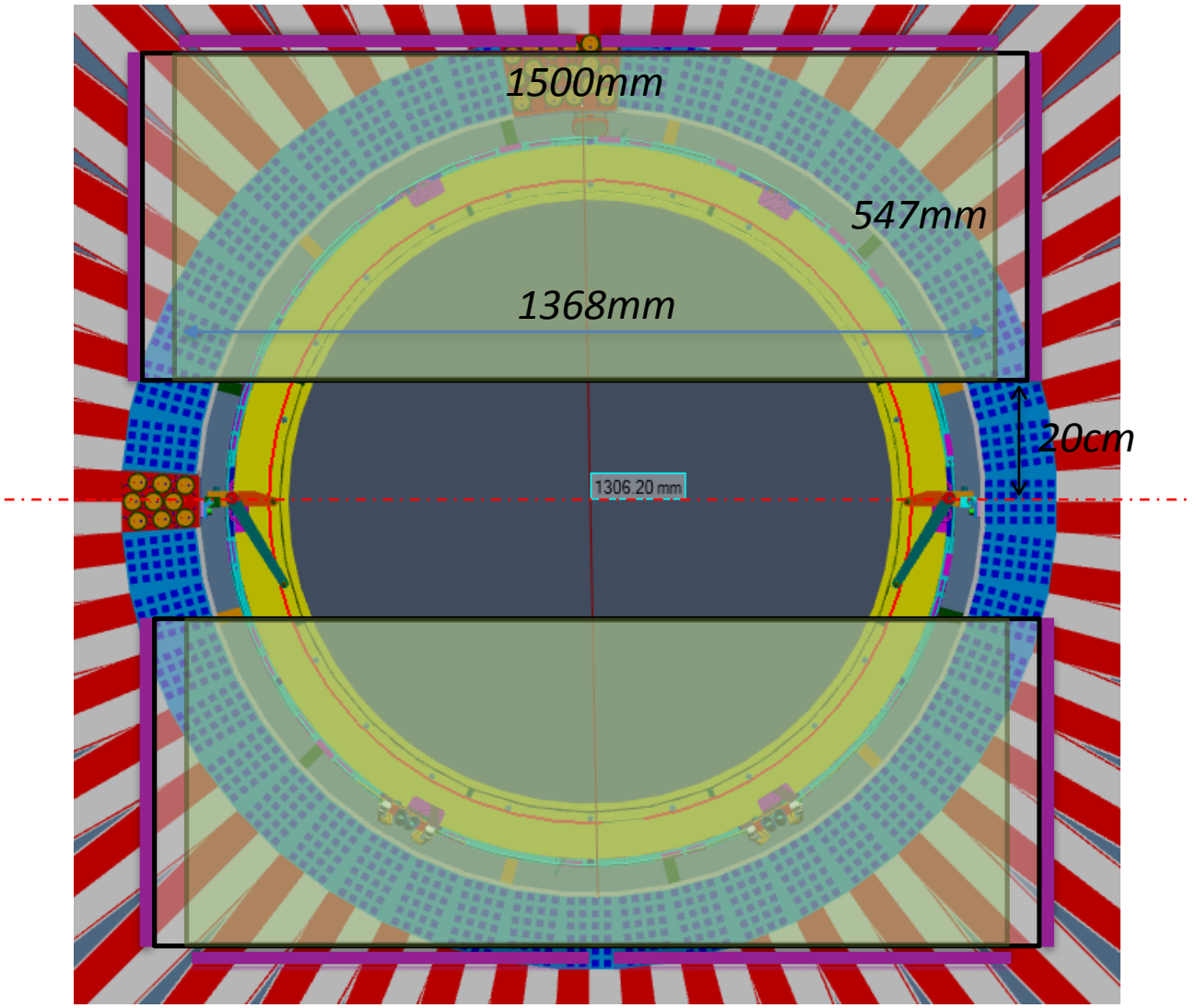


# Option 1



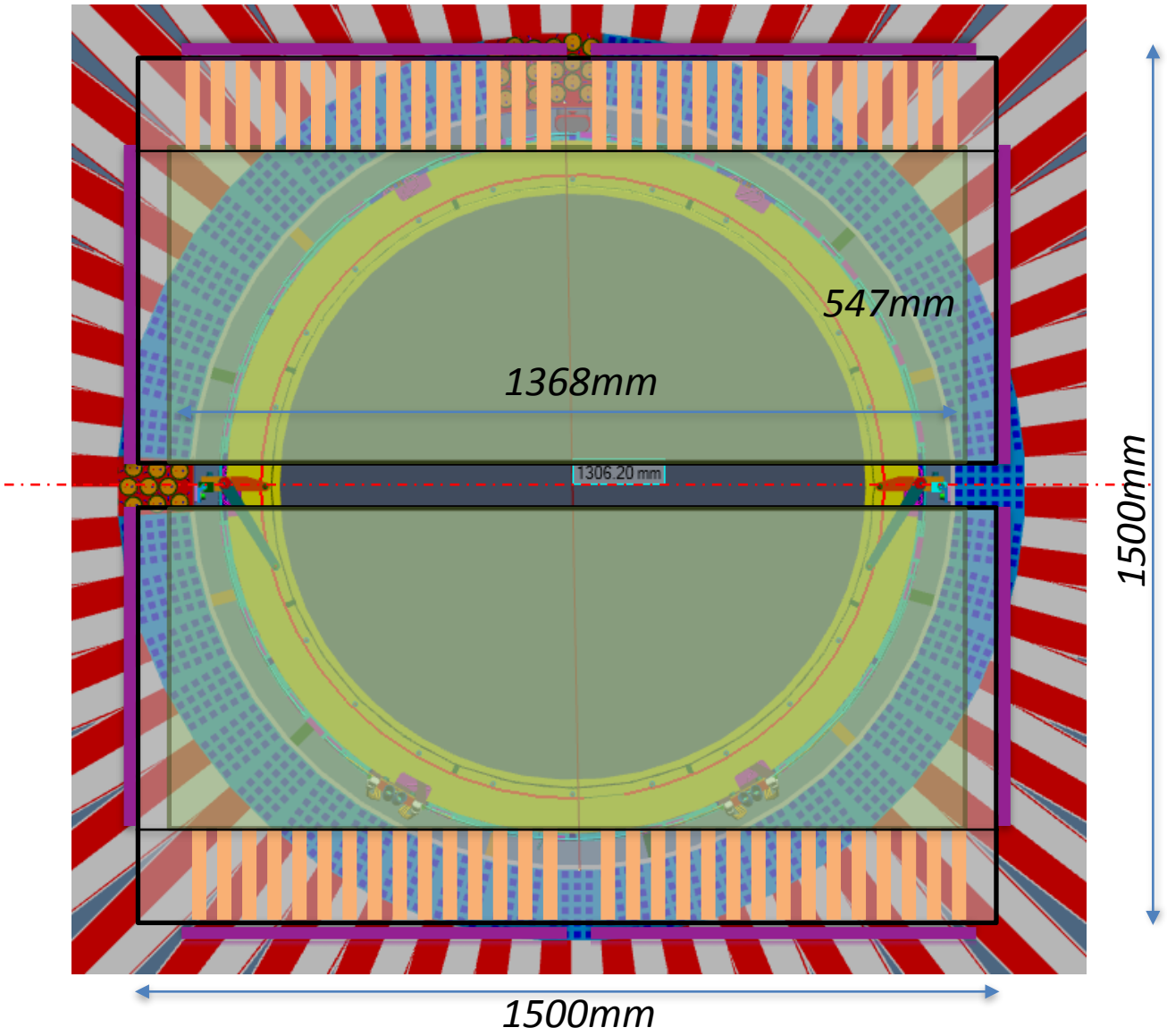
# Option 2

547x 1368 mm$^2$ sensitive area



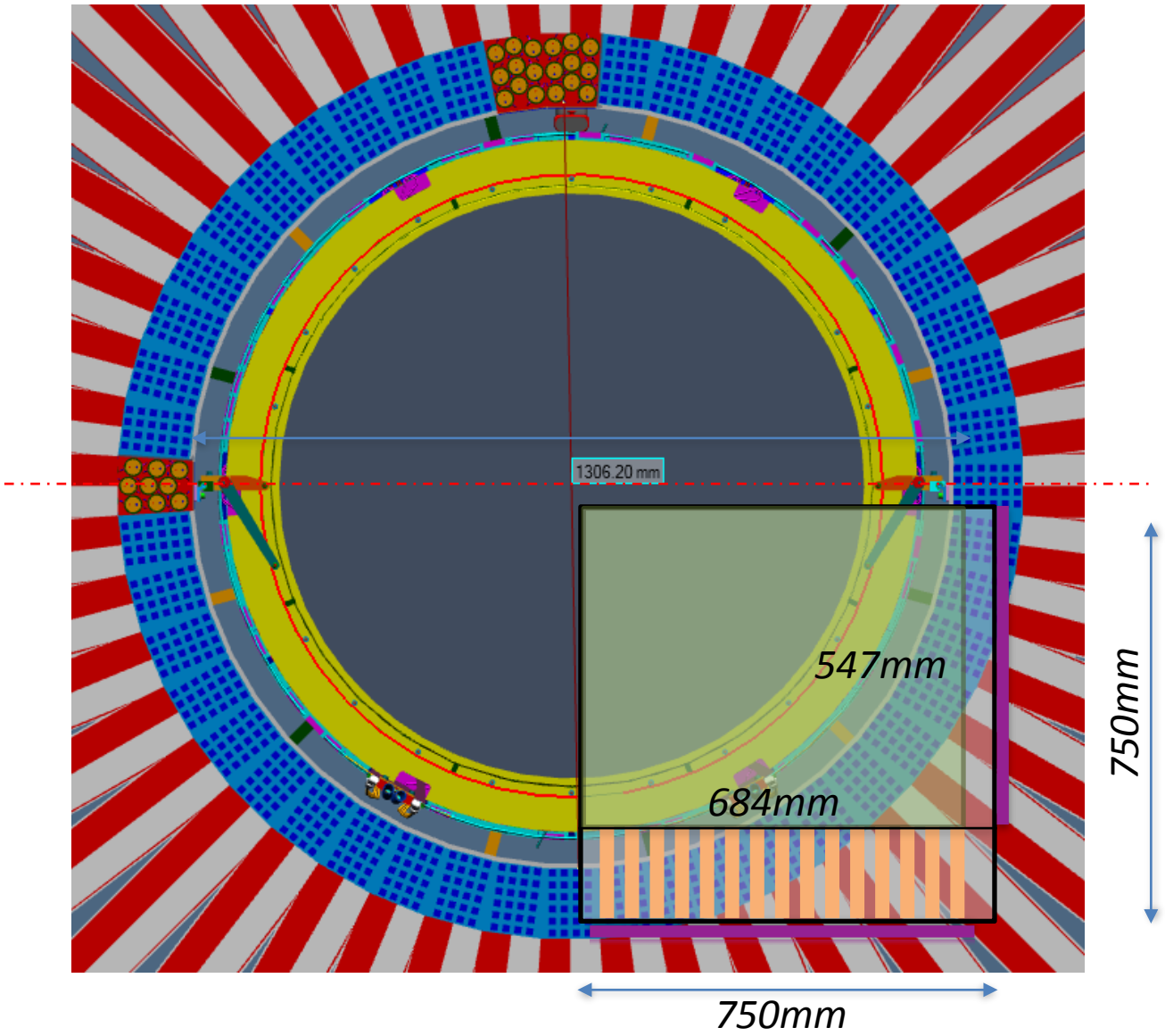
# Option 3

547x 1368 mm$^2$ sensitive area

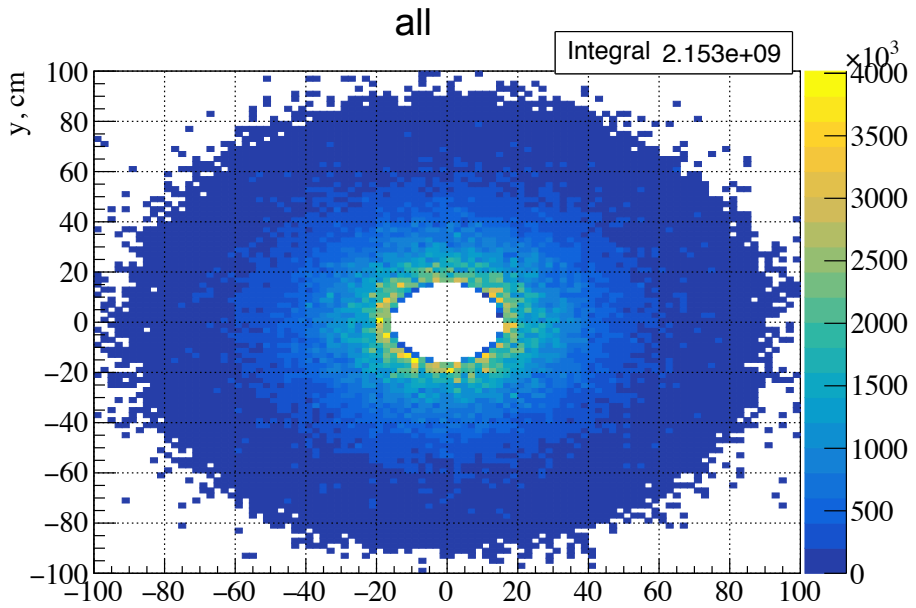


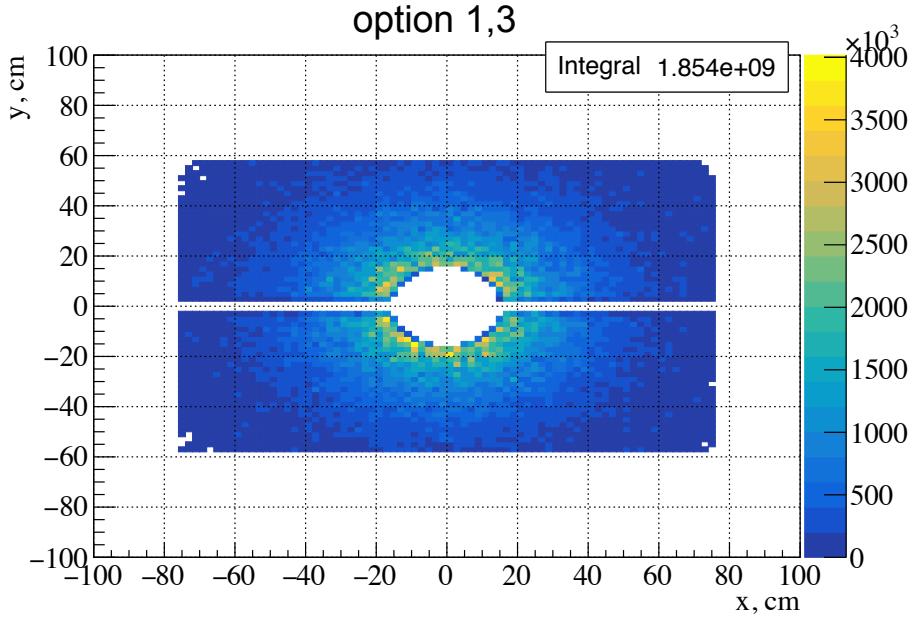
# Proposed prototype - option 3

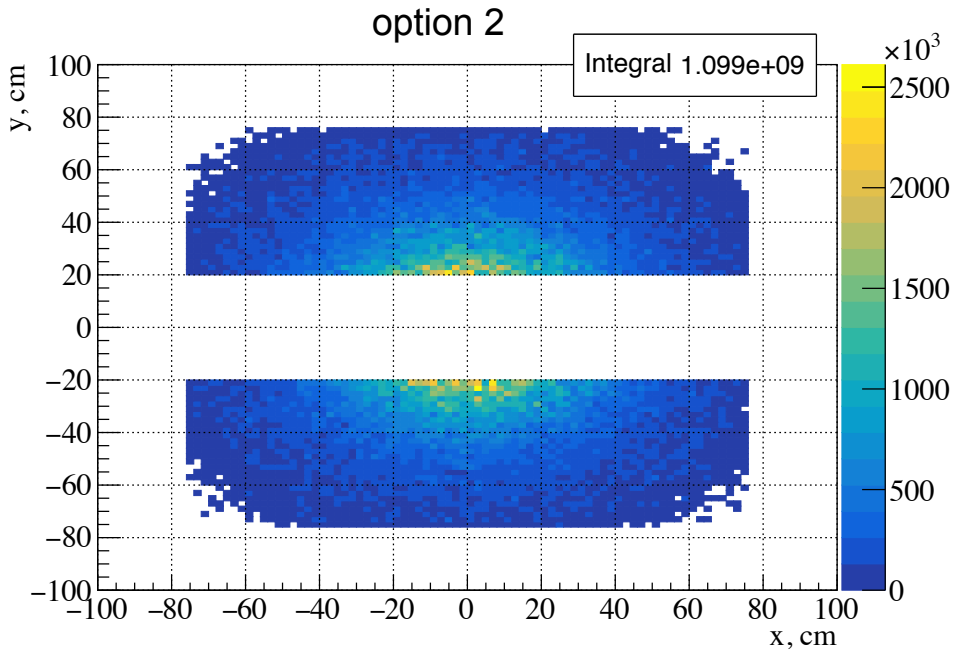
547x 684 mm$^2$ sensitive area



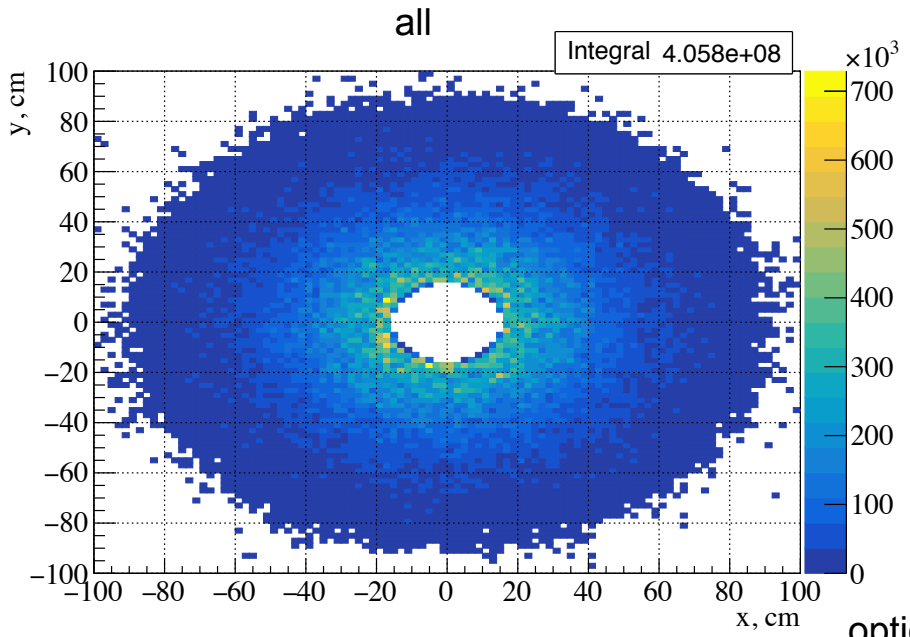
# BH M(e+e-)>1.2 GeV

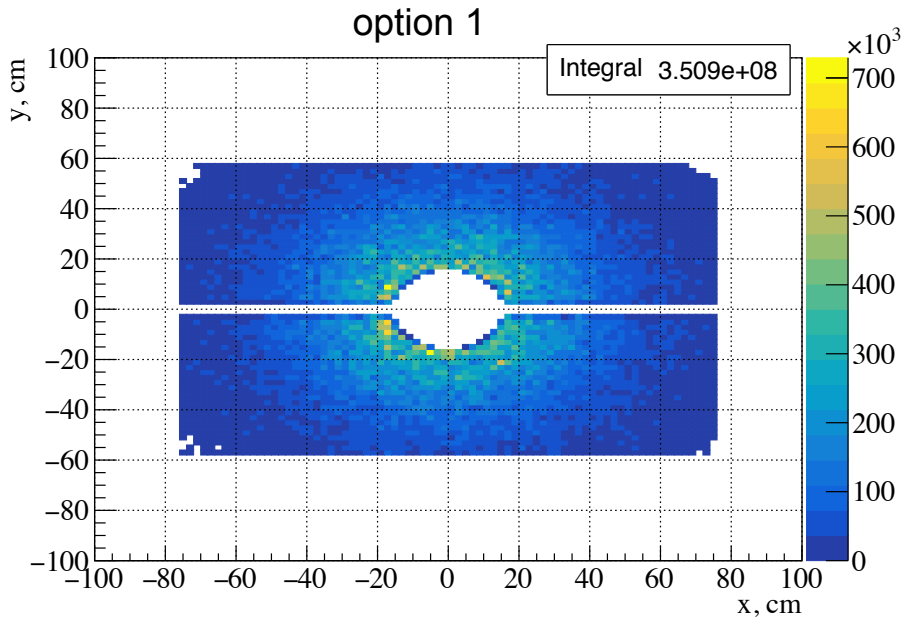

all
Integral 2.153e+09
y, cm
×10^3

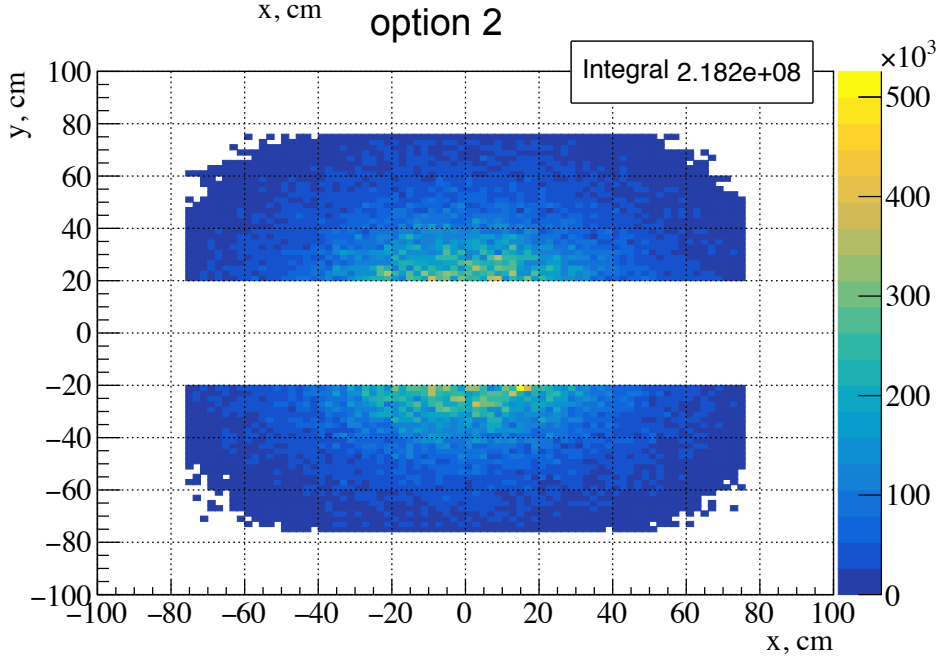

option 1,3
Integral 1.854e+09
y, cm
x, cm
×10^3


option 2
Integral 1.099e+09
y, cm
x, cm
×10^3

# BH M(e+e-)>2 GeV


all
Integral 4.058e+08
y, cm
x, cm
×10^3

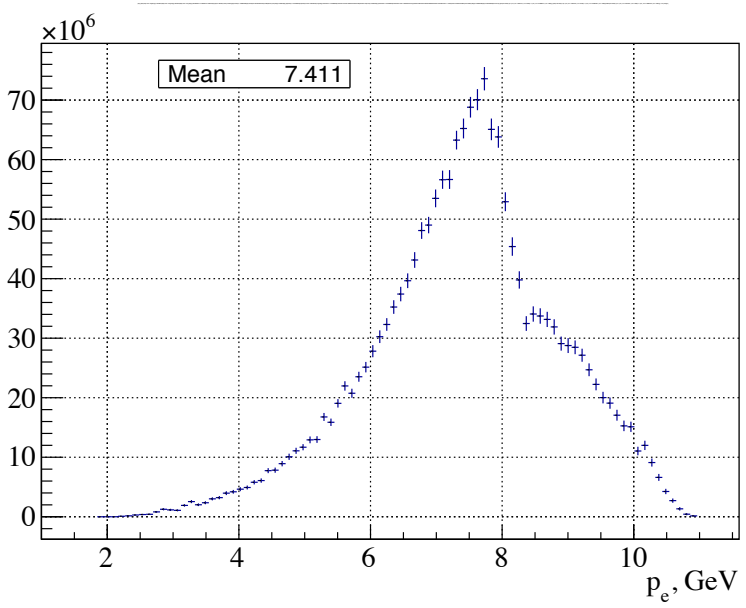

option 1
Integral 3.509e+08
y, cm
x, cm
×10^3


option 2
Integral 2.182e+08
y, cm
x, cm
×10^3

# BH

| | M>1.2 GeV | M>2 GeV |
|---|---|---|
| Option 1,3 | 86% | 87% |
| Option 2 | 51% | 54% |

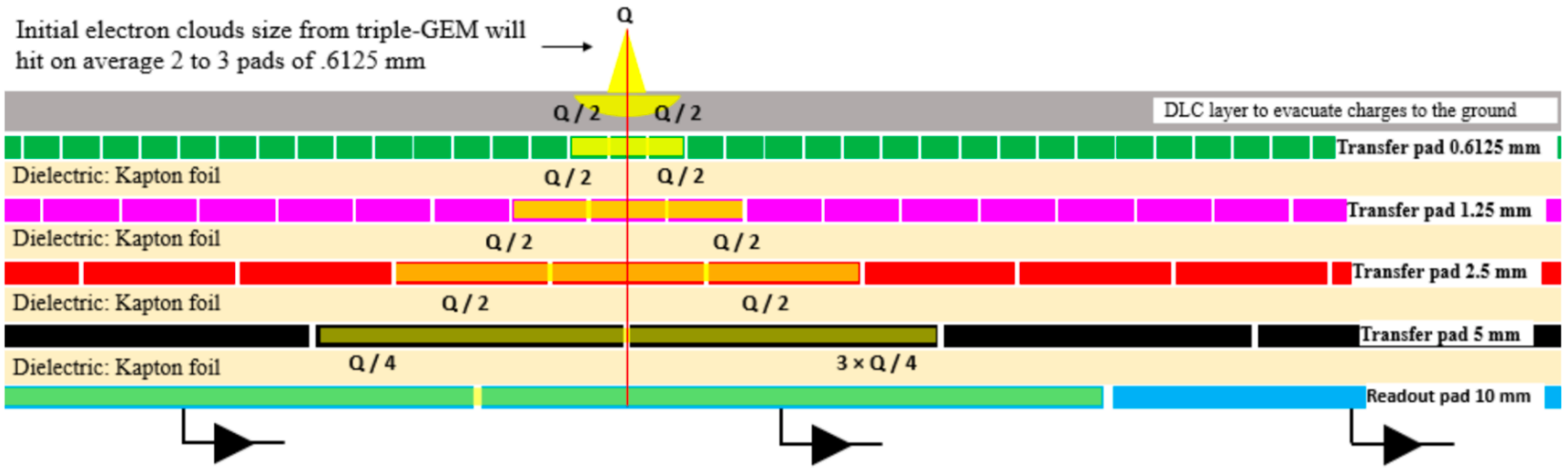
Geometrical efficiency




M(e+e-)>1.2 GeV

# Readout

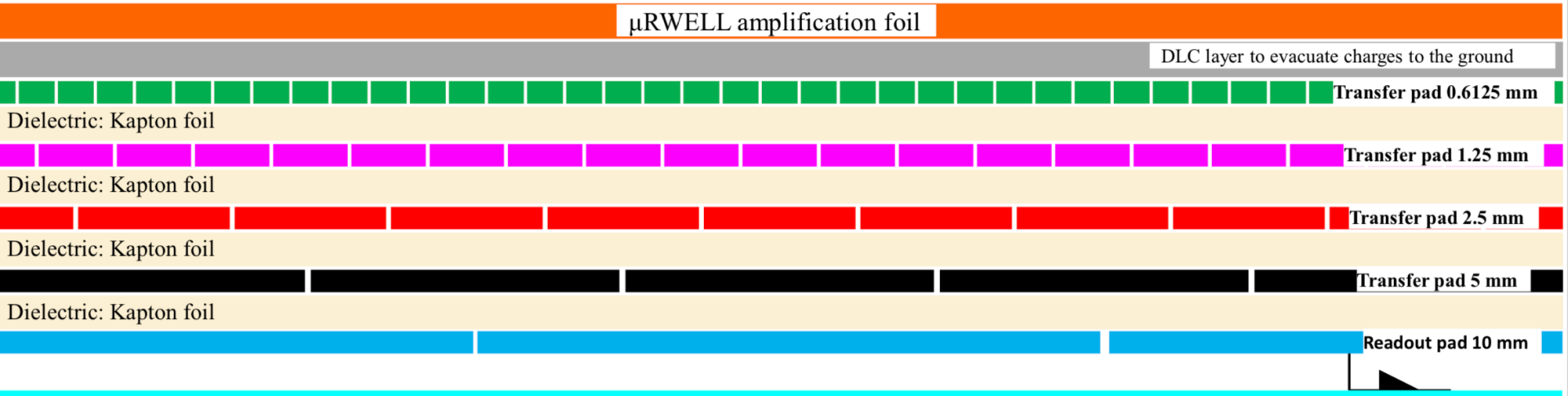
## Basic principle of capacitive-sharing readout




- **Please for now on focus:**
  - More on the charge sharing through capacitive coupling i.e. capacitive- sharing aspect i.e. all the layers except the bottom one
  - not so much on the large pads, the idea equally works for strips (X/Y, U/V and whatever etc …) as well.
  - For GEM-TRD, it will be wiser to go for capacitive-sharing X/Y strip readout (rather than pads)
- **Here:** The DLC layer (resistive layer) serves two purposes:
  - Evacuate charges from amplification structure (μRWELL GEM or whatever)
  - Spread charges on the readout PCB with position resolution
  - But also limit the rate capability

# Readout

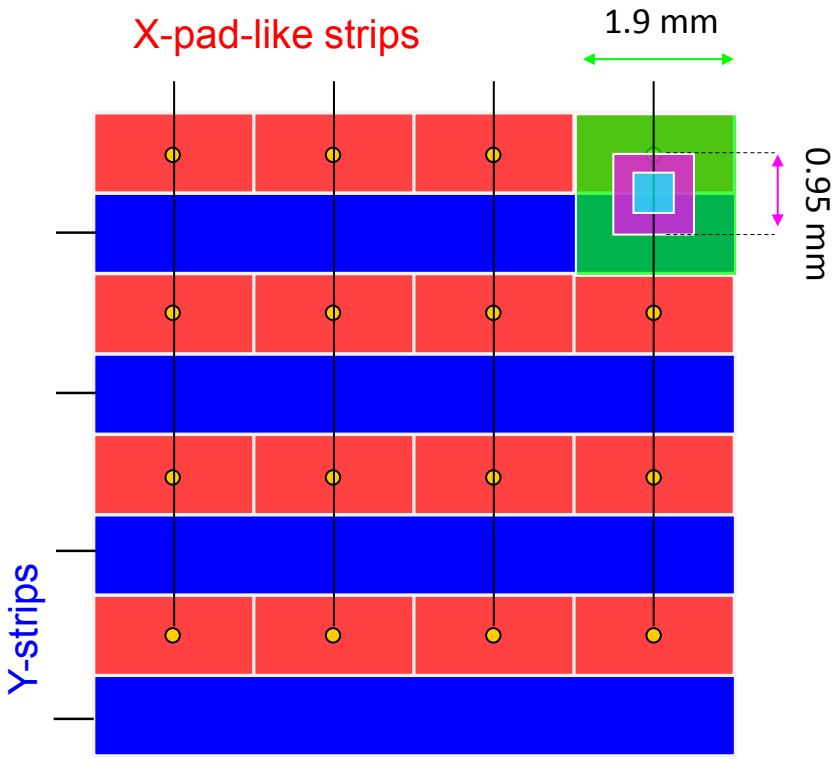
## µRWELL with capacitive-sharing readout

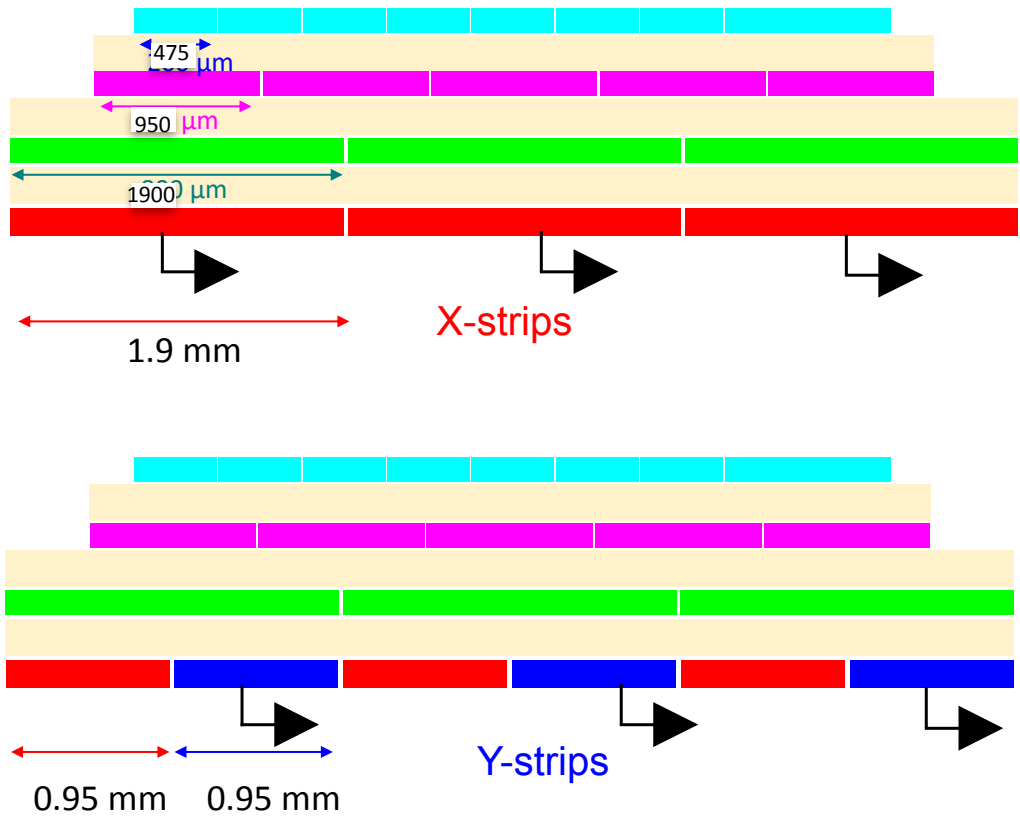



- **Here:** The DLC layer (resistive layer) serves two purposes:
  - Quenches the discharges from the µRWELL
  - Evacuate charges from amplification structure
  - Spread charges on the readout PCB with position resolution
  - But also limit the rate capability

# Readout

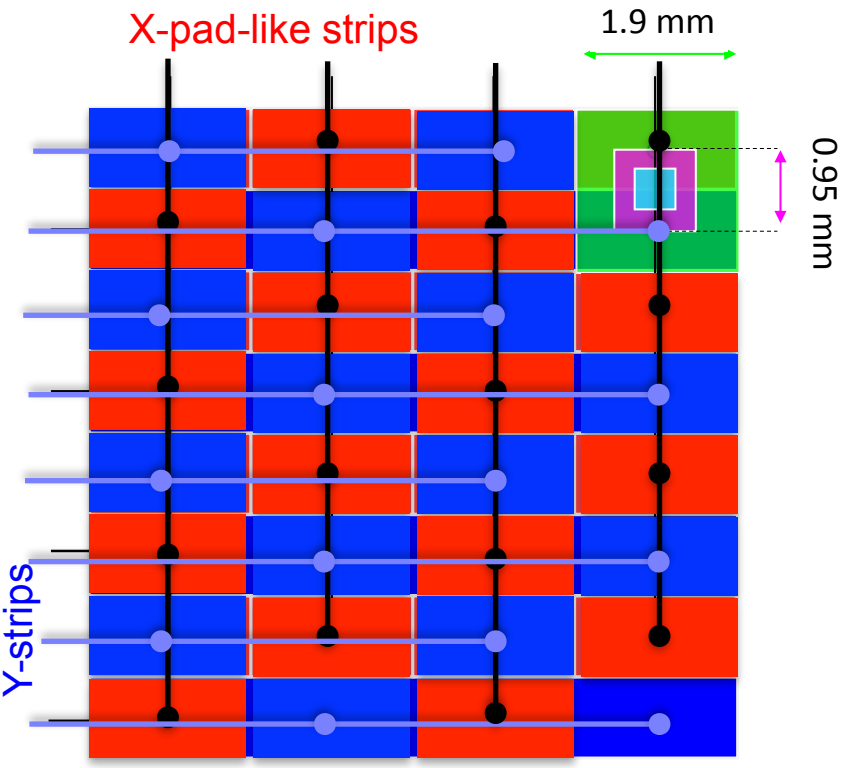
Capacitive-Sharing Large-Strip Readout: Low channel count X-Y strip readout

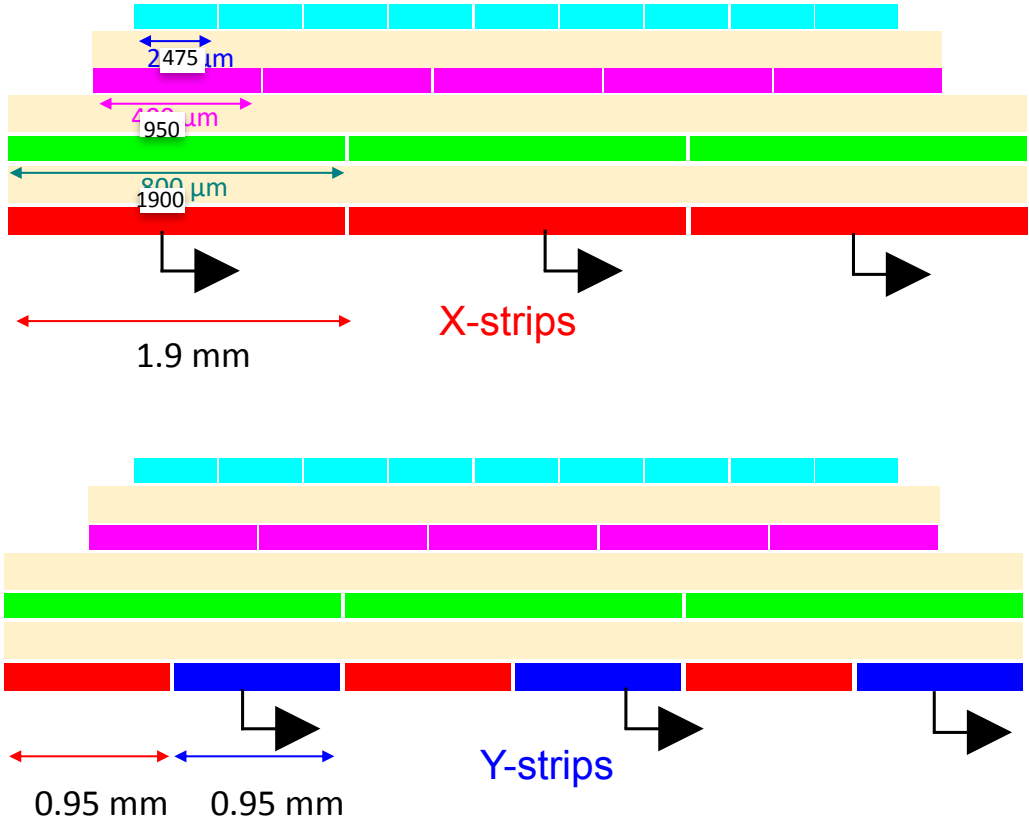


# Readout

Capacitive-Sharing Large-Strip Readout: Low channel count X-Y strip readout



# Readout

The above example has strip pitch of 0.8mm, starting with 0.2x0.2mm^2 pads and two stages of capacitive coupling.
The pitch can be scaled depending on the resolution requirement and budget.
We can start with 0.475x0.475mm^2 pads and after two stages will have 1.9mm strip pitch.

With 1.9mm pitch for one readout block (half chamber):

- vertical strips: 5 fADCs x 3 pre-amps x 24 chan. x 1.9mm = 360 chan. x 1.9mm = 684 mm
- horizontal strips: 4 fADCs x 3 pre-amps x 24 chan. x 1.9mm = 288 chan. x 1.9mm = 547 mm

In total: 648 chan. per readout block, or 2,592 chan. for the whole project.