SYSTEM SPECIFICATIONS DOCUMENT

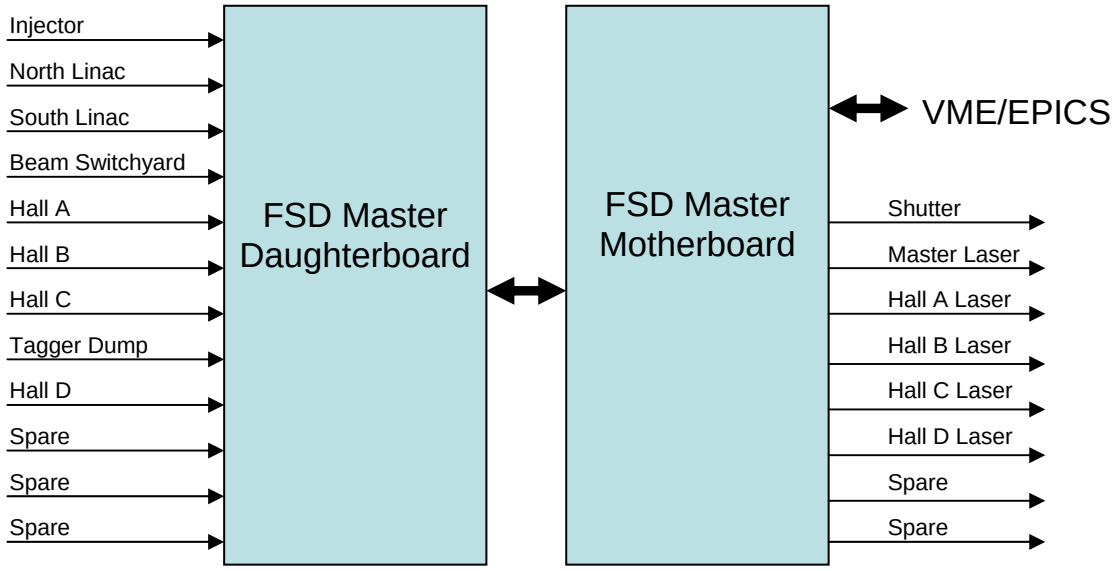
Fast Shutdown Master

Introduction

The Fast Shutdown (FSD) Master Module is located at the top of the FSD tree and is responsible for monitoring the overall FSD signals from all the major CEBAF areas. This will include the Tagger and Hall D FSD signals that will be required as part of the 12 GeV upgrade. It will be possible to mask FSD inputs if they are not applicable to a specific machine setup while other FSD inputs will always be required. If any of the active FSD inputs are faulted then the FSD Master terminates beam by taking away the permissive to the appropriate laser(s) and/or the shutter.

Hardware

The FSD Master Card will take in 12 and output 8 fiber optic FSD signals. It will reside in a VME crate which limits the board size and prevents all 20 required fiber optic connectors from fitting on one board. Therefore, the FSD Master Module will consist of two boards; the FSD Master Daughterboard and the FSD Master Motherboard. A block diagram of the module is shown below with all of the input and output FSD signals.



Hardware Block Diagram

The motherboard will be a full sized VME card that will supply 8 optical FSD outputs on the front panel, takes in the 12 FSD inputs from the daughterboard, use an

Altera FPGA to implement the desired functionality, and provide a VME interface for communication with the EPICS control system. In addition, the motherboard FPGA will drive a LED status light for each fiber optic FSD output and provide 12 signals to the daughterboard for LED status lights. Each output signal will pass through a switch that disables that fiber optic output and loops the signal back to the FPGA using the corresponding LED status signal. This provides an onboard hardware confidence test capability. All the switches will share the same enable signal from the FPGA and that signal will also be passed to the daughterboard.

The daughterboard will be smaller and will stack on top of the motherboard. It will take in the 12 fiber optic FSD inputs from the front panel, convert them to electrical signals, and pass them to the motherboard through a 50 pin connector. The 12 additional signals provided from the motherboard will be used to light status LEDs for each channel. The switch enable signal from the motherboard will be used to switch the receiver hardware from the fiber optic receivers to the corresponding LED status signals. This again provides a loopback confidence check of the hardware.

Firmware

The FPGA on the motherboard will be programmed with the desired board functionality. This includes the VME interface for read backs and controls, detecting FSD signals and driving the appropriate FSD signals, driving status LEDs to indicate valid and invalid FSD signals, and loopback confidence tests for hardware and firmware verification.

The fiber optic FSD inputs and outputs oscillate at 5 MHz when valid and do not oscillate when invalid. The FPGA firmware will detect the edges of the input FSD signals and count until the next edge is detected. If two consecutive edges (rising or falling) of the 5 MHz signal are not detected then the FSD signal will be considered invalid. An invalid input FSD will be latched as such. Both the latched and present FSD status will be provided to EPICS as read backs. The corresponding status LED will be derived from the present status. It will be possible to mask a latched input through EPICS but the present status will always reflect the actual optical input. An EPICS based reset control will be provided to clear the latched status FSD signals.

Optical outputs will be derived from the latched status of the FSD inputs. It will be possible to enabled or disable each FSD output though EPICS. The Master Laser and Shutter outputs will be identical and require that all of the latched FSD input signals are valid. The individual Hall Laser FSD signals will require that the accelerator related FSD signals are valid (Injector, North Linac, South Linac, and Beam Switchyard) as well as the specific Hall FSD signal(s). For example the Hall A Laser FSD output requires that the Injector, North Linac, South Linac, Beam Switchyard, and Hall A latched FSD inputs are valid while the Hall D Laser FSD output requires that the Injector, North Linac, South Linac, Beam Switchyard, Tagger Dump, and Hall D latched FSD inputs are valid. The status of the output FSD signals will be read back through EPICS as well as indicated by the corresponding output FSD status LED.

It will be possible to place the FSD Master Module into a loopback confidence check mode through EPICS. This will cause all the FSD inputs and outputs to be switched from the fiber optic receivers and transmitters to the corresponding LED status signal. All input and output fibers will be hardware disabled in this mode. In the case of FSD outputs, the LED status signal from the FPGA will have to change from an output to an input and thus be a bidirectional pin. The FSD input LED status signals will remain as outputs. There will be EPICS registers used to turn on each FSD input individually or in any combination. This will cause the appropriate LED status lines to be driven with a 5 MHz signal. These signals will loopback through the hardware and firmware and result in driving the appropriate FSD outputs based on how the FSD inputs are setup when the latched inputs are reset. This will allow an automated EPICS application to completely test and verify the functionality of the module as well as allow a user to perform the check manually. The 5 MHz signals can also be verified visually by looking at the flashing status indicators.

Labor and Procurements

Preliminary schematics for the motherboard and daughterboard have been developed and used for procurement and labor estimates. Only one FSD Master Module is required in the accelerator however, a spare module will also be manufactured. The

labor and procurement numbers below represent building two modules and re-spinning the entire design once.

Labor estimates have been divided between electrical engineers, electrical designers (CAD), fabrication technicians, electrical technicians, and computer scientists. The project phases have been defined as follows; creating the PCB schematics, laying out the PCBs, ordering parts and PCBs, PCB soldering/module fabrication, FPGA firmware development, PCB/module testing, EPICS software development, documentation, and field commissioning. The labor and procurement estimates are shown in the table below. All labor is in person-weeks and procurements are in thousands of dollars.

	Elec Eng	**Elec Des**	**Fab Tch**	**Elec Tch**	**Cmp Sci**	**Procurement**
PCB Schematics	3	3				
PCB Layouts		5				
Parts & PCB				2		6
PCB Fabrication			5			
FPGA Firmware	4					
PCB Testing	2			4		
EPICS Software					4	
Documentation	2			2		
Commissioning	2			3		
Totals	**13**	**8**	**5**	**11**	**4**	**6**

Labor in Person-Weeks and Procurements in Thousands of Dollars