

CEBAF Tech Notes

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<p>TITLE</p> <p style="text-align: center;">USER MANUAL FOR FAST SHUTDOWN NODE MODULE</p>	<p>TN # TN-91-042</p> <p>DATE June 18, 1991</p>			
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**User Manual for Fast Shutdown Node Modu**

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## Z0004 Fast Shutdown Node Module

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## **I. Introduction**

### **I.1. Purpose of Circuit**

The Fast Shutdown Node Module is designed to monitor high speed alarm signals and either send a permission signal to the Injector Driver, or remove permission if an alarm appears.

### **I.2. Brief Functional Description**

The fast shutdown system is designed to send a permission signal to the injector driver. When an alarm occurs, it must remove permission within 10 microseconds of receiving the alarm signal.

Each node module monitors all its input alarms and if all inputs are good, it sends a permission signal consisting of a 5 Mhz square optical waveform to the injector driver. If an alarm occurs, it holds the state of the permission signal at the instant it detects an alarm condition.

Each node module consists of a watchdog timer, a CAMAC P1 alarm input, 7 CAMAC P1 inputs, and 7 optically isolated electrical inputs. A readback register is also present to facilitate system startup.

### **I.3. Obvious Extensions of Use**

High-speed, highly reliable interlock systems.

## II. Specifications

### II.1. Minimum User Requirements

- Remove run permission from injector within  $10\mu s$  (overrun)
- Hold fault conditions existing at instant of fault detection
- Send fault reading to computer via CAMAC upon request

### II.2. CDG Extensions to Requirements

- Have an internal timeout to next computer scan.
- Have an internal readback register for system checking.

### II.3. Detailed Specifications Met by Design

#### Timing:

Each node interrupts permission to next level within  $10\mu s$  of removal.

Latches interrupt within  $1.2\mu s$ .

Discriminates between fault inputs more than  $1.2\mu s$  apart.

#### Input requirements:

Timing—an FSD interrupt must remove permission for  $10\mu s$ .

External inputs—5 Mhz  $\pm$  500Khz 12 ma rectangular duty cycle.

Optical inputs—5 Mhz  $\pm$  500Khz optical rectangular waveform  
Packard HFBR 2404 or equivalent with 40%-60% duty cycle.

CAMAC P1 connector input—short to ground through 7 pin.

#### Output signals:

FSD permission—5 Mhz optical waveform with 40%-60% duty cycle.

Auxiliary permission—5Mhz 12 ma waveform with 45%-55% duty cycle.

Watchdog signal—TTL level.

### III. Descriptions

#### III.1. Detailed Functional Description

The CAMAC interface handles communication with the control system, decoding commands and executing appropriate responses. Valid commands are:

Function	Addresses	Action
F0	0	read current status of fault register
	1	read current value in mask register
	2	read current value in readback register
F16	0	no operation, no data transferred
	1	write new mask to mask register
	2	write new value to readback register
F9	0	reset fault, load new fault status into fault registers

(note: two reset commands are required if there are no current faults; the first resets permission, the second clears the fault annunciation registers.)

The input conditioners are 5Mhz detectors which will generate a fault condition if their inputs change substantially from a 5Mhz square wave. There are three classes of inputs: seven fiber optic inputs with connectors on the front panel, seven optically isolated electrical inputs with connections through the rear connector, and the CAMAC P1 bus line from the CAMAC connector. There is finally a fourth fault condition, the watchdog timer, which times computer scans of the module and generates a fault if the computer does not scan within the timeout period.

#### III.2. Required Supporting Resources

CAMAC crate and controller

external fault detection modules (may be other FSD nodes)

#### III.3. Operational Description and Operating Instructions

##### III.3.1 Fault Function Interfacing

The Fast Shutdown Node Module (FSD) has three sets of inputs and one output for fast shutdown operation. There are also internal functions for system integrity checkout.

The first input is the P1 line on the CAMAC bus connector. The FSD module puts on the P1 line a 5 MHz slow transition time trapezoidal waveform from 0V to +5V through a 200 ohm resistor. This line should be shorted to ground using a 7417 or equivalent by functions needing to generate a fast alarm, but having no particular need to signal that they were the first to alarm. Functions alarming on the P1 line MUST respond to subsequent inquiry from the computer that they have an alarm condition.

The FSD module will short the P1 line to ground within approximately  $1\mu s$  of detecting an external fault; functions needing a fast fault signal may monitor this line for early detection of fast category faults, but a module's total loading of the line should not exceed 30pf in parallel with  $10K\Omega$  resistance. Suggested input buffers are 74HC14's (*not* HCT!).

The second category of inputs is the external isolated inputs. These are 7 optically isolated inputs on the auxiliary rear connector which require a 5MHz 0-12ma rectangular current waveform with duty cycle between 45% and 55% for permission to continue. These are intended for functions which must signal themselves as the first fault in a sequence of faults. Functions using the external inputs **MUST NOT** also short the P1 line, since the FSD module will not then be able to determine which fault is first. The FSD module will signal the fault to modules on the P1 line as soon as it detects the fault.

When a fault function detects a fault condition, it must interrupt the output; within two missing cycles the FSD module will detect loss of permission and interrupt its own permission signal to the system. Within two or three more cycles the fault will latch, the first fault registers will be triggered, and the loss of permission will be irrevocable. Note that this implies that a fault signal must be an interruption greater than  $1.2\mu s$  wide; hence the specified requirement of  $2\mu s$  minimum interruption. When the control computer queries the FSD node module, the interrupted signal will be identified as the first fault detected by that FSD module, and the module that interrupted the sequence will be asked for appropriate information regarding the fault.

We must point out that the cable waveform on the external inputs looks strange at first. It is a current waveform into a very nonlinear load (a light-emitting diode), in parallel with a potentially large cable capacitance. Figure V.3.1.1 shows a correctly operating external input on a 20-foot cable in the CEBAF injector. See CEBAF TN-0193 for more information.

The third category of inputs is the optical inputs on the FSD module's front panel. These inputs are intended as inputs from other FSD nodes; however, since all inputs are not likely to be used, a few may be available in some crates for fault function use. They require a 5MHz optical rectangular waveform with 45% -55% duty cycle. Suggested fiber optic transmitters are the Hewlett-Packard HFBR-1412 series. Fault detect criteria are the same for these inputs as for the external isolated inputs. In particular, functions using these inputs **MUST NOT** also short the P1 line, since the FSD module will not then be able to determine which fault is first. The FSD module will signal the fault to modules on the P1 line as soon as it detects the fault.

### III.3.2 Timer setup

The watchdog timer is used to monitor control system operation. When the control system scans the FSD module, the timer is reset to the value programmed into the timer switches and starts counting down toward zero. If it reaches zero, that is considered a fault and the fault detector shuts down the beam. If the system scans the module before the timer

reaches zero, the timer is reset to the programmed value, and the count starts over. Any control system access at all to the module resets the count.

The timer operates with a power of two resolution. This allows a wide range of timeout settings with relatively few required settings. If a specific time to failure can be identified, set the timer for less than that time.

Otherwise, set the timer for several times the expected scan period. It may be necessary to experiment with several settings to find a timeout that will reflect a true system failure without tripping occasionally due to computer load variations.

The following table gives timeout values for each switch setting.

Hex Switch Value	Timeout
0	6.55ms
1	13.1ms
2	26.2ms
3	52.4ms
4	104.8ms
5	209.6ms
6	419.2ms
7	838.4ms
8	1.677s
9	3.354s
A	6.707s
B	13.41s
C	26.83s
D	53.66s
E	107.32s
F	214.6s

### III.3.3 Programming

The node module software structure follows:

Address A0:	Fault Register
F16:	write {any 16-bit word}—No operation has no significance.
F0:	read {16-bit word}
	after fault: first fault sensed
	after reset (F9): current fault status
F9:	Reset fault and reload fault register.
Address A1:	Mask Register
F16:	write {16-bit word}—set mask bit for
F0:	read {16-bit word}—read current mask
Address A2:	Readback Register
F16:	write {any 16-bit word}
F0:	read {last written word}

#### Channel & mask assignment:

bit 0:	Watchdog Counter
1-7:	Fiber Optic Inputs
8-14:	Isolated External Electrical Inputs
15:	CAMAC P1 line

There are some considerations to note in programming the node will not latch or recognize new faults coming after a fault trip. while a node is tripped, the new fault will never be seen. This will be understood.

Second, since new faults are not latched while a node is tripped, until the node module is reset (F9 A0). When a node is reset, status into its fault registers. Note that the order of occurrence will be determined. If there are new faults, the node does not pass permission.

Finally, resetting a node consists of sending a CAMAC reset command (F9 A0). If all inputs have a valid permission signal or their channels (that is, there are no unmasked faults), the module will pass permission of the fault tree, and will be armed for subsequent fault trips. If no permission signal, the fault is loaded into the fault registers and passed to the next level. *Permission cannot be passed up until all unmasked faults are cleared.* that if there are no current faults, it is necessary to reset twice: the first time is to get permission, but does not reset the fault annunciation registers. The second time will reset the registers.

## IV. Theory

### IV.1. Functional Block Diagram Theory

#### IV.1.1 Overall Block Diagram Theory

The Fast Shutdown Node Module (FSD Node) consists of three sections: the CAMAC interface, the input conditioner and fault detectors, and the permission logic section. However, an introduction to the intended use of the module is required to understand the functions accomplished.

Figure Z0004B01 is the system block diagram of a hypothetical system built using these FSD node modules. Fault detector modules for beam loss, fast valve signalling, and other fault conditions feed into FSD node modules, which feed into the injector and the computer control system by different paths. This allows faster shutdown than with the computer alone, and allows better and easier fault tracing than possible with a strictly hardwired system. The FAST INTERRUPT LOGIC portion of the diagram is the province of the FSD node module.

Diagram Z0004B02 shows the arrangement of the FSD logic part of a FSD system. The nodes are intended to be connected in a tree structured configuration, with fault detecting modules as the leaves of the tree. Note three considerations in setting up a FSD tree:

1. The total propagation delay through the tree is proportional to the number of levels. The number of nodes in a level has no effect on delay.
2. Each node is built to accept 7 subtrees and 7 external fault detection inputs. Thus, a given node can handle up to 56 faults with a single lower level, and discriminate within about  $1.2\mu s$  which was first.
3. Only external inputs are discriminated in time to within about  $1.2\mu s$ . P1 inputs within a crate are indistinguishable from one another; if a second P1 fault occurs before the control system reads the node and its crate's status, there is no way to determine which fault occurred first.

#### IV.1.2 Node Module Block Diagram Theory

Figure Z0004B03 is the block diagram of the FSD node module. The four classes of fault inputs feed into the fault registers and the fault detect logic by different paths. Each individual signal goes into the registers on its own separate signal line; the 15 external signals go into the fault detector as a common fault sum. Signal conditioning for the external signals permits detection of a fault in either failed- high or failed-low conditions.

The internal watchdog fault is a simple TTL signal with low=ok, high=time expired. It is generated by a programmable timer, programmed in powers of two by DIP switches on the module PC board.

The fault detect logic monitors the condition of all the inputs via the fault sum line, and if any one loses its permission signal it removes permission to the next level. It latches any input faults until explicitly reset by the CAMAC interface.

The CAMAC interface allows users to set up the operating environment of the module. It permits masking by setting bits in the mask registers, and reading and resetting of current faults. The CAMAC interface never participates directly in the fault detection/shutdown process.

## IV.2. Detailed Circuit Theory

### IV.2.1 CAMAC Interface

The CAMAC interface (drawing Z0004D01) mediates communication between the control system and the independent FSD interlock system. It contains the registers that hold the FSD interlock and mask states, and allows the computer to modify these states. It is important to note that the control system does not participate directly in the interlocking: it only sets up the environment in which the interlock system operates.

The command decoder U12 decodes the function codes and addresses with which the control system communicates with the FSD system. It is a programmable logic device; its program is listed in section V.5.2. This program is also available on the CEBAF computer system in file user1:[jperry.abel]z0004.abl. For programming new devices download z0004.jed to the programmer.

The fault registers are manipulated through address A0. They may be read at any time to get the current state of the registers; what is in them, however, depends upon the fault state of the fault detector, which is described in section IV.2.3. The value in the fault registers is gated onto the CAMAC read bus by the CAMAC read command (F0).

There are two ways to load the fault registers. First, if the module is not already in a fault condition and it detects a fault, the fault detect signal goes to the command decoder's FDET input. Second, a reset command (F9) may be sent to address A0. The command decoder has a fault detect input to allow it to both pass through a detected fault from the fault detect circuitry, and reset (or update) the fault registers when a reset command is sent to address A0.

The mask registers are manipulated through address A1. They may be read at any time to verify the actual state of the masks, and they may be written at any time to inhibit the operation of any fault input. The mask register section consists of three pairs of registers: the mask, mask backup, and the mask status registers.

The mask and mask backup registers are part of the high reliability path in the FSD system. Each pair contains the same information, and they drive separate mask switches in the input conditioning sections. These mask switches are described in section IV.2.2.

Since the mask registers must always be active, their output controls are tied to ground and a separate pair of latches is used to gate the current mask state to the read bus when the command decoder detects a READ MASK command (F0 A1). These latches have their input gates permanently tied high so they follow the mask register states faithfully, and their outputs are controlled by the command decoder.

The readback registers fulfill a system integrity function for the control system; they simply latch whatever is on the data lines when a write command is sent to them (F16 A2). The control system then reads back this value by sending a read command (F0 A2).

#### IV.2.2 Input conditioners

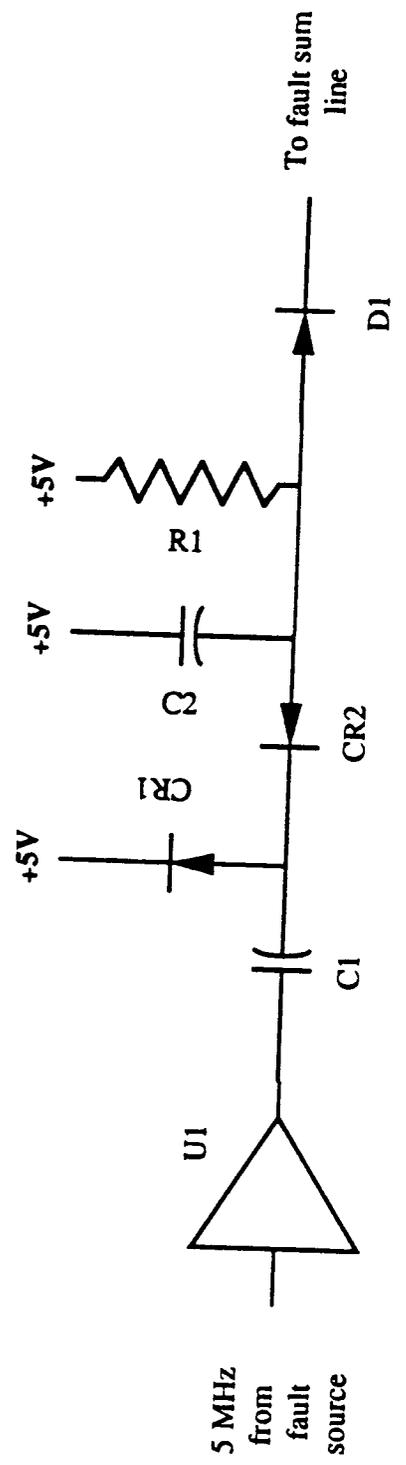
The input conditioners detect permission or its absence from a number of inputs, and send the permission state to the fault detector. There are 15 user-oriented inputs for which the input conditioners serve, and the watchdog timer, which is connected directly to the fault detector, and will be described there.

The input conditioners all have identical decoding circuits, so only one will be described here. The differences are in the external connections, which for the optical inputs are via fiber optic receivers, and for the external permissions are optoisolators. The input to the permission decoders is in all cases a 5 Mhz rectangular wave. Of interest may be the set of correct waveforms shown in figure V.3.1. These waveforms are taken from correctly operating FSD node modules.

The permission decoders operate by transferring charge from a series capacitor to a parallel one at a high enough rate to keep the permission node's voltage below the logic threshold of a CMOS gate in the fault detector. Consider the idealized circuit in figure IV.2.2.1. The input buffer squares up the input waveform, giving sharp logic transitions for the following circuitry. Capacitor C1 blocks DC so that if an input signal fails low, it cannot hold the permission decoder in the permissive (low) state. It also acts as a charge collector for the decoding circuitry. The charge collection is as follows: on the positive transition of the permission waveform, the Schottky diode CR1 conducts, draining from C1 any charge and clamping C1's voltage to a maximum of 0.25V. CR2 opens very quickly to keep from draining any charge from the permission holding capacitor, C2. C2 is now being discharged through R1 to the +5V supply. The time constant is  $2.5 \times 10^3 \times 150 \times 10^{-12}$ , or 375 ns.

When the negative transition arrives, C1 is pulled down to ground, and CR1 switches very fast to the nonconducting state. CR2 conducts, permitting C1 to influence the permission node. R1 is now charging C1, but C1 is also injecting charge into C2, causing the voltage across C2 to increase, pulling the permission node's voltage toward ground. The voltage at the permission node is a function of the charge drained constantly to +5V by R1, the charge (which comes from R1 and C2 through CR2) being dumped from C1 through CR1, and the ratio of charge divided between C1 and C2.

If permission pulses come into the circuit at a constant 5Mhz rate, the permission node voltage stabilizes between 1V and 2V. If the permission pulses stop, leaving the output



of the buffer high, R1 charges C2 through +2.5V (the threshold of the fault detect gate), removing permission within about 400ns. If the pulses stop, leaving the output of the buffer low, R1 charges C1 and C2 in parallel, removing permission within about  $2\mu s$ . Figure V.3.1.2 gives a detailed picture of the voltage on a permission holding capacitor (C2); figure V.3.3 shows a fault occurrence.

Junction diode D1 prevents the 15 permission nodes interfering with one another. If any node goes high, its D1 will conduct and all others will open, keeping their permission nodes from holding the permission sum node down. Figure V.3.1.4 gives a detailed picture of the voltage at the sum node; figure V.3.5 shows a fault occurrence.

The practical circuit (see drawing Z0004D03, the bottom branch) is slightly modified for reliability and monitoring features. The basic structure of the ideal circuit is clear; the additions enhance failure tolerance. The correspondence between idealized components and practical components is:

practical	ideal	purpose
U22b	U1	input buffer
C74	C1	transfer capacitor
CR31	CR1	dump switch
CR32	CR2	transfer switch
C71	C2	permission holding capacitor
R120, R121	R1	permission drain resistor
R119, R122	(not ideal)	test point resistor
R123	(not ideal)	sum node resistor

U22b section 3 corresponds to the input buffer; it drives C74, the input blocking and charge transfer capacitor. CR31 corresponds to CR1; CR32 corresponds to CR2. C71 is the permission holding capacitor C2 and R120, R121 are the charge draining resistor R1. R1 is doubled in the practical circuit because if it opens, there is no way to pull C2 over the permission threshold. D67 and D68 correspond to D1; they are doubled to prevent a single-device failure from keeping a high permission node voltage from the fault detector. R119, R122 allow testing procedures to determine easily if one of the parallel diodes is failed. R123 provides a safe high resistance path to the fault detector so that if all inputs are either permitted or masked, the parallel equivalent of  $160K\Omega$  will pull the CMOS fault detect gate input down. However, if even one input goes high, it will overwhelm the  $\approx 150K\Omega$  left and pull the permission sum up through the threshold.

The mask branch (Q36, Q37, SW6c) allows the module to ignore unused or noncritical failed inputs by shorting the permission node to ground. Since either transistor alone would cause a potentially catastrophic failure if it failed as a short, it is doubled in series, so that both must be shorted simultaneously to cause a spurious permission condition. Note that the mask registers from the CAMAC interface section are also doubled for the same reasons.

Finally, the line from the permission node to the fault comparator U28 allows the CAMAC interface to determine the state of the node for reporting to the control system.

All the external permission inputs work in exactly this fashion. The P1 line, however, is also an output: it is a copy of the permission signal from the fault detector. When the fault detector detects a fault from another input, it clamps the P1 line to ground. This should be kept in mind when dealing with the P1 line input or output. Since the P1 line is faulted whenever the module is in a fault condition, one should not expect to see a P1 signal except when the module is clear, and one should expect a P1 signal then unless the output is disconnected.

### IV.2.3 Fault detector

The fault detector, drawing Z0004D02, monitors all the possible fault sources and removes permission to the next level if any one of them loses permission from its source and is not masked. The key component of the fault detector is the fault gate, U6a. It is a 74HC4002 dual 4- input NOR gate. The HCMOS series gates have a fairly accurate threshold of  $\frac{V_{CC}}{2}$ , which is about 2.5 volts for this circuit.

The fault detector is connected to a 5Mhz gate oscillator, U5a, U5b, U5c, which is set by R11 and C9 to oscillate at about 5Mhz. This pulse train comes to the fault gate on pin 2, and is passed on to the output fiber optic transmitter, U30, through driver Q1, if all other pins are LOW. If any other pin goes and remains HIGH permission is removed from the transmitter, since the fault gate output is held LOW. The output permission signal is also sent out to local users who may need it through buffer U13a.

The pulse train also goes to the P1 line driver, Q6-Q7, which drives the CAMAC P1 line through resistor R34. This signal goes onto the CAMAC backplane bus, and is detected as an input by the input channel starting at U3b pin 17 on drawing Z0004D04 (the bottom branch). See the description in section IV.2.2 above for details of its operation. If any fault is detected, the output to the P1 line is shorted to ground by Q5, sending a signal to any other module that monitors it that permission in the local area is removed. That is, the P1 line functions both as permission input if the input conditioner is not masked, and as a fault signal to other modules in the CAMAC crate if switch SW1 is closed. If more than one FSD node is in a crate, SW1 must be opened on all but one of them to keep them from interfering with one another.

Finally, the 5Mhz pulse train goes as a clock to the watchdog timer U4. Whenever a CAMAC command of any type is sent to the command decoder, the decoder sends a pulse to the timer pin 11, clearing the count. If too long a delay elapses between commands, the counter reaches its limit and its Q output pin 7 goes HIGH. This puts a HIGH level on pin 3 of the fault gate, removing permission (since the output can no longer follow the pin 2 input), and setting a HIGH level on the input pin 2 of the CAMAC fault register U17. There is an auxiliary output which also sends the watchdog signal through U5d, U13b to other users who may need it. The timer is set by switches SW2a-d. The programming

times are listed in the Maintenance section V.

All the external inputs, 7 optically isolated, 7 fiber optic, and 1 P1 input, are summed onto the fault sum bus pin 4 of the fault gate. The fault sum is pulled down only if all 15 inputs are low (whether by permission or by mask). Inputs which are low pull the fault sum bus down through the  $10M\Omega$  resistors shunting the logic diodes. Note that there is no other path to ground from the fault sum. If any fault node goes positive, its diode conducts, overwhelming the  $10M\Omega$  resistors of the other channels, and pulls the fault sum through the threshold of the fault gate.

The other half of the fault gate chip, U6b, is used as a strobe generator for the CAMAC fault monitoring circuitry. If the fault sum or watchdog timer go HIGH, its output goes LOW, enabling the input channel fault comparators U20, U21, U28, U29 (drawings Z0004D03, Z0004D04). This output is also inverted by U5e and used to signal the CAMAC decoder that a fault has occurred. The decoder then strobes the fault registers U17, U25 (drawing Z0004D01), which get their input data from the fault comparators. The voltage level for the comparison is set by resistors R125, R126 (drawing Z0004D03) to approximately 2.25V to insure that any channel that is over the fault gate's threshold is detected as a fault.

The required fault latching function is performed by the signal decoding branch connected between the output pin 1 and the last input pin 5 of the fault gate U6a. The output of the fault gate is buffered by the bus driver U22b, and decoded by an input signal conditioner. If the output signal stops, the decoding network charges to +5V, holding the output down. It is then necessary to send a reset command to the module to permit the fault gate to continue. Q4 is the reset switch for the latch feedback; Q2-Q3 is the reset switch for the input, doubled for reliability.

The function of Q2-Q3 is to allow the module to reset and load secondary faults in case of multiple faults. Without Q2-Q3, there would be no way to re-strobe the fault latches in the case of secondary fault conditions, since U6b would not be able to change state.

U13a, U13b, and U5d provide output signals for external use in local areas. U13a buffers the node's permission signal so that local users can monitor the local status of the FSD system for their own purposes. Note that only the status available is that of the node itself and any subtrees connected; the overall system status is not available unless the node being monitored is the FSD Master node.

U5d and U13b invert and buffer the watchdog timer signal for external use. This signal is LOW unless the timer has tripped; it is HIGH if the timer is tripped.

#### IV.2.4 Power Distribution

See drawing Z0004D05. Power is distributed to the module from the CAMAC bus connector. Since neither +6V nor -6V are used in the circuit, but all components require  $\pm 5V$ , the CAMAC  $\pm 6V$  supplies are reduced to about  $\pm 5.3V$  by diodes D72, D73, D71. Fuses

F1 and F2 protect the CAMAC crate power supply from short circuit faults which may occur within the module.

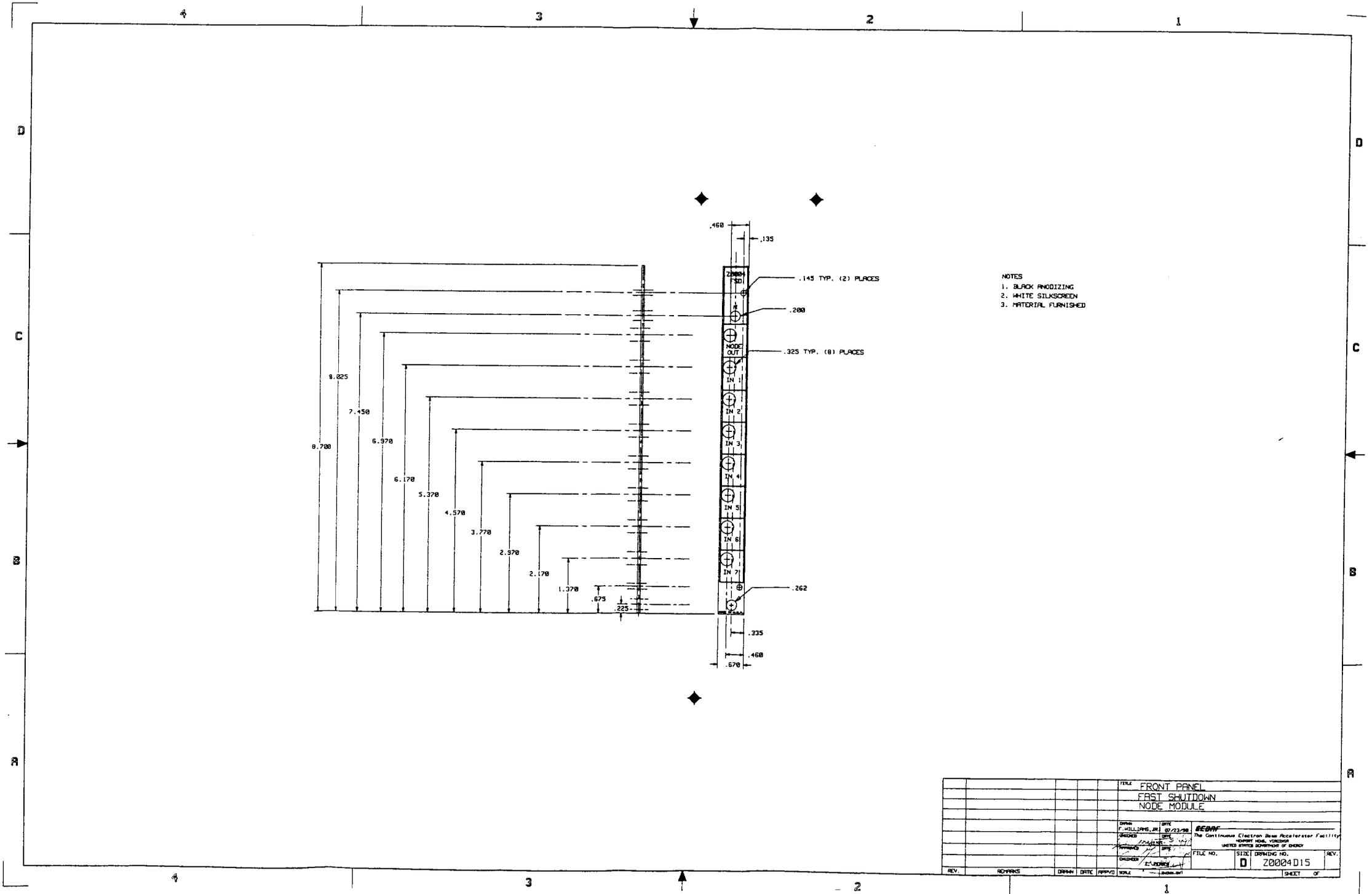
The two electrical connectors are also detailed on the power distribution sheet.



DRAWING NUMBER  
Z0004D15

DRAWING NUMBER  
Z0004D15

DRAWING NUMBER  
Z0004D15



NOTES  
1. BLACK ANODIZING  
2. WHITE SILKSCREEN  
3. MATERIAL FURNISHED

REV.	NO.	DATE	BY	APP'D	SCALE	DATE	FILE NO.	SIZE	DRAWING NO.	SHEET	OF
									Z0004D15		

FRONT PANEL  
FAST SHUTDOWN  
NODE MODULE

DRAWN: J. WILLIAMS, JR. DATE: 07/23/58  
CHECKED: DATE: 5/1/59  
DESIGNED: E. J. JONES  
The Continuous Electron Beam Accelerator Facility  
DEPARTMENT OF ENERGY  
UNITED STATES GOVERNMENT OF ENERGY

## V. Maintenance Information

Maintenance consists of verifying operation of each of the critical paths of the FSD module. There are no adjustments to be performed; however, repair may be required to correct malfunction.

### V.1. Overall Interface Response

#### V.1.1 Readback Register Operation

Write a value of zero to address A3. Read A3: the value must be zero. Write a value of  $FFF_{16}$ . Read A3: the value must be the same.

#### V.1.2 Mask Register Operation

This procedure checks operation of each mask bit and its backup.

Write a value of zero to address 1. Check with a voltmeter each of the 31 test points listed in the following table. Every output must be zero (TTL low). Write  $FFF_{16}$ . Every output must be 1 (TTL high). Following is a table of test points for each mask bit.

BIT	TEST POINT	BIT	TEST POINT
0	U4 pin 5	8	R95, R96
1	R56, R57	9	R97, R101
2	R61, R62	10	R103, R104
3	R67, R68	11	R106, R107
4	R73, R74	12	R111, R112
5	R76, R77	13	R114, R115
6	R78, R79	14	R117, R118
7	R84, R85	15	R87, R88

#### V.1.3 Fault Register Operation

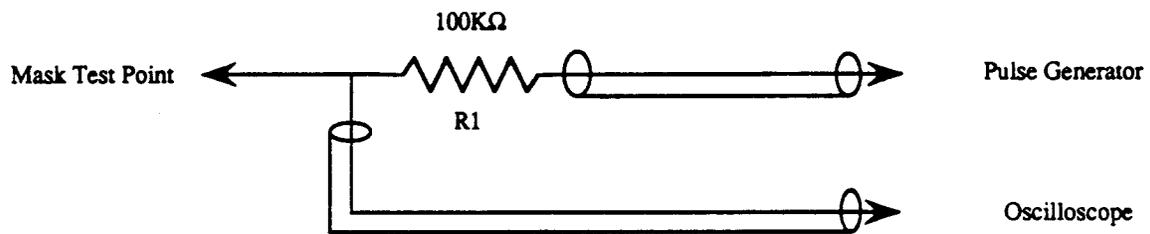
Clear all masks. Remove permission from all inputs. Reset the module and read the fault status (F0 A0). Every bit except the most significant (the watchdog line) and the least significant (CAMAC P1 input) must be set. The watchdog line will be reset by the computer access required to read the faults. The CAMAC P1 fault only occurs for external shorts to ground. The watchdog check is addressed in section V.4.

Short pin 1B of the CAMAC connector to ground. The fault register should now read the least significant bit set with the others.

Mask all inputs. Reset the module twice. Every bit must be clear.

## V.2. Mask Function

Clear all masks and remove all test pulses. Verify that the output of each of the 30 mask registers is TTL low. Connect the mask probe (fig. V.2.1) to each test point. The scope trace should be clean in both the high and low transitions. There should be only a slight increase in the rise and fall times from the square wave input of the probe to the output, and the signal should not be loaded down. Read the fault registers with the computer; all channels should be faulted.

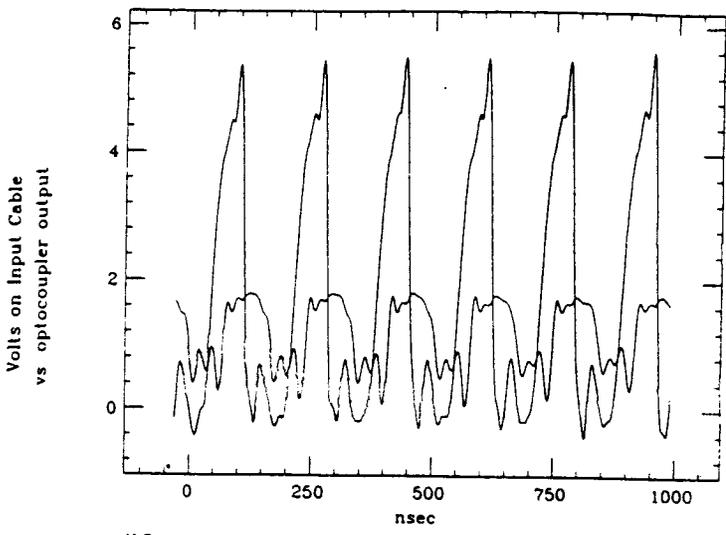


**Figure V.2.1 Mask Probe Schematic**

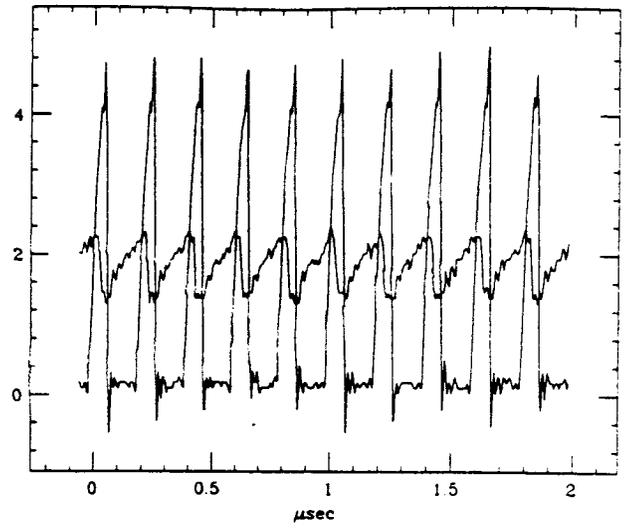
### V.3. Fault Decoder Operation

Clear all masks. Put the pulse generator signal into the FSD Test Box. Send the test box output to fiber optic input 1. Monitor the voltage on the anode of CR18. The signal must conform to waveform 2 in fig. V.3.1. The following table gives input versus test point for each input signal conditioner of the module.

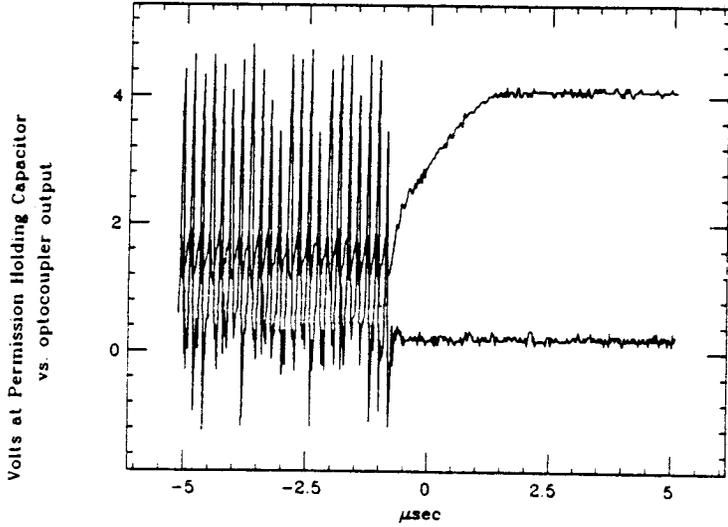
Input	Test Point
Fiber Optic Input 1	anode CR18
Fiber Optic Input 2	anode CR22
Fiber Optic Input 3	anode CR24
Fiber Optic Input 4	anode CR26
Fiber Optic Input 5	anode CR28
Fiber Optic Input 6	anode CR30
Fiber Optic Input 7	anode CR32
P2-1A	anode CR3
P2-3A	anode CR4
P2-5A	anode CR7
P2-7A	anode CR8
P2-9A	anode CR10
P2-11A	anode CR16
P2-13A	anode CR12
P1-1B	anode CR14



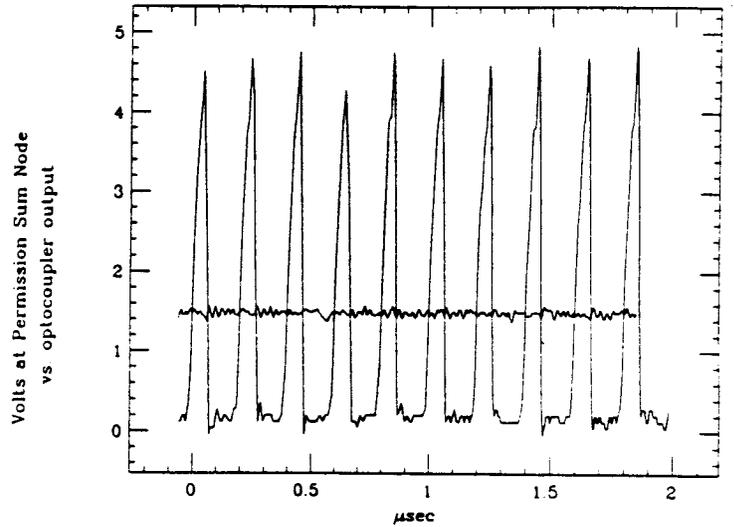
V.3.1.1. Correctly Operating External Channel  
C:\TEK\INP-16.TOP, 05-20-1991



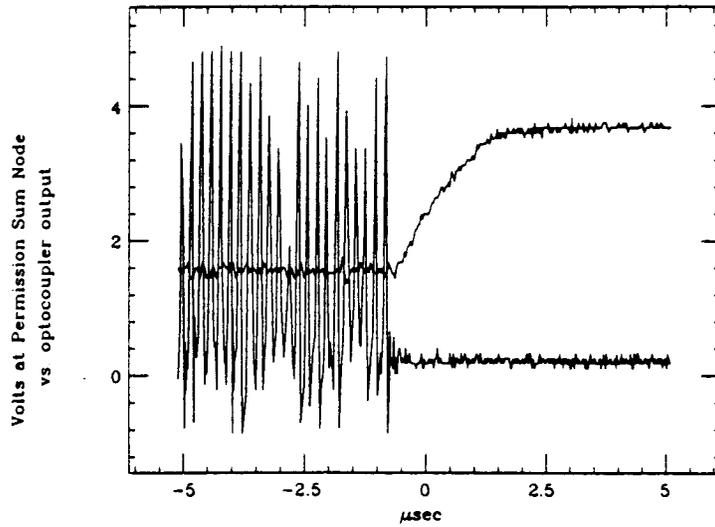
V.3.1.2. Correctly Operating Input Channel  
C:\TEK\FSD-4.TOP, 04-12-1991



V.3.1.3. Input Channel (Optical, External, or P1) Detecting Fault  
C:\TEK\FSD-10.TOP, 04-12-1991



V.3.1.4. Correctly Operating Inputs  
C:\TEK\FSD-6.TOP, 04-12-1991



V.3.1.5 Correctly Operating External Fault Channel  
C:\TEK\FSD-8.TOP, 04-12-1991

### V.3.1 Correct FSD Node Waveforms

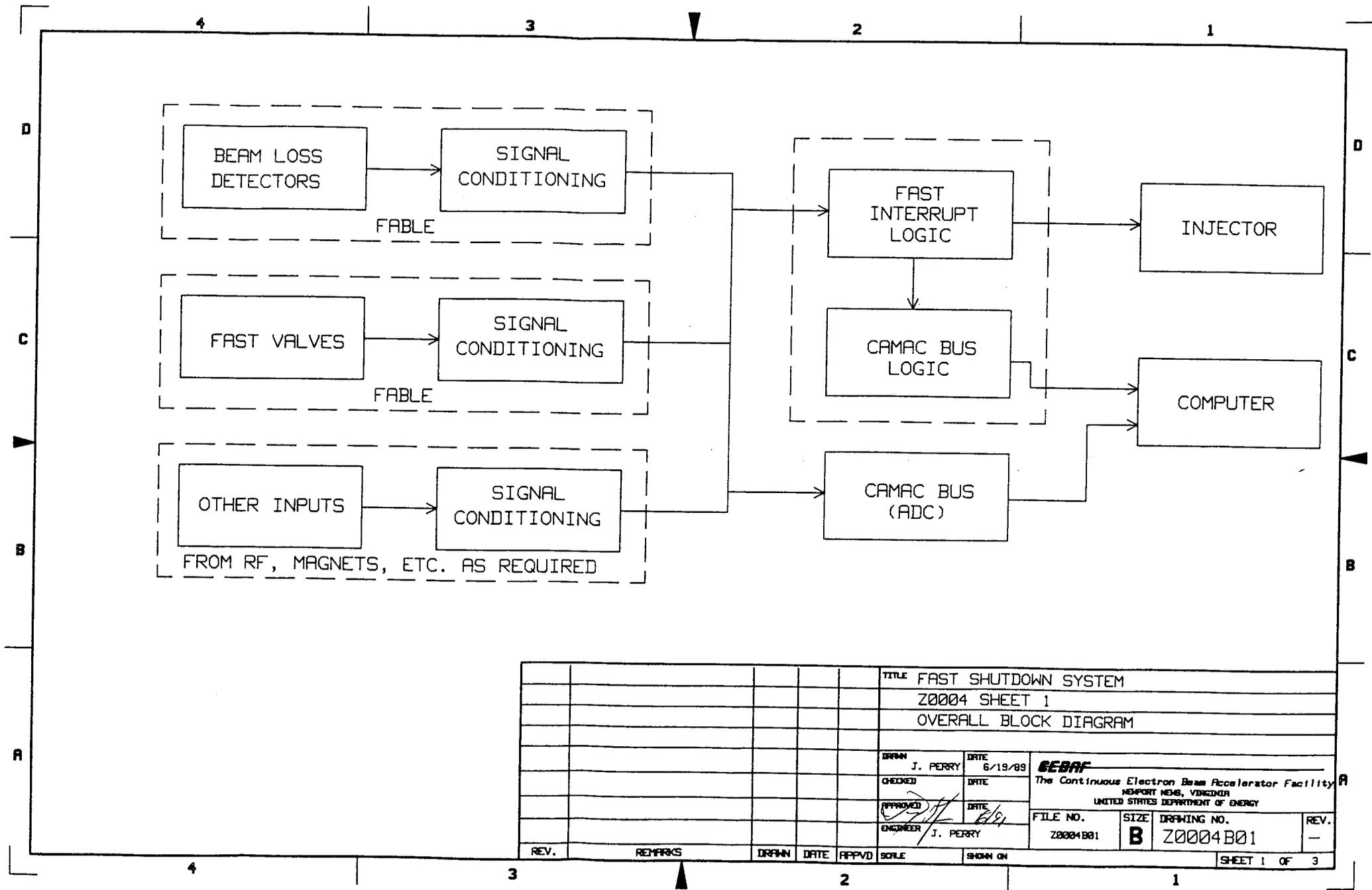
#### V.4. Watchdog Timer Operation

Attach the scope probe to the reset input and the Q<sub>0</sub> computer to read any address once upon command. The vs. input at each slot access. Set each timer switch in tu check the timeout according to the following table.

Hex Switch Value	Timeout
0	6.55ms
1	13.1ms
2	26.2ms
3	52.4ms
4	104.8ms
5	209.6ms
6	419.2ms
7	838.4ms
8	1.677s
9	3.354s
A	6.707s
B	13.41s
C	26.83s
D	53.66s
E	107.32s
F	214.6s

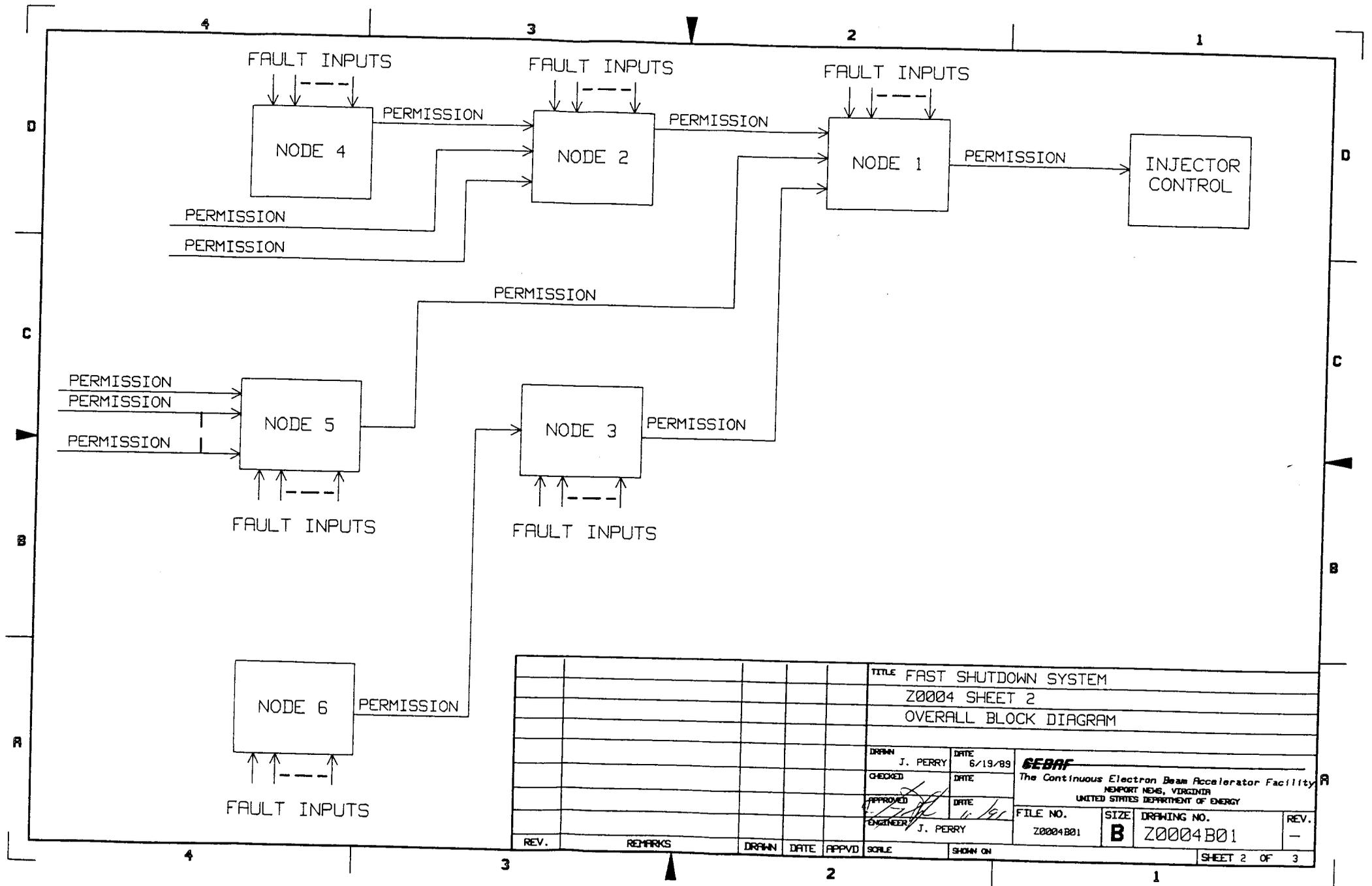
## V.5. Layout

1 OF 3

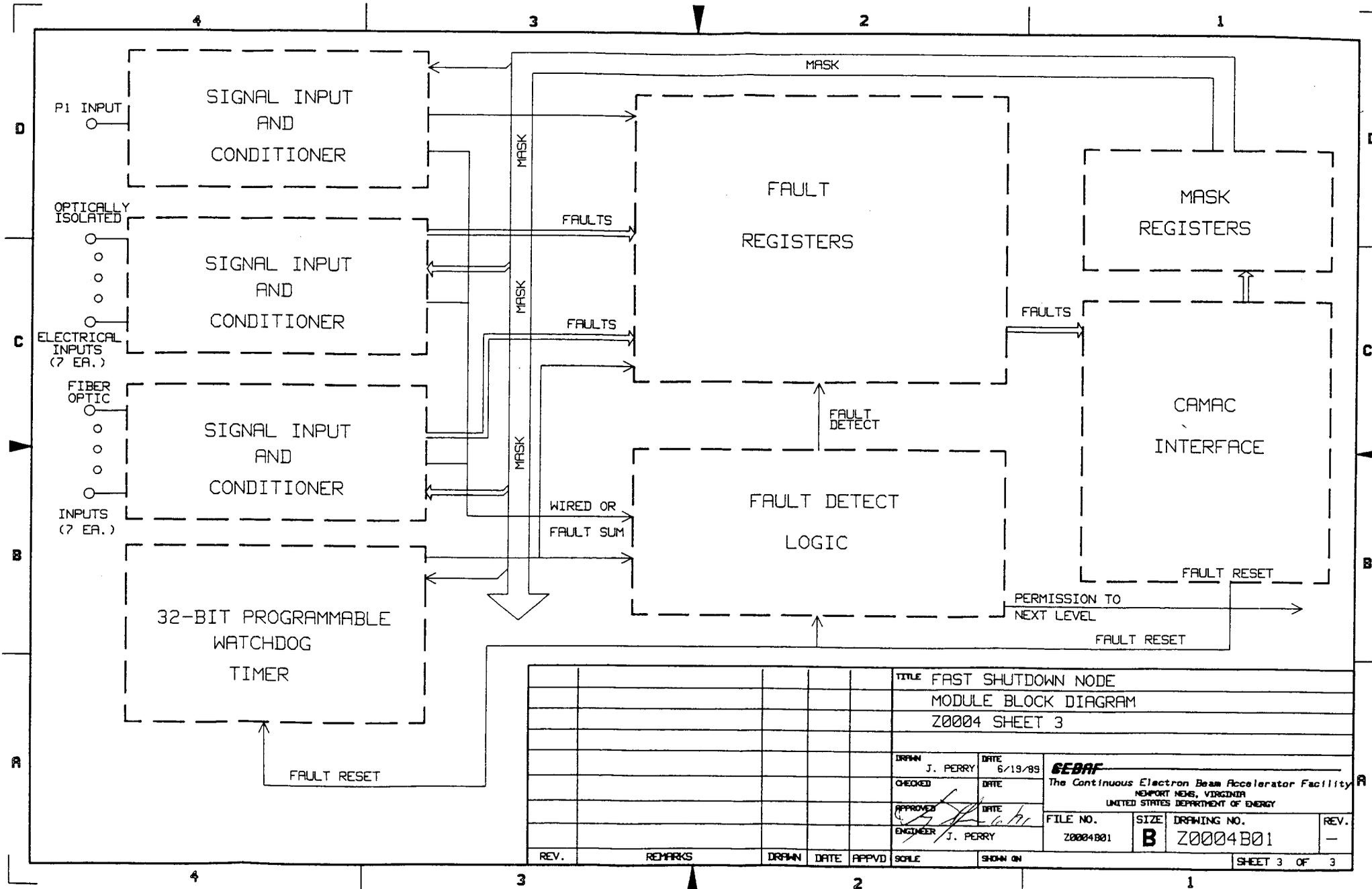


				TITLE FAST SHUTDOWN SYSTEM			
				Z0004 SHEET 1			
				OVERALL BLOCK DIAGRAM			
DRAWN		DATE		 The Continuous Electron Beam Accelerator Facility NEWPORT NEWS, VIRGINIA UNITED STATES DEPARTMENT OF ENERGY			
J. PERRY		6/19/89					
CHECKED		DATE					
APPROVED		DATE		FILE NO.	SIZE	DRAWING NO.	REV.
		6/21		Z0004B01	B	Z0004B01	-
ENGINEER	J. PERRY			SCALE	SHOWN ON		SHEET 1 OF 3
REV.	REMARKS	DRAWN	DATE	APPVD			

4 UT 3



REV.		REMARKS		DRWN	DATE	APPVD	SCALE	SHOWN ON	TITLE FAST SHUTDOWN SYSTEM Z0004 SHEET 2 OVERALL BLOCK DIAGRAM					
									DRAWN J. PERRY DATE 6/19/89	<b>CEBAF</b> The Continuous Electron Beam Accelerator Facility Newport News, Virginia UNITED STATES DEPARTMENT OF ENERGY	FILE NO. Z0004B01	SIZE <b>B</b>	DRAWING NO. Z0004B01	REV. -
									SHEET 2 OF 3					



						TITLE FAST SHUTDOWN NODE									
						MODULE BLOCK DIAGRAM									
						Z0004 SHEET 3									
						DRAWN	J. PERRY	DATE	6/19/89	<b>CEBAF</b> The Continuous Electron Beam Accelerator Facility NEWPORT NEWS, VIRGINIA UNITED STATES DEPARTMENT OF ENERGY					
						CHECKED		DATE							
						APPROVED		DATE							
						ENGINEER	J. PERRY	FILE NO.	Z0004B01	SIZE	B	DRAWING NO.	Z0004B01	REV.	-
REV.	REMARKS	DRAWN	DATE	APPVD	SCALE	SHOW ON			SHEET 3 OF 3						

V.6. Parts list

CAMAC Module-Bill of Materials 4/3/91  
 Fast Shutdown Module  
 Model: Z0004 Rev.1

Part No.	Qty.	Description	Component ID
74HC14N	1	Cmos Hex Inverter	U-5
74ALS580N	2	Octal Latch	U-5,6
74HC240N	1	Cmos Octal Bus Driver	U-3,22
74HC244N	1	Cmos Octal Bus Driver	U-3,22
74LS221N	1	Dual One-Shot	U-14
74LS125AN	1	Quad Tri-state Buffers	U-13
74LS292N	1	Programmable Timer	U-4
74HC4002N	1	Dual Quad-in Nor Gate	U-6
74ALS574N	2	Octal Register	U-15,23
74ALS576N	6	Octal Register	U-17,18,19,25,26,27
PEEL173P-35	1	12-Input PLD, CEBAF #Z0004A	U-12
MC3430	4	Quad Comparator	U-20,21,28,29
HFBR1412	1	Fiber Optic Transmitter	U-30
HFBR2412	7	Fiber Optic Receiver	U-31,32,33,34,35,36 U-37
6N137	7	High Speed Opto-coupler	U-1,2,7,8,9,10,11
VP2410	1	P-channel FET	Q-7
VN1206M(VN2010)	36	N-channel FET	Q-1,2,3,4,5,6,8,9,10 Q-11,12,13,14,15,16 Q-17,18,19,20,21,22 Q-23,24,25,26,27,28 Q-29,30,31,32,33,34 Q-35,36,37
1N5401	3	3 Amp Diode Rectifier	D-71,72,73
SBR5731	1	L.E.D., Red-Diffused	CR-33
1N4148-1JTX	37	Switching Diode	D-1,2,3,4,5,6,7,10 D-11,13,14,16,17,20 D-21,25,26,28,29,32 D-33,36,37,38,39,44 D-45,50,51,54,55,59 D-60,63,64,67,68
HP5082-2800	3	Schottky Signal Diode	CR-1,2,3,4,5,6,7,8,9 CR-10,11,12,13,14 CR-15,16,17,18,19,20 CR- 21,22,23,24,25 CR-26,27,28,29,30,31 CR-32
4308R-101-102	3	1.0K $\Omega$ SIP Res Network	RN-1,2,3

RN55C3012F	1	30.1K $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-66
RN55C2741F	1	2.74K $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-125
RN55C1821F	1	1.82K $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-59
RN55C51R1F	1	51.1 $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-25
RN55C2000F	2	200 $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-12,34
RN55C2211F	1	2.21K $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-126
RN55C1001F	38	1.0K $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-1,2,15,16,26,27 R-0,31,35,56,57 R-61,62,67,68,73,74 R-76,77,78,79 R-84,85,87,88,94,95 R-96,97,101,103 R-104,106,107,111 R-112,114,115,117 R-118,127,128,129 R-130,131,132,133 R-13,14,28,29,33A R-38,53,60,64,75 R-86,93,105,116,123
RN55C1005F	15	10.0M $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-11
RN55C5620F	1	562 $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-3,4,7,8,17,18
RN55C4991FJ	33	4.99K $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-21,22,32,33,36,37 R-41,42,45,46,47,48 R-51,52,70,71 R-82,83,90,91,99,100 R-109,110,120 R-121,124
RN55C1000FJ	31	100 $\Omega$ $\frac{1}{4}$ W 1% M.F. Res	R-5,6,9,10,19,20,23 R-24,39,40,43,44 R-49,50,54,55,58,63 R-65,69,72,80,81 R-89,92,98,102,108 R-113,119,122 R-149,155,156 R-157,158
199D106X9025CA1	2	10 $\mu$ F 25V Tant. Cap.	C-72,76
199D225X9025AA1	1	2.2 $\mu$ F 25V Tant. Cap.	C-36
CKR05BX103KM	39	.01 $\mu$ F 50V Mon. Cer. Cap.	C-1,2,3,8,10,11,12 C-13,18/A,21,27 C-28,29,30,38,40,41 C-42,43,44,45,46 C-50,51,54,55,57,59 C-60,61,62,63,64 C-65,66,69,70,73,75

CKR05BX151KM	16	150pF 200V Mon .Cer. Cap.	C-5,7,15,17,23,25,26 C-32,47,53,58,67,71
CKR05BX102KM	1	1000 pF 50V Mon.Cer. Cap.	C-31
CKR05BX821KM	16	820 pF 50V Mon.Cer. Cap.	C-4,6,14,16,19,20,22 C-24,35,48,49,52,56 C-68,74,77
CKR05BX820KM	1	82 pF 50V Mon.Cer. Cap.	C-9
CKR05BX680KM	1	68 pF 50V Mon.Cer. Cap.	C-39
265-002	2	2 Amp Pico Fuse	F-1,2
76MRSB04	5	SPST DIP Switch	SW-2,3,4,5,6
76MRSB06	1	SPST DIP Switch	SW-1
HLMP-0103	1	L.E.D. Panel Mount Hardware	H-1
107201	1	CAMAC Single-wide Hdware Set	H-2
Z0004	1	FSD Bare PCB	Z0004
TOTAL	363		

## **V.7. Schematic Diagrams**

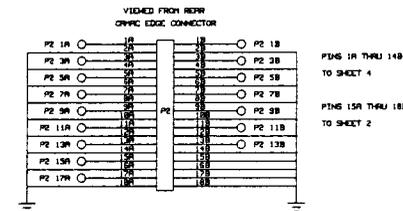
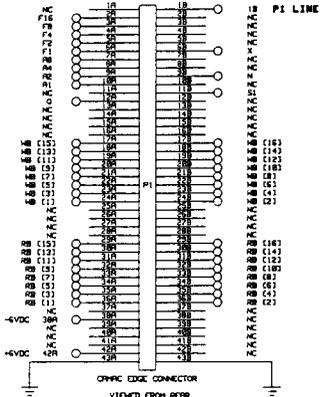
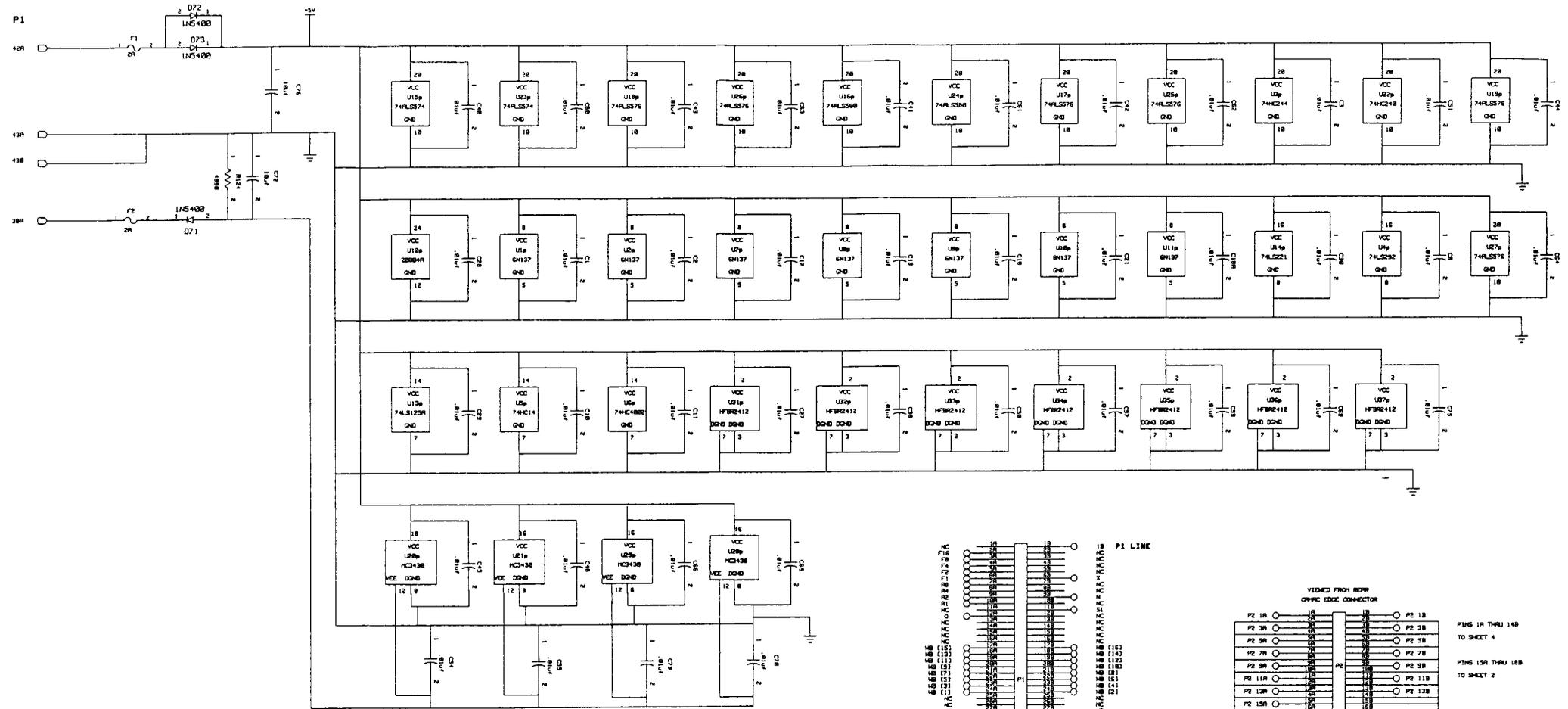
### **V.7.1 Block Diagrams**

### V.7.2 Rear Connector signal assignments

Signal Name	SIDE A	Position	SIDE B	Signal Name
EXT 0 SIG	A	1	B	EXT 0 RET
GND	A	2	B	GND
EXT 1 SIG	A	3	B	EXT 1 RET
GND	A	4	B	GND
EXT 2 SIG	A	5	B	EXT 2 RET
GND	A	6	B	GND
EXT 3 SIG	A	7	B	EXT 3 RET
GND	A	8	B	GND
EXT 4 SIG	A	9	B	EXT 4 RET
GND	A	10	B	GND
EXT 5 SIG	A	11	B	EXT 5 RET
GND	A	12	B	GND
EXT 6 SIG	A	13	B	EXT 6 RET
GND	A	14	B	GND
WD OUT SIG	A	15	B	WD OUT RET
GND	A	16	B	GND
AUX PERM SIG	A	17	B	AUX PERM RET
GND	A	18	B	GND

Fig. V.7.2-J2 connector signal definitions

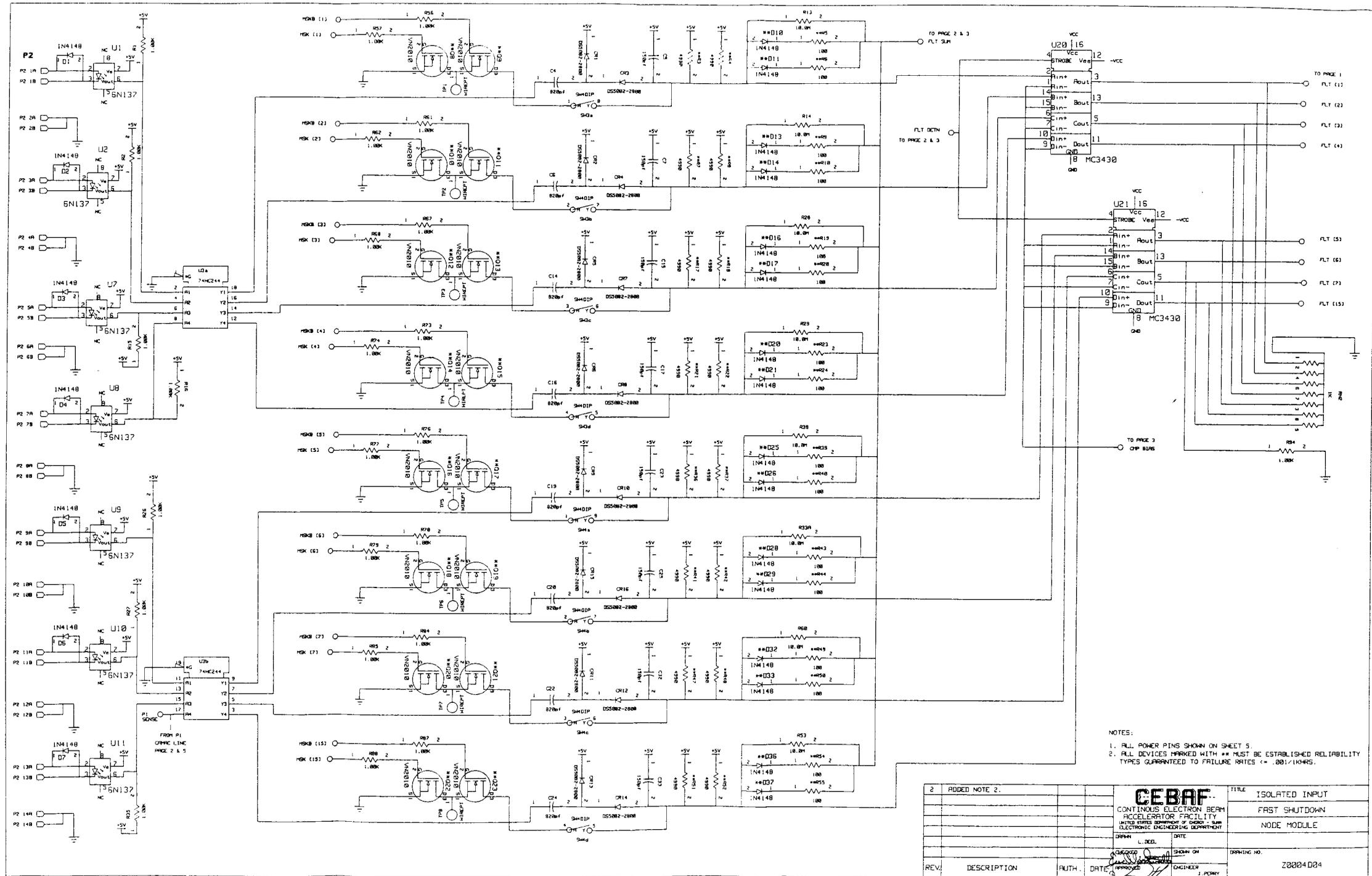
Z0004D05



ALL ORPIC CONNECTORS CONNECTED TO PAGE 1 EXCEPT FOR 18 WHICH IS CONNECTED TO PAGE 2 & 4, 38V & 42V WHICH ARE CONNECTED ABOVE.

		<b>CEBAF</b>		TITLE POWER DISTRIBUTION	
		CONTINUOUS ELECTRON BEAM ACCELERATOR FACILITY		FAST SHUTDOWN	
		MITSUBISHI UNIVERSITY OF SCIENCE & TECHNOLOGY ELECTRONIC ENGINEERING DEPARTMENT		NODE MODULE	
DATE	DESIGNED BY	DATE	DESIGNED BY	DATE	DESIGNED BY
11/11/83	J. PERCY	11/11/83	J. PERCY	11/11/83	J. PERCY
REV.	DESCRIPTION	AUTH.	DATE	DESIGNED BY	Z0004D05

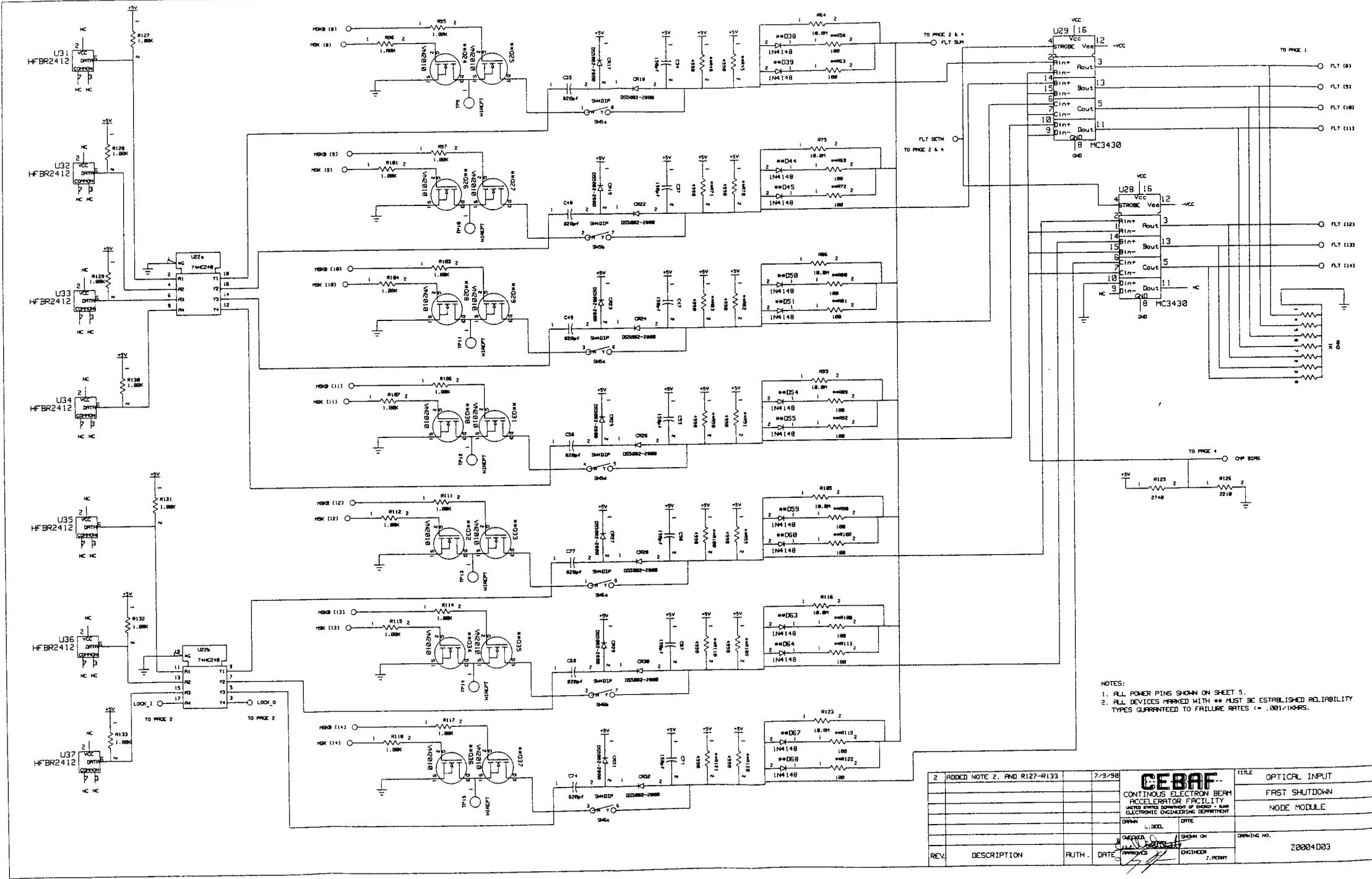
Z0004D04



2	ADDED NOTE 2.				
REV:	DESCRIPTION	AUTH:	DATE:	SHOWN ON:	DRAWING NO. Z0004D04

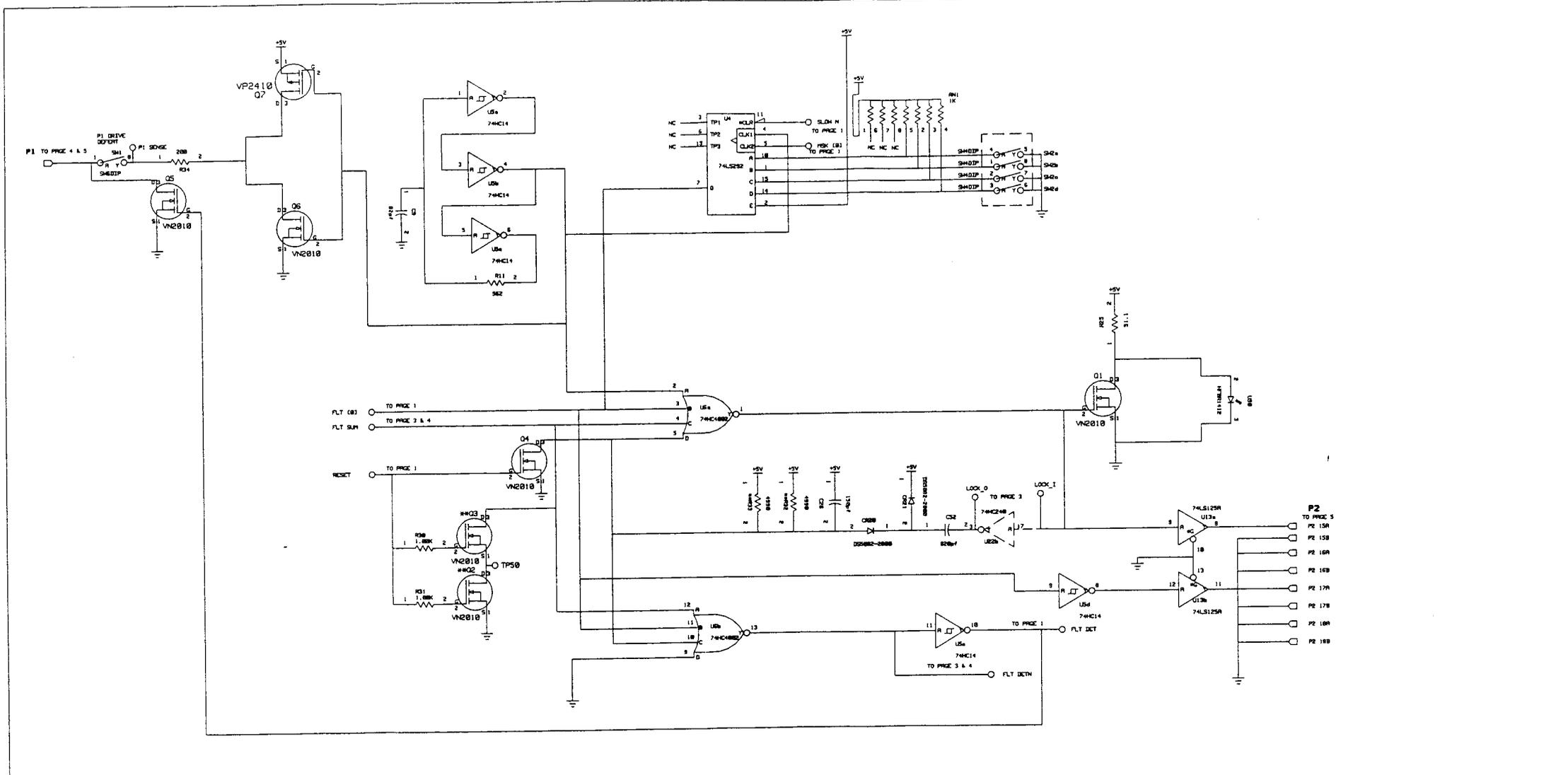
**CEBAF**  
 CONTINUOUS ELECTRON BEAM  
 ACCELERATOR FACILITY  
 UNITED STATES DEPARTMENT OF ENERGY  
 ELECTRONIC ENGINEERING DEPARTMENT  
 DATE: \_\_\_\_\_  
 L. DEL. \_\_\_\_\_  
 CHECKED: \_\_\_\_\_  
 APPROVED: \_\_\_\_\_  
 ENGINEER: J. POKRY

Z0004D03



NOTES:  
 1. ALL POWER PINS SHOWN ON SHEET 5.  
 2. ALL DEVICES MARKED WITH \*\* MUST BE ESTABLISHED RELIABILITY TYPES GUARANTEED TO FAILURE RATES (<= .001/HRS).

2	ADDED NOTE 2, AND R127-R133	7/9/98	<b>CEBAF</b> CONTINUOUS ELECTRON BEAM ACCELERATOR FACILITY JAMES CLAYTON LABORATORY OF PHYSICS - SLAC ELECTRONIC ENGINEERING DEPARTMENT		TITLE OPTICAL INPUT
			DRAWN: [Signature] DATE: [Blank]		FAST SHUTDOWN
			CHECKED: [Signature] DATE: [Blank]		NODE MODULE
			APPROVED: [Signature] DATE: [Blank]		DRAWING NO. Z0004D03
REV.	DESCRIPTION	AUTH.	DATE	DESIGNED BY J. PERRY	

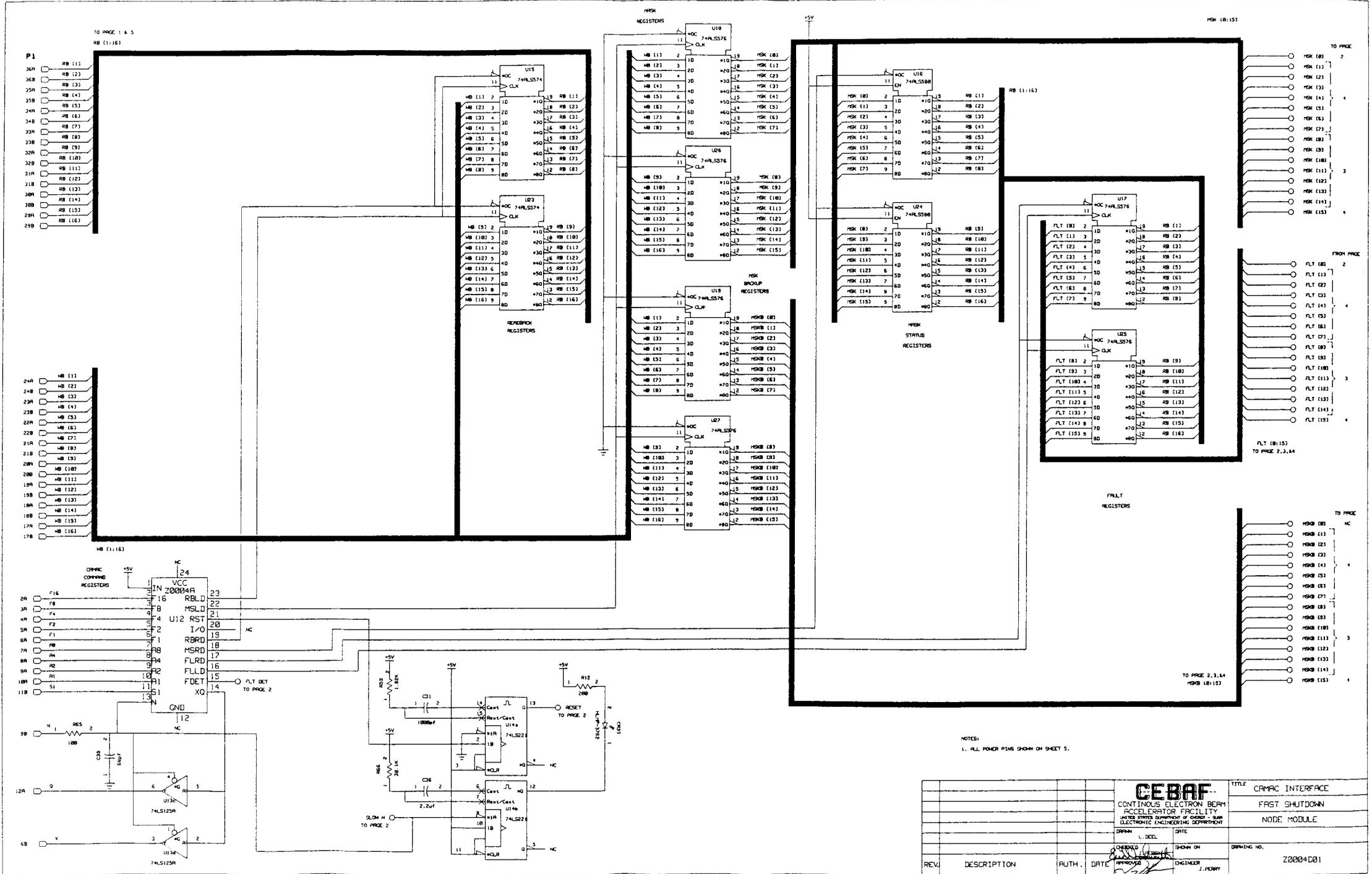


NOTE: 1. ALL DEVICES MARKED WITH \*\* MUST BE ESTABLISHED RELIABILITY TYPES GUARANTEED TO FAILURE RATES <= .001/10KHS.

2	ADDED NOTE 1.				
A	ECO #E5012				
REV.	DESCRIPTION	AUTH.	DATE	APPROVED	ENGINEER

<b>CEBAF</b> CONTINUOUS ELECTRON BEAM ACCELERATOR FACILITY <small>UNIVERSITY OF MARYLAND SYSTEM          ELECTRONIC ENGINEERING DEPARTMENT</small>		<b>TITLE</b> FAULT LOGIC SECTION	
		FAST SHUTDOWN	
		NODE MODULE	
DRAWN L. DEL DATE	CHECKED J. POWRY SHOWN BY	DATE	DRAWING NO. Z0004D02
APPROVED J. POWRY ENGINEER			

20004D01



NOTES:  
1. ALL POWER PINS SHOWN ON SHEET 5.

<b>CEBAF</b> CONTINUOUS ELECTRON BEAM ACCELERATOR FACILITY <small>UNIVERSITY OF MARYLAND - BALTIMORE          ELECTRONIC ENGINEERING DEPARTMENT</small>		TITLE	
		CAMAC INTERFACE	
DRAWN: U. DEEL CHECKED: [Signature] APPROVED: [Signature]		DATE	
		DRAWING NO. Z0004D01	
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