DAQ and Trigger for HPS run

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Requirements

- 50kHz event rate at Event Builder
- 250MB/s data rate at Event Builder (calorimeter 25MB/s, muon 6MB/s, SVT 215(up to 500)MB/s)
- 100MB/s data rate on tape (after level3 trigger)

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DAQ System Overview

- SVT readout system (ATCA)
- Calorimeter and Muon System Readout: 442 channels of 12bit 250MHz Flash ADCs, 144(<=256) channels of 85ps resolution pipeline TDCs with discriminators
- Flash ADC - based trigger system
- 2 VME, 1 VME64X, 3 VXS, 1 ATCA crates equipped with Readout Controllers and Trigger Units
- JLAB CODA DAQ software

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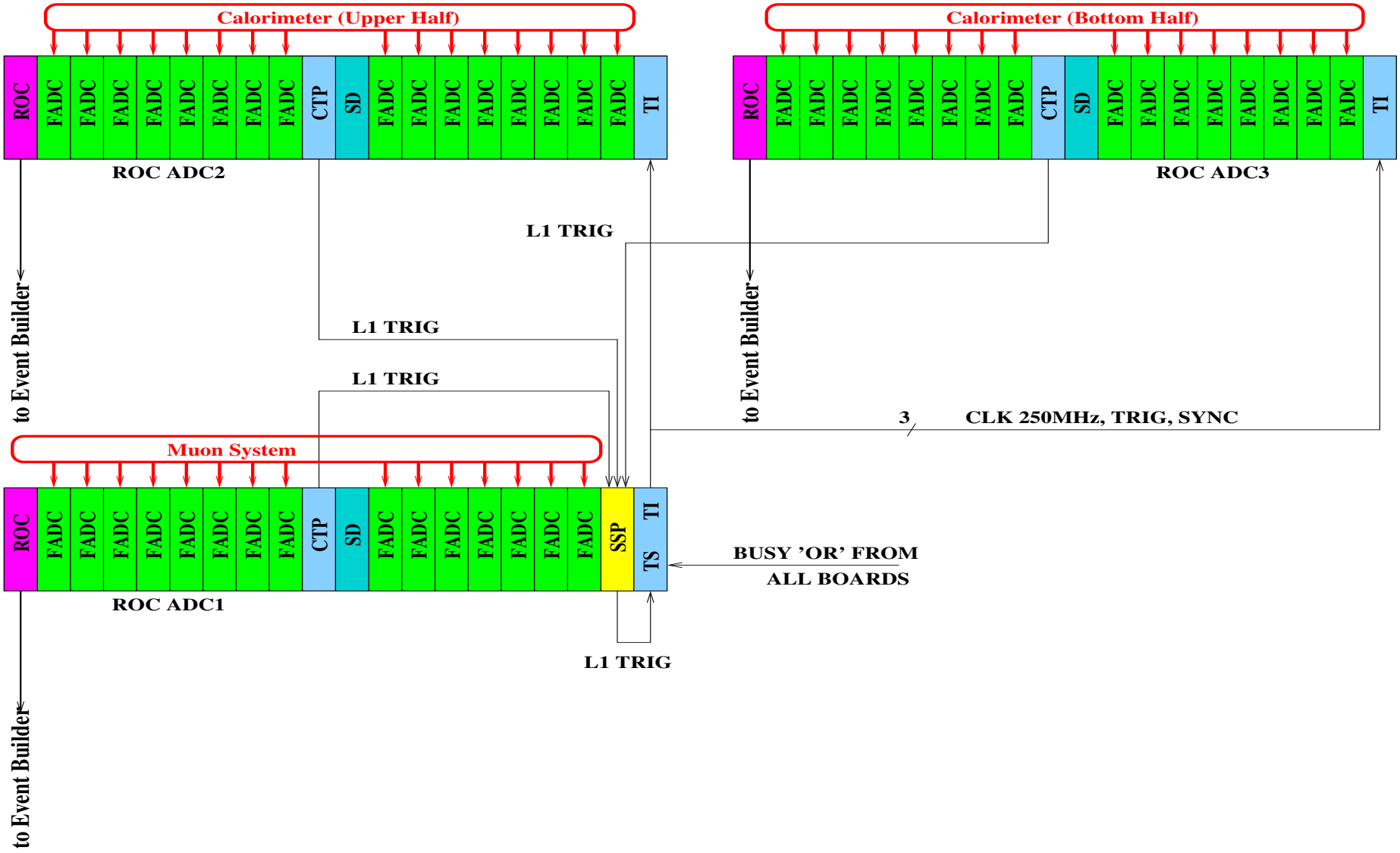
ATCA SVT Readout System (SLAC)

- One year time scale to finish electronics development
- Will test SVT readout with the rest of the system, probably using simplified setup in SLAC

Flash ADC and Trigger System (VXS)



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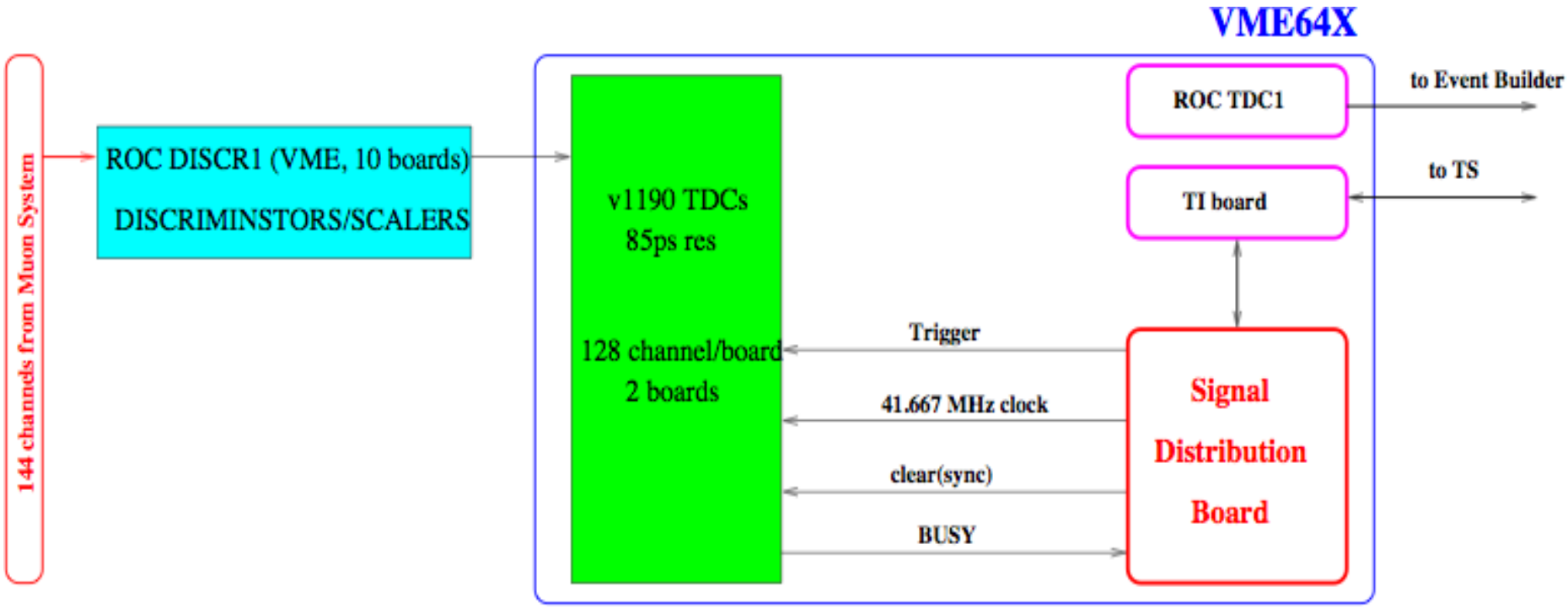
Pipeline TDC System (VME64X/VME)



NOTE: will not use it if FADCs produce timing and scalers (timing is not implemented yet)

Trigger processing - CTP/SSP

- Calorimeter: search for clusters using 3x3 crystals window
- Muon system: search for hits
- Trigger 1: two calorimeter clusters; cuts on cluster multiplicity, geometry (with respect to beam) and energy (two thresholds)
- Trigger 2: two muon hits, cuts on geometry (upper and bottom) and energy (threshold)
- Possible problem: boundary effects because of segmented calorimeter readout and limited bandwidth between CTP and SSP – will be addressed with new CTP design increasing bandwidth to SSP

Slow control and online data analysis

- EPICS information will be inserted into data stream
- DAQ/Trigger parameters (pedestals, thresholds etc) will be loaded using standard procedure (TBD), and inserted into data stream, in most cases directly from electronic boards
- Logbook and slow control logging are under development in JLAB, should be one solution for all groups
- Environment to run online (level 3) software will be provided
- Working analysis is REQUIRED from the very beginning of the run to obtain trigger parameters

Timeline

- All boards are available and tested: end of 2013 (except CTP – will try go have it summer 2014)
- New version of FADC, CTP and SSP trigger FPGAs firmware: end of 2013 (summer 2014; timing from FADC ?)
- Testing with new SVT electronics: end of 2013 (?)
- DAQ /Slow Control/Online Monitoring software: summer 2014 (hope to complete in time)
- New network/computing: end of 2014
- HPS commissioning: end of 2014
- Manpower: we switched to CLAS12 DAQ software development; also have new Hall B visitor working on slow control; all that in favor of HPS run plans