Overview of SVT DAQ Upgrades

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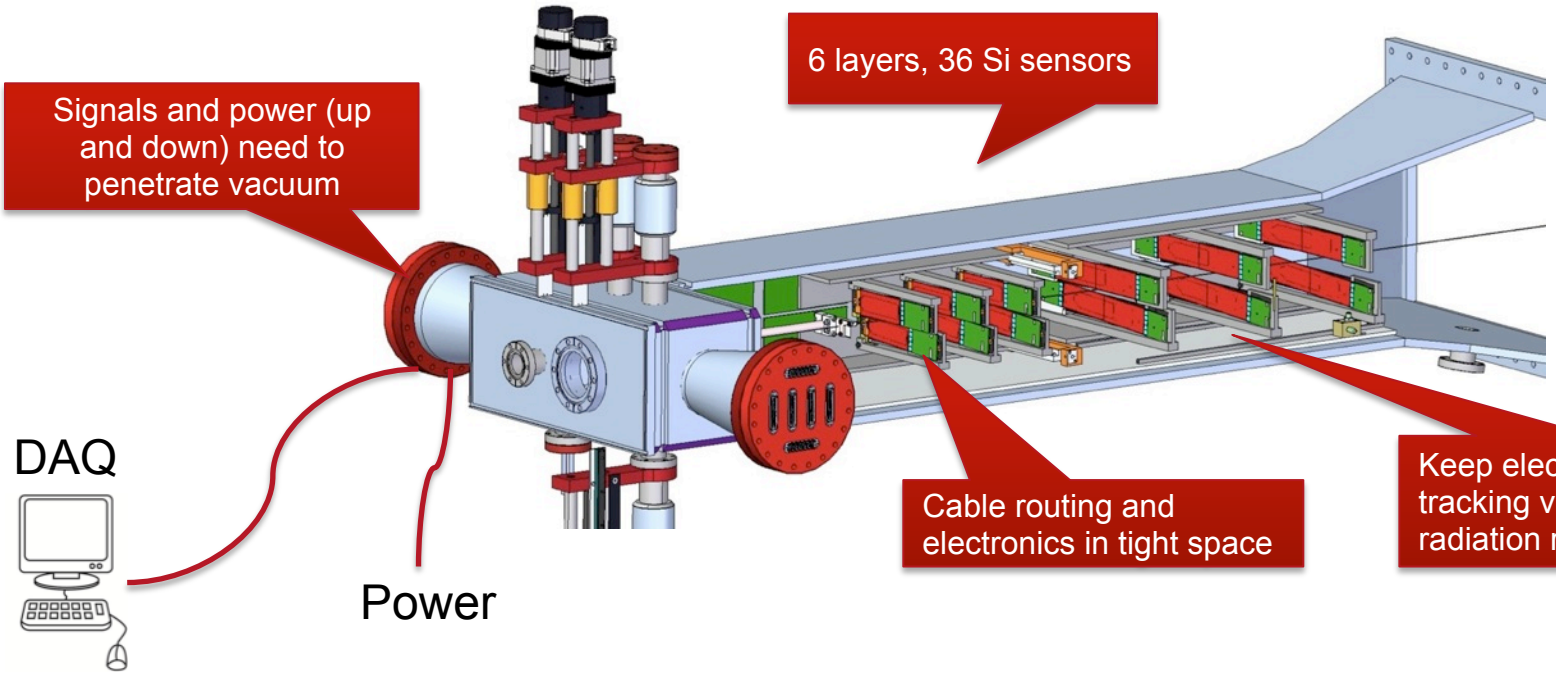
SVT DAQ Requirements and Constraints

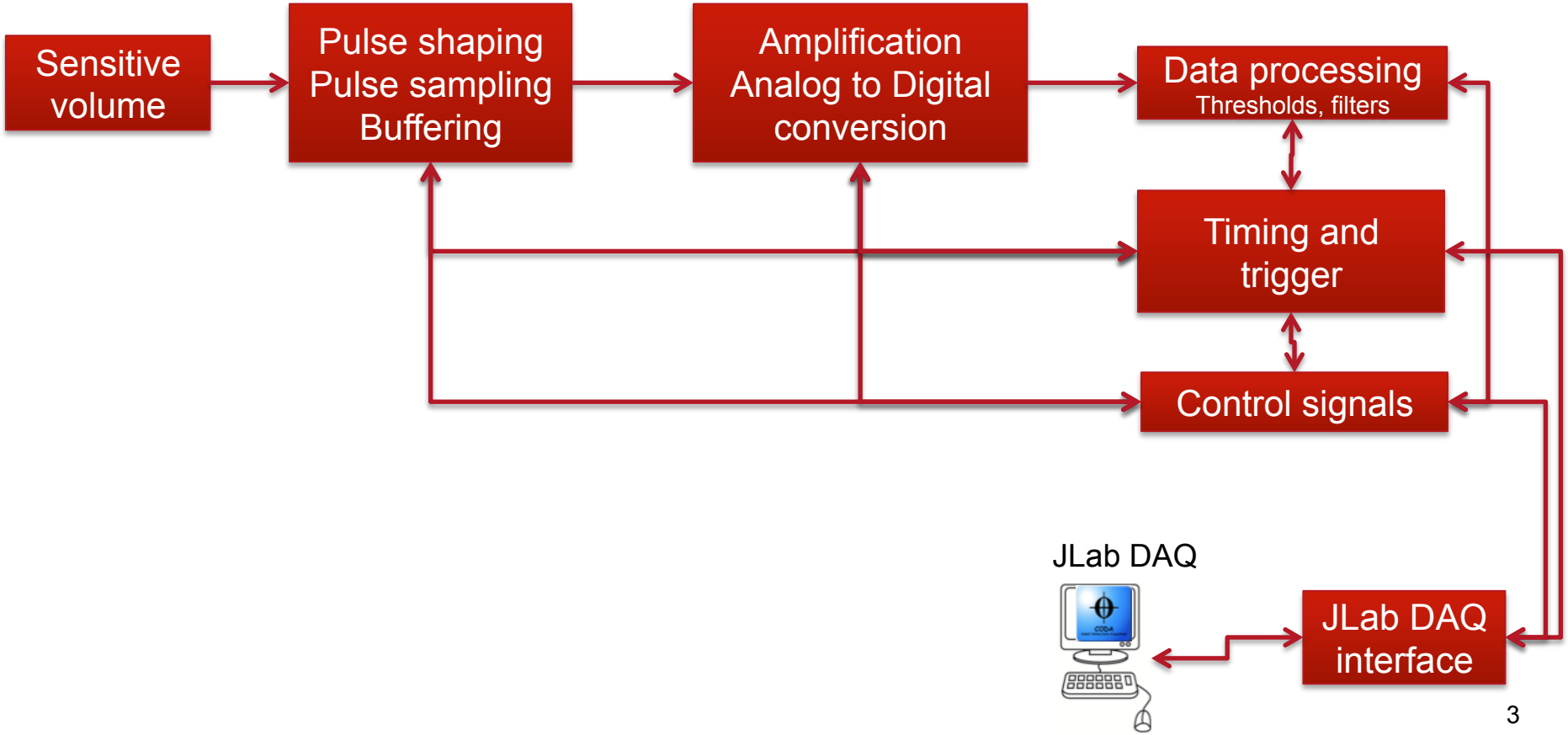
Basic requirements for the SVT DAQ

- Continuous readout of 23'040 channels
- Low noise (S/N>20 to achieve high spatial resolution)
- Facilitate hit time reconstruction ~2ns
- High rate and bandwidth: up to 50kHz and 100MB/s

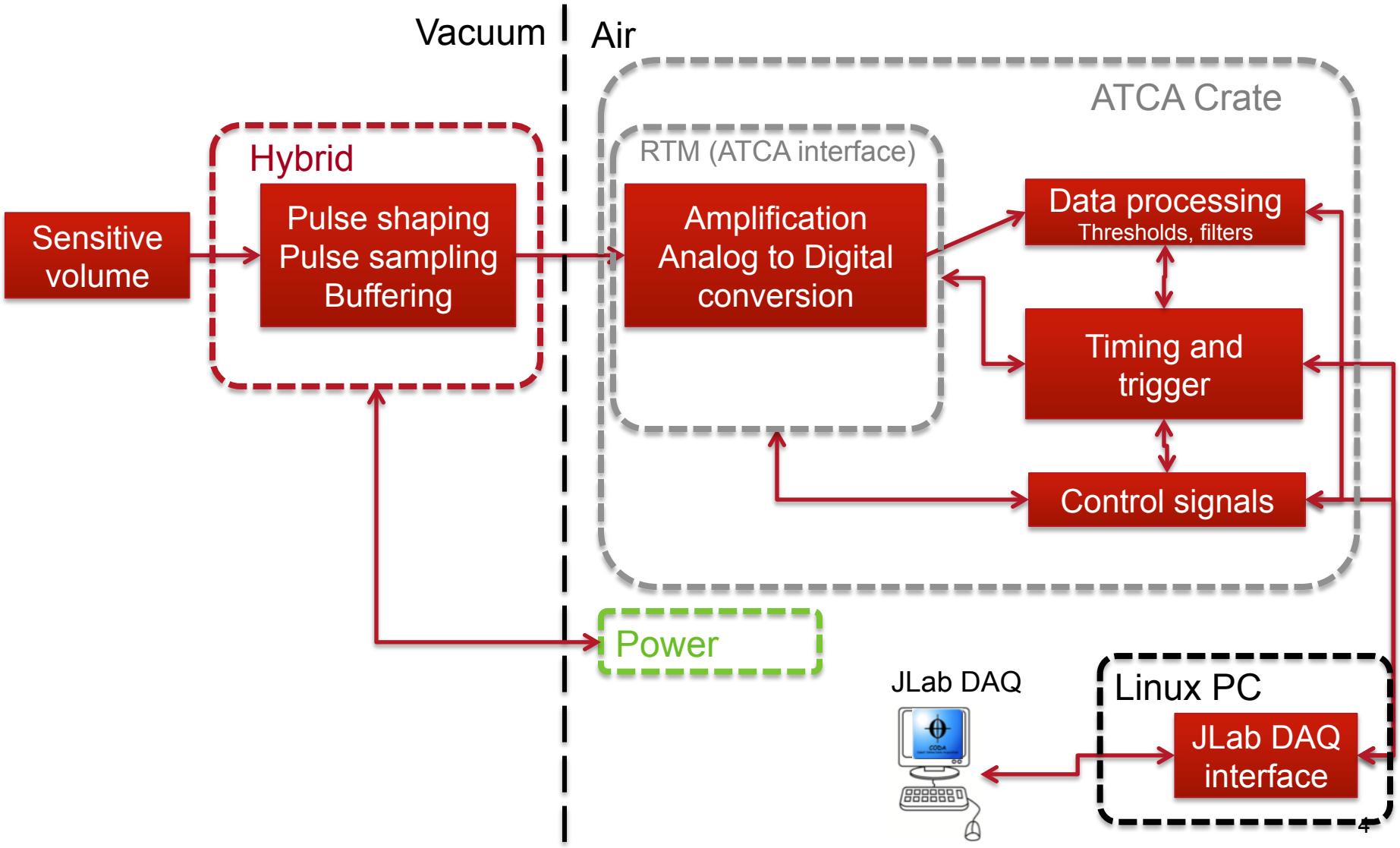
Physical constraints



SVT DAQ Functional Overview



SVT DAQ Functional Overview – Test Run DAQ



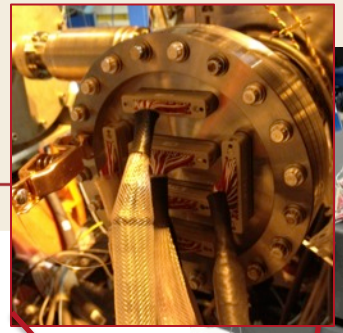
Key Areas Driving Upgrades

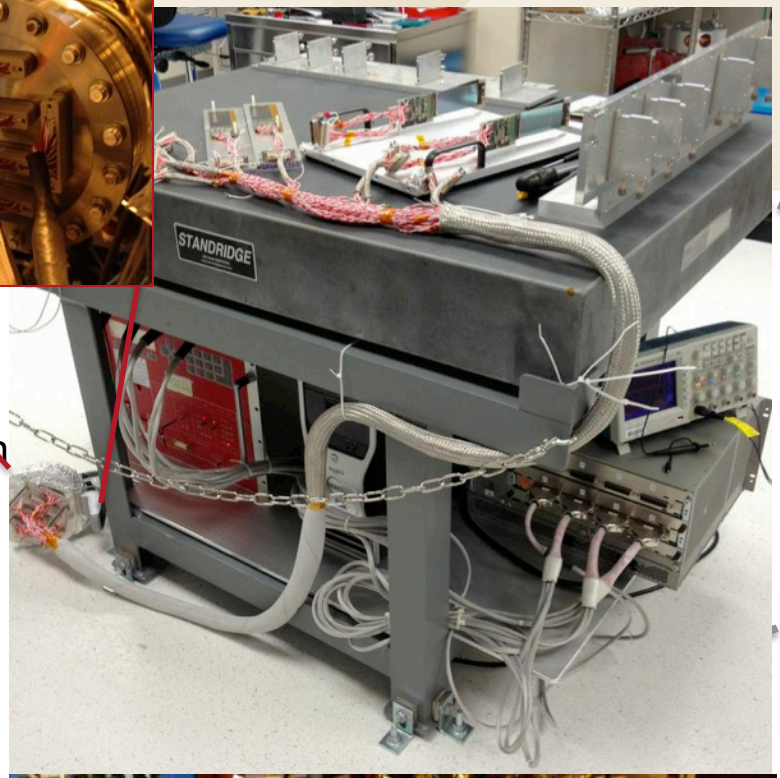
Test run discoveries

Improved performance and JLab integration

Support for additional (16) hybrids

Test Run Discoveries





Large vacuum penetration count and long cable runs

- Fragile connections
- Impendence mismatches: caused reflections in test run
- FPGA based FIR filters deployed (clock and trigger?)

⇒ **Power distribution inside chamber**

⇒ **Custom vacuum flange boards with fixed circuit board feed-troughs**

⇒ **Digitize closer to hybrids**

Clock & trigger skews observed

⇒ **Per hybrid timing adjustments (per FPGA/3hybrids in test run)**

ATCA power supply failure (most likely due to radiation)

⇒ **Optical conversion to allow greater flexibility in location**

Improve Performance and JLab Integration

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Rate was limited in test run (full system tests to 11.5kHz)

- External Linux PC used as DAQ computer
- Full event frames assembled from ATCA (TI DPM) on low latency (PCI-e) card into event buffer
- JLab ROC application transferred data on 1Gbps Ethernet link to JLab DAQ

Upgrades to reach 50kHz rate

- Use latest generation SLAC ATCA-architecture (w/ gen3 RCE computation element) to replace external DAQ PC
- Implement ROC on RCE (ARM w/ Linux OS) or separate Intel processor blade
- 10Gbps link between SVT and JLab DAQ
- Support for burst trigger mode for APV25 chips

Improved trigger interface: use full JLab implementation

Support for Layer 4-6

New SVT half module for 2014 run

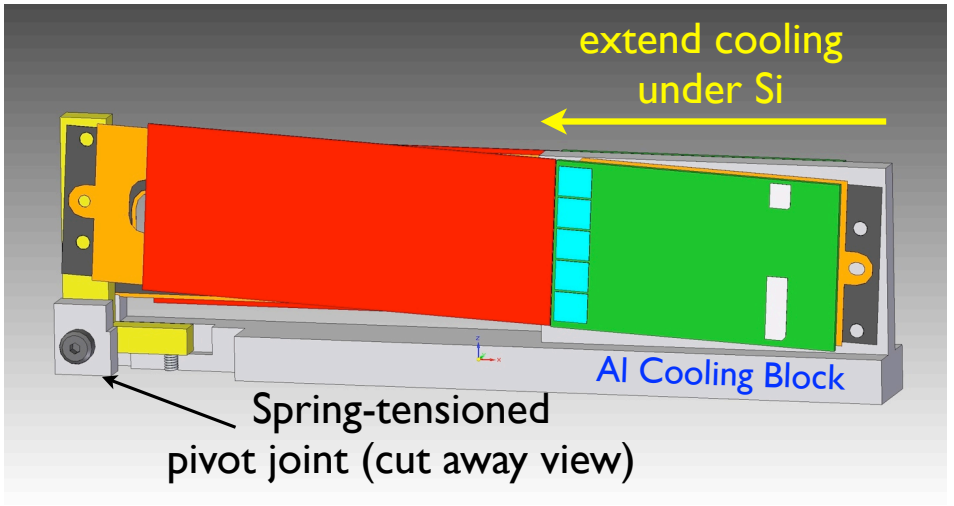
- Layer 1-3: re-use test run half-modules
- Layer 4-6: new double-wide modules

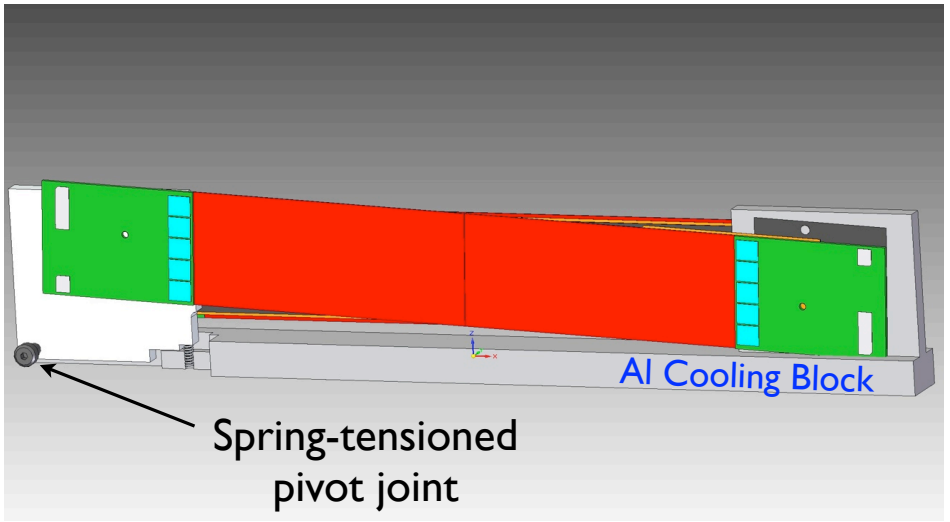
Need smaller hybrid

- Length: 69.6➔49mm
- Similar width

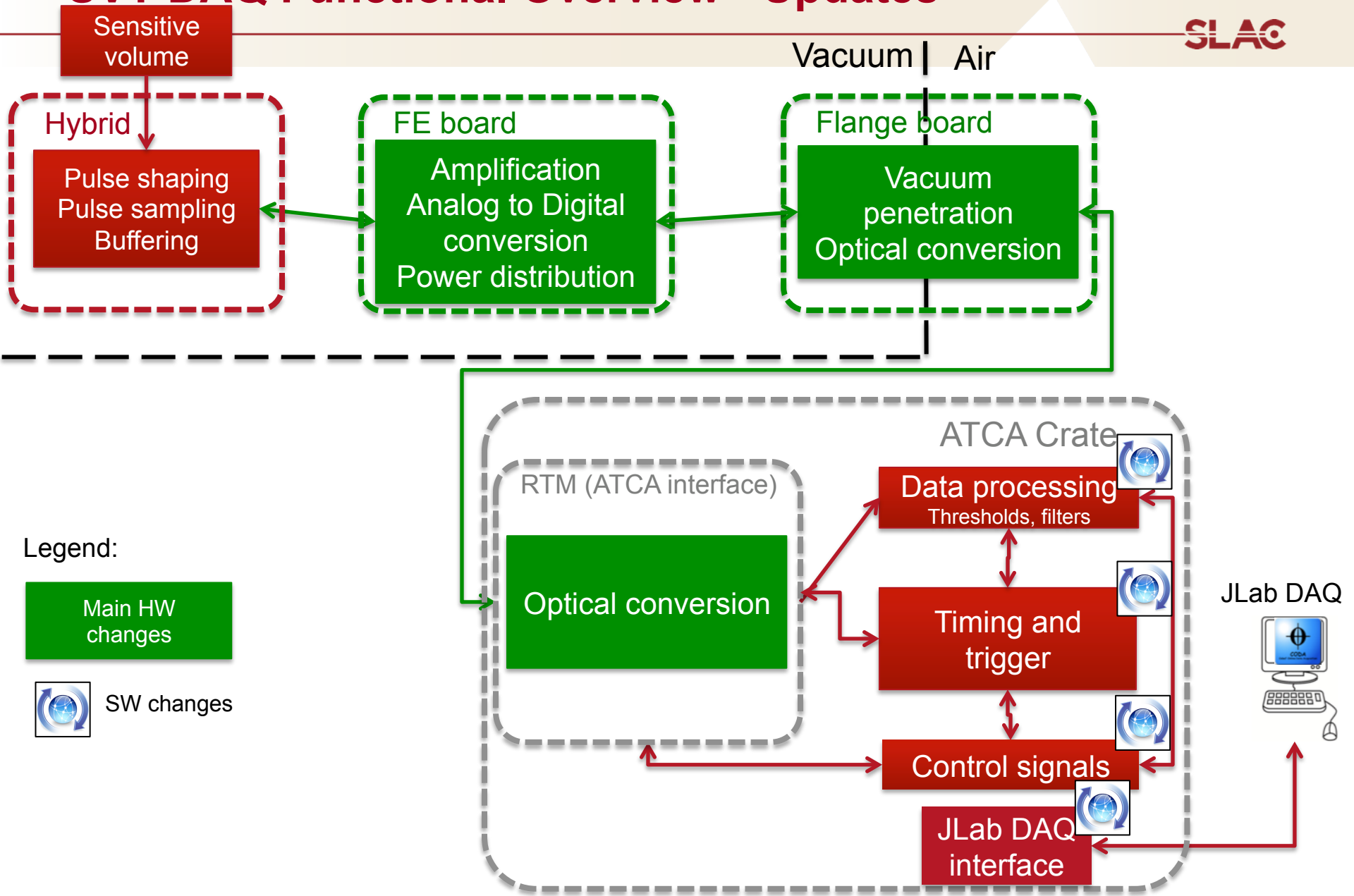
Existing hybrid layout revised

- Remove unused components
- Smaller connecterization footprint





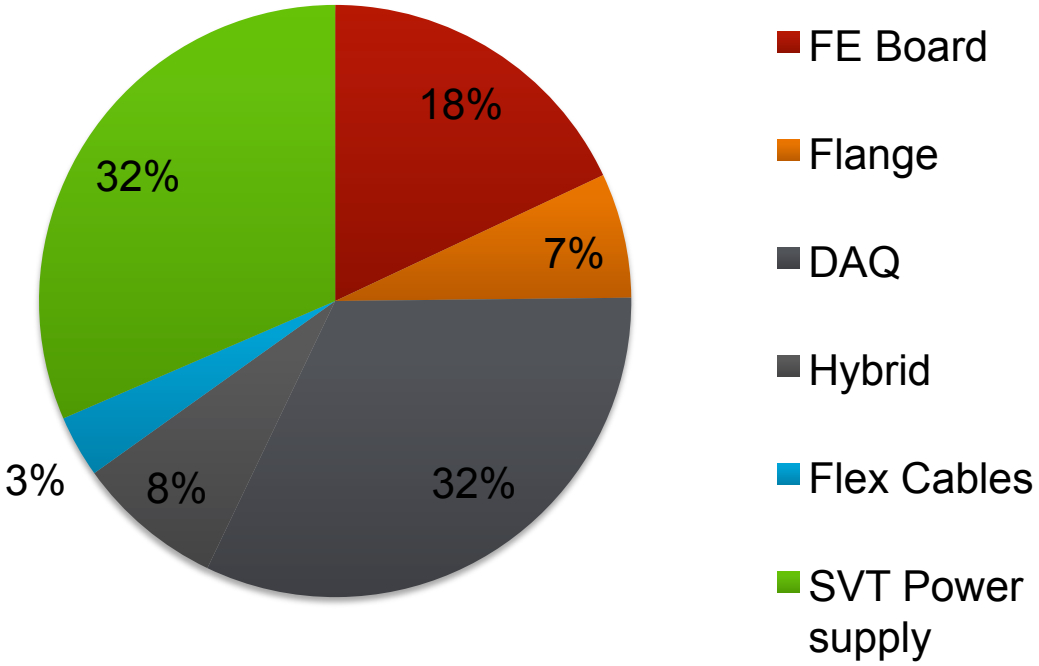
SVT DAQ Functional Overview - Updates



Project Overview

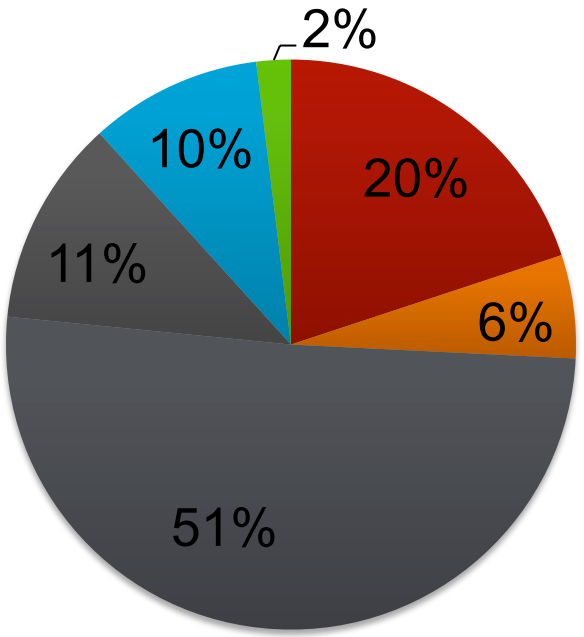
Broken into six sub-projects

Materials



Total: $267,000

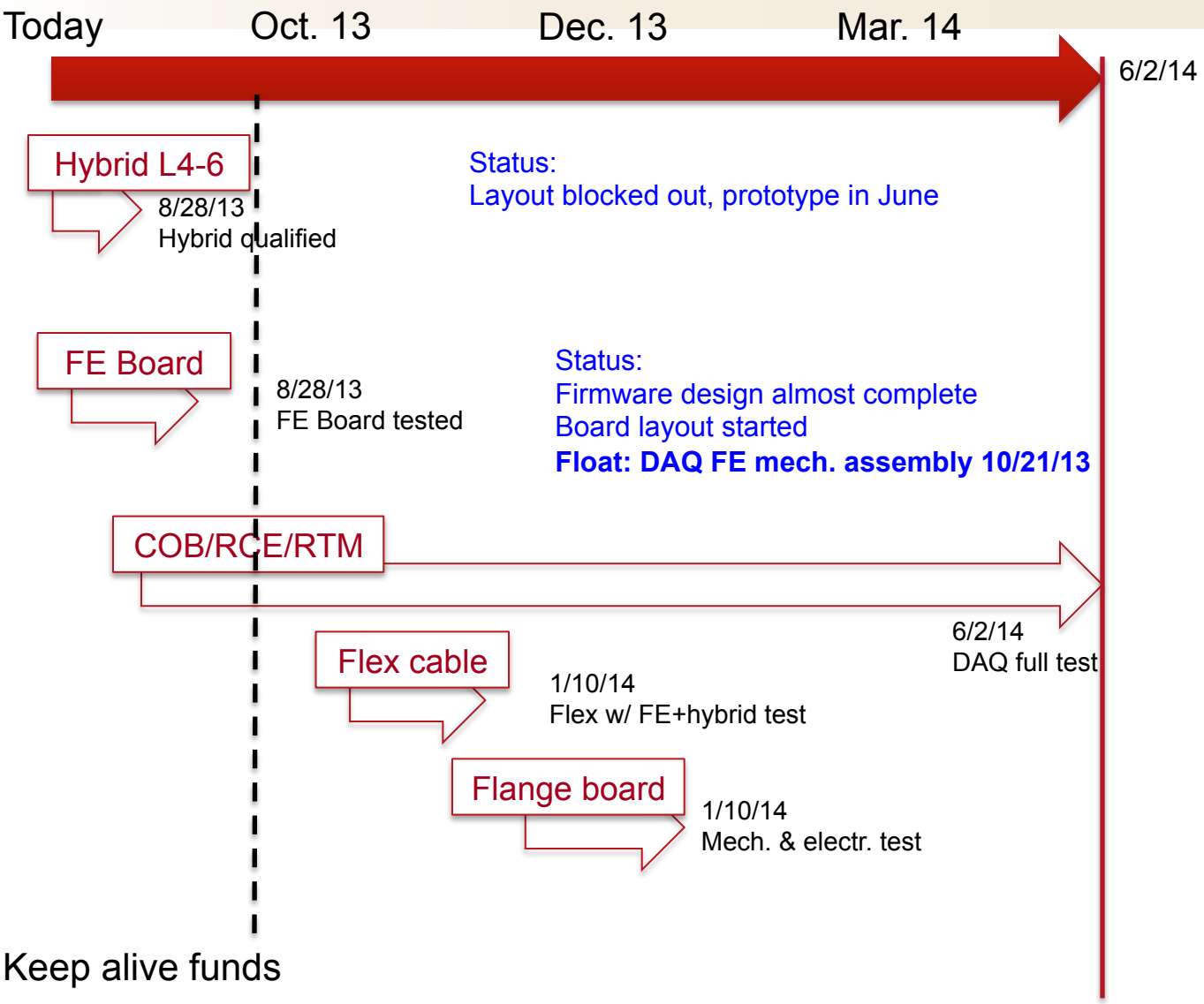
Manpower



Total: $342,000

Cost w/o cont. /w OH (SLAC)

Project Overview



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Summary of SVT DAQ Upgrades

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SVT DAQ for commissioning run based on test run DAQ

- Repackaging of test run components
- Some new hardware
- Bulk of development in DAQ software

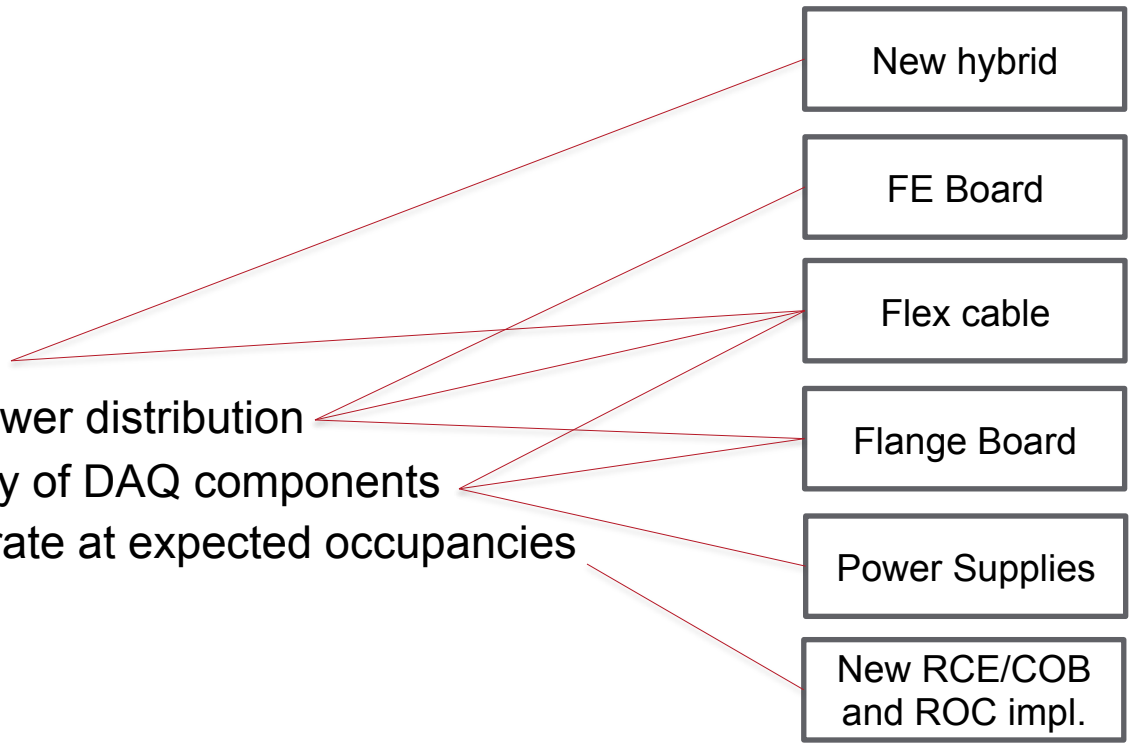
Upgrades driven by

- Mitigate test run issues
- Support additional 16 hybrids
- Improve performance

Key features

- Support for new Layer 4-6
- In chamber digitization and power distribution
- Improved stability and flexibility of DAQ components
- Performance: 50kHz readout rate at expected occupancies

Upgrade project components



Backup