HPS Collaboration Meeting, JLAB June 4-6, 2013

SVT Data Acquisition Architecture

Ryan Herbst

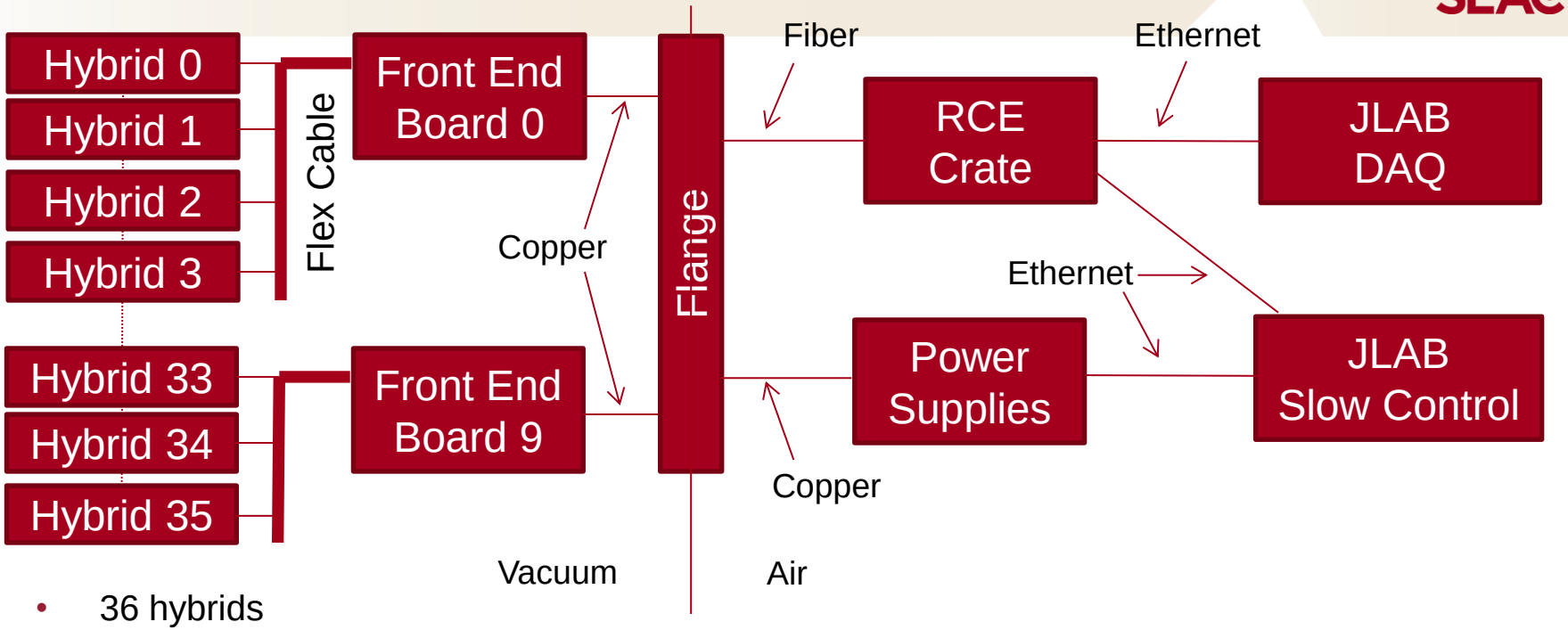
U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Overview

- SVT DAQ Overview
- In chamber electronics
  - Hybrids
  - Flex Cables
  - Front End Boards
- Flange & feed through
  - Signal feed through & fiber optic conversion
  - Low voltage distribution
  - High voltage distribution
- External electronics
  - Fiber optics
  - RCE platform
  - SVT DAQ Software
- Interface to JLAB DAQ

SVT Overview



- 36 hybrids
  - 12 in layers 0 – 3 (4 per layer, 2 top, 2 bottom)
  - 24 in layers 4 – 6 (8 per layer, 4 top, 4 bottom)
  - 3.33Gbps raw ADC data per hybrid
- 10 front end boards
  - 4 servicing layers 0 – 3 with 3 hybrids per board
    - 10 Gbps raw ADC data per board
  - 6 servicing layers 4 – 6 with 4 hybrids per board
    - 13 Gbps raw ADC data per board
- RCE crate for event building and data reduction

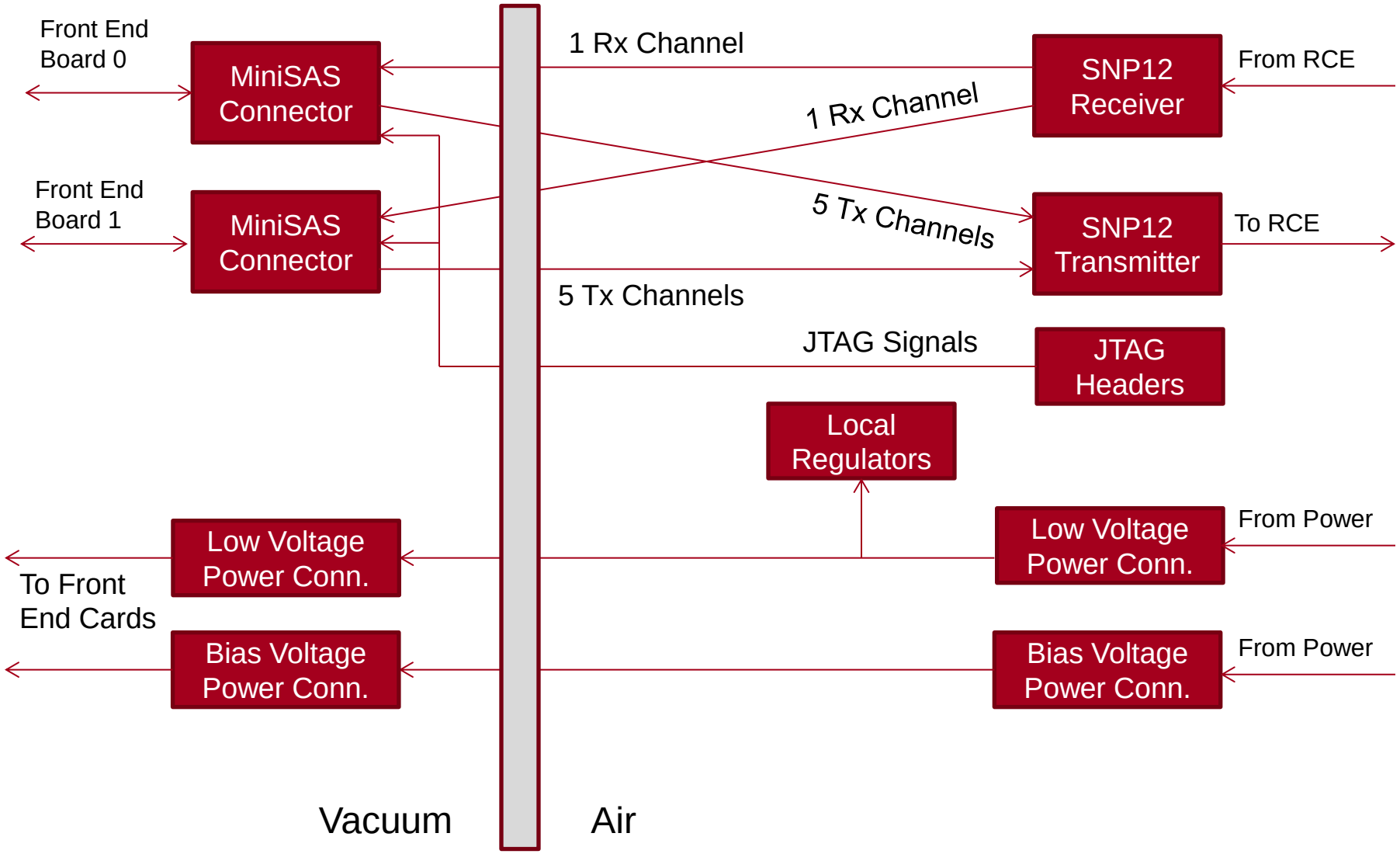
In Chamber Electronics

- Hybrids
  - Interface to detector
  - Provide detector bias voltage and filtering
  - 5 x APV25 ASICs for readout
  - Layers 0 – 3 use existing hybrid/sensor modules
  - Layers 4 – 6 are an updated design
- Flex cables
  - Interface between hybrids and front end boards
  - New for 2014 run
  - Variety of cables required
    - One cable set per front end board
    - Creative approaches to minimize number of unique designs
  - Variety of design constraints
    - Must support 100ohm differential analog signals @ 50Mhz readout
    - Must support low voltage busses for each hybrid with minimal voltage drop
    - Must support 1KV bias voltages for each connected hybrid
    - Reliable connectors which support all of the above
- Front End Board
  - New for 2014 run
  - Provide power to hybrids
  - APV25 configuration and monitoring
  - APV25 clock and trigger generation
  - ADC and data transmission
  - Simple well tested firmware to minimize upgrade necessity

Vacuum Flange

- Must support the following:
  - 56 High speed digital signal pairs
    - 1 output per hybrid at 5Gbps
    - 1 output per front end board at 2.5Gbps
    - 1 input per front end board at 2.5Gps
  - 30 low voltage channels
    - 1 digital voltage and return per front end board
    - 1 positive analog voltage and return per front end board
    - 1 negative analog voltage and return per front end board
  - 36 high voltage channels
    - 1KV bias voltage and return per hybrid
  - 4 JTAG signals per front end board
- Internal vacuum cables
  - Mini-SAS cables for high speed digital and JTAG
  - Twisted pair mil-spec cables for low voltage
  - TBD for bias voltages
- External cables
  - Fiber optics for high speed digital
  - Twisted pair mil-spec cables for low voltage
  - TBD for bias voltages (SHV?)
- Implemented as multi-layer circuit board potted into flange at the middle
  - All active components are socketed for in field replacement
  - Will require its own low voltage supply for transceivers

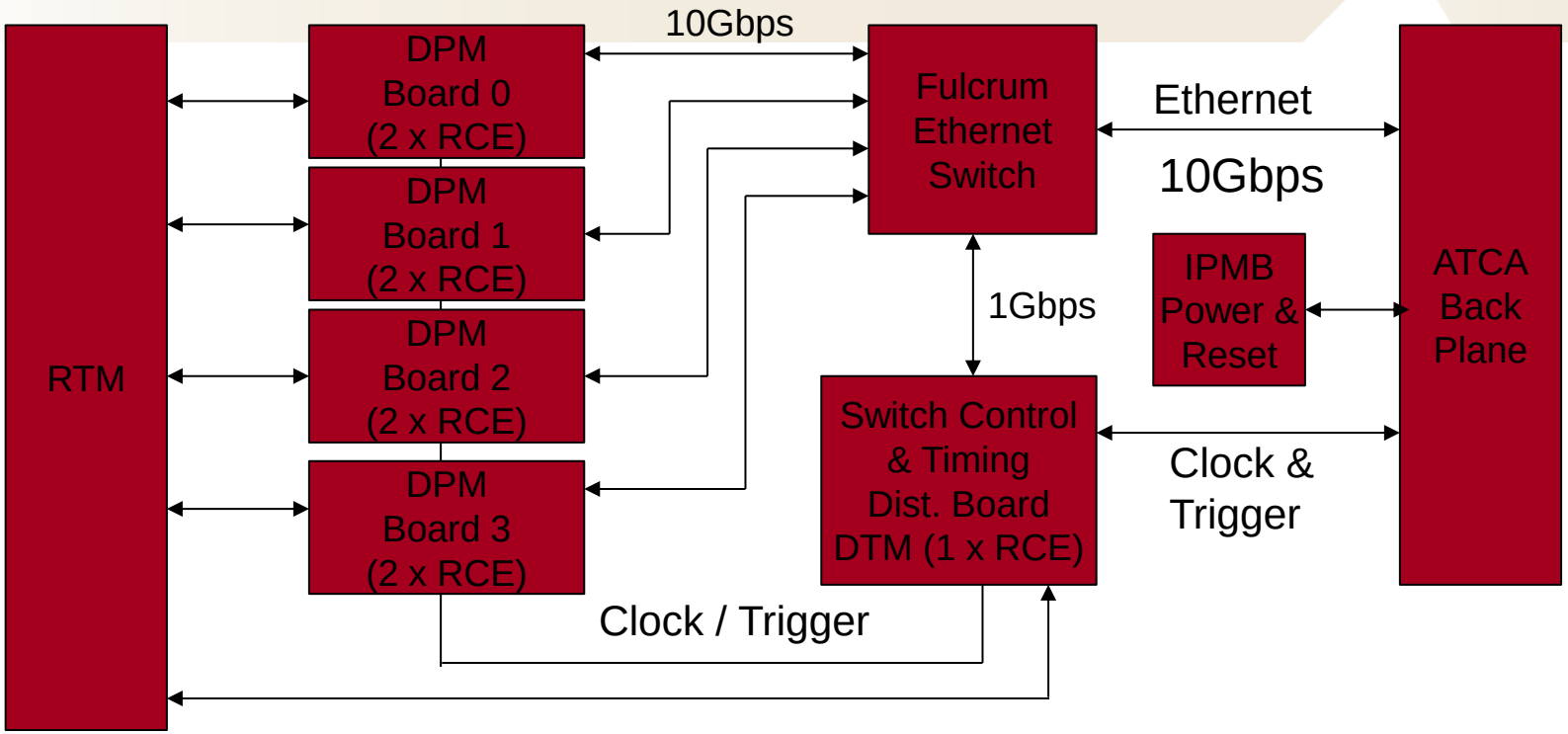
Vacuum Flange



External Electronics

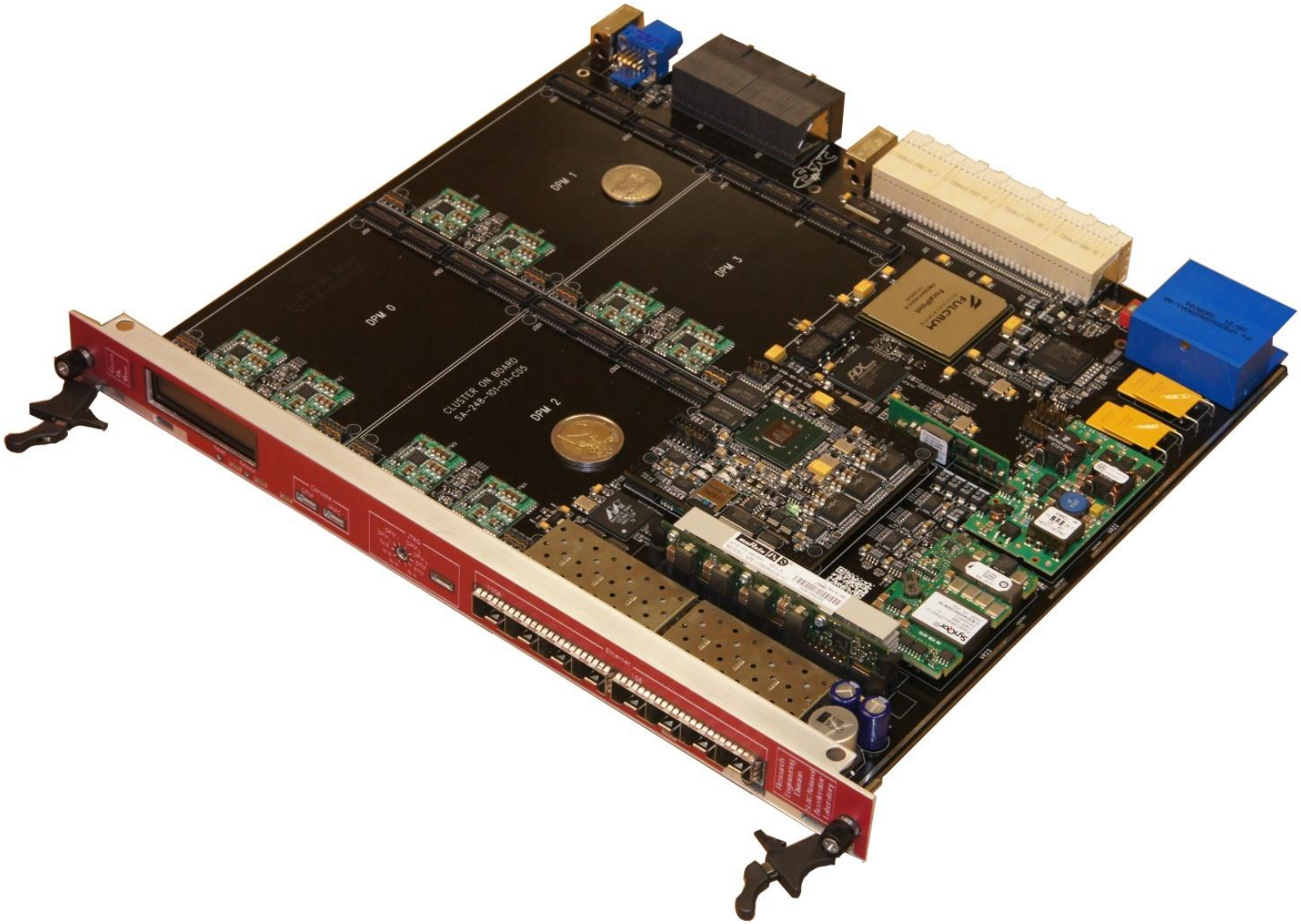
- Fiber optic interface between flange and SVT DAQ
  - Provides distance between beam line and DAQ crate
- DAQ node based upon SLAC RCE platform
  - Reconfigurable cluster element
  - ATCA based platform
  - 10Gbps Ethernet internal interconnect
  - Used in a variety of experiments
    - Current: LCLS, LSST, HPS, ATLAS IBL test stands
    - Planned: ATLAS CSC, LBNE, Darkside
  - Hosts firmware data processing
    - Analog signal filtering
    - Data reduction
    - Event formatting
  - Hosts software event building
    - Buffer management and event packaging
- Interface to JLAB DAQ
  - 10Gbps Ethernet for data path
  - JLAB standard trigger interface

SLAC Gen3 COB



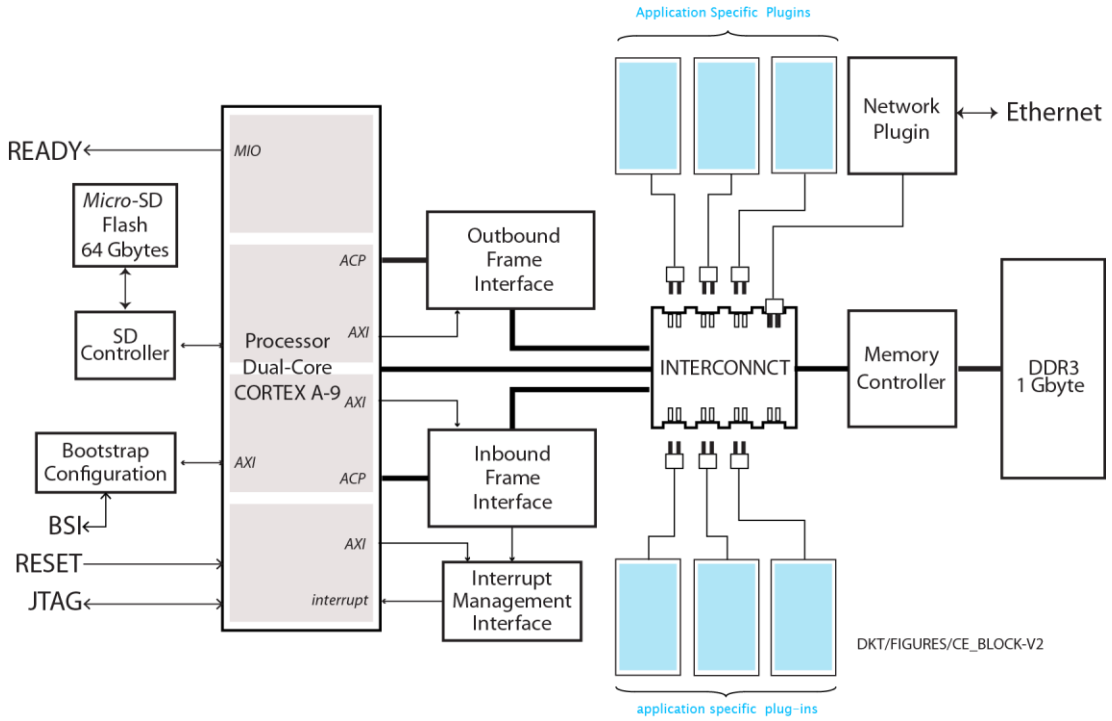
- COB (Cluster On Board)
  - Developed at SLAC as standard DAQ platform
- Supports 4 data processing FPGA mezzanine cards (DPM)
  - Interconnected by Fulcrum Ethernet switch
  - 2 RCE nodes per DPM
  - Each has connection to ¼ RTM
- Data transport module (DTM)
  - 1 RCE node
  - Contains RCE node in smaller FPGA package
  - Provides Fulcrum switch management
  - Interface to backplane clock & trigger lines & external trigger/clock source

RCE GEN3 COB

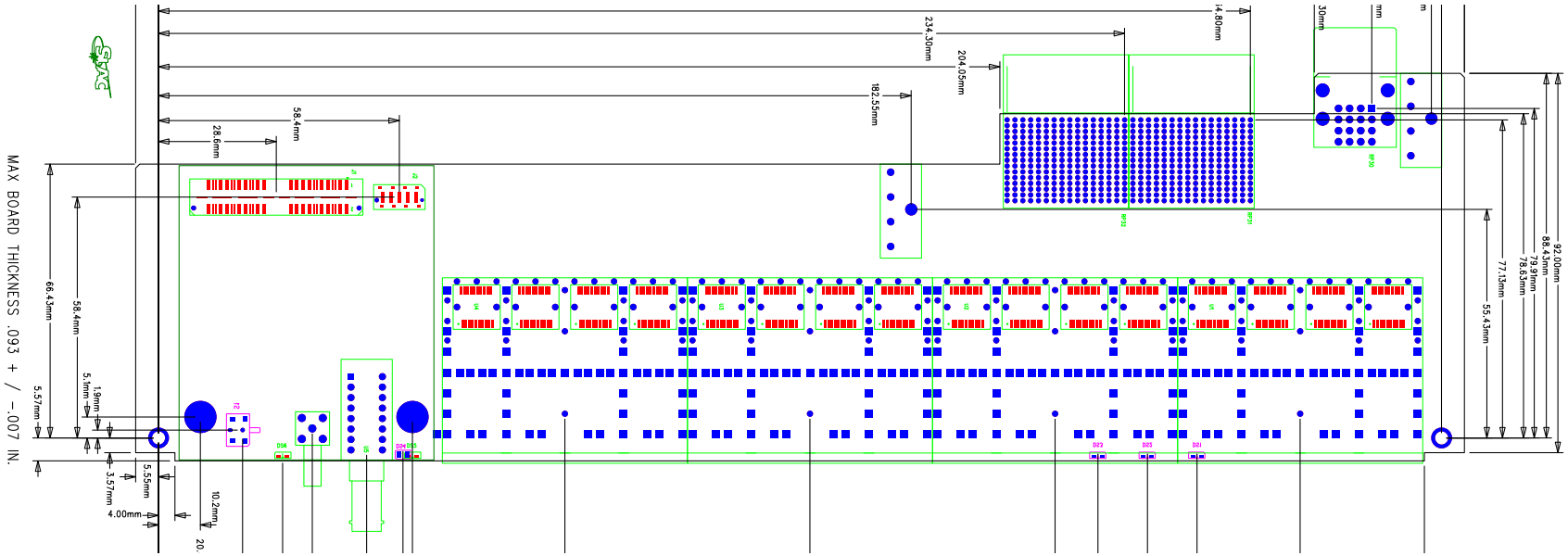


RCE (Reconfigurable Cluster Element)

- Two versions
  - 2 x Zynq XC7Z045 FPGA for DPM
  - 1 x Zynq XC7Z030 FPGA for DTM
- ARM (dual-core) A-9 @ 900 MHZ
  - 1 Gbyte DDR3
  - Micro-SD (removable)
  - 10-GE MAC
- Bootstrap configuration
  - External I2C interface
  - Communicates with IPMC
- Socket Interface for plugins
  - transfer data in units of frames
  - 10Gbps bandwidth into memory
- Software (bundled with CE):
  - Linux
    - Based on 3 series kernel
  - RTEMs
    - Open Source Real-Time kernel
    - POSIX compliant interfaces
  - TCP/IP stack
  - Plugin socket library
- External serial interfaces
  - 10 GTX receive channels
  - 6 GTX transmit channels

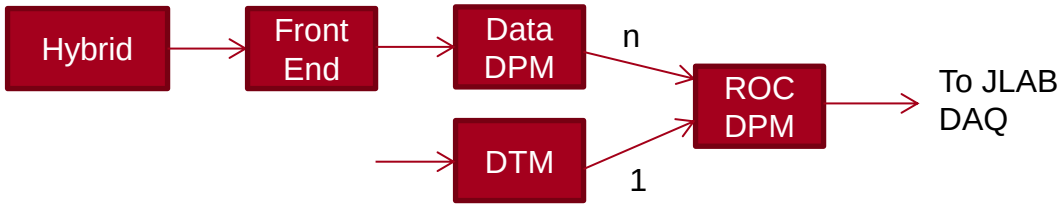


RCE GEN3 RTM



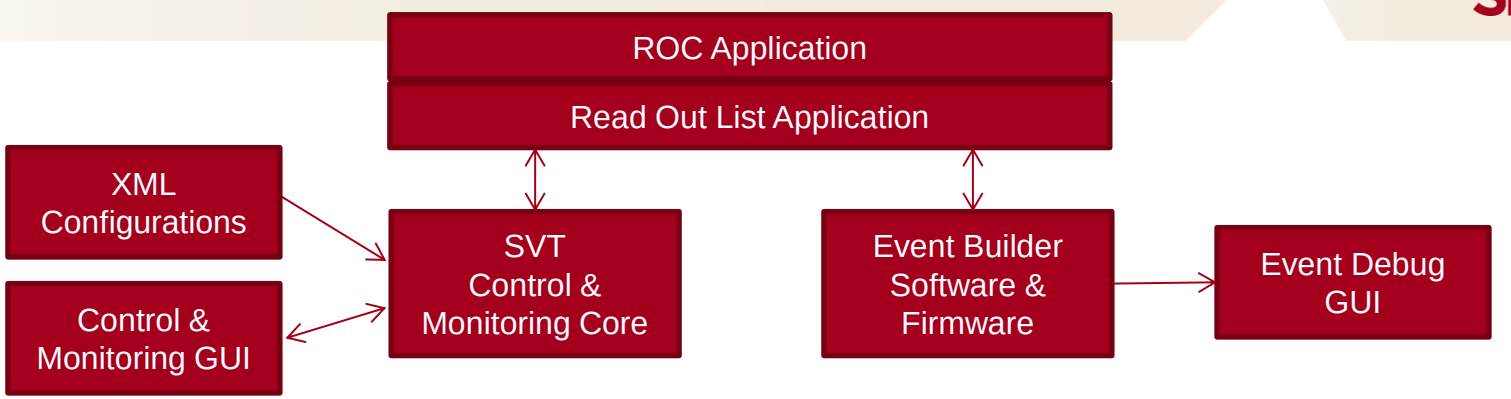
- Standard SLAC RTM
  - 10 receive channels per RCE
  - 6 transmit channels per RCE
- SNP12 fiber optic interface
- Daughter board for application specific timing interface and distribution
  - Will host interface to JLAB trigger supervisor
  - Distributes timing and trigger to each RCE on a COB

SVT Data Flow



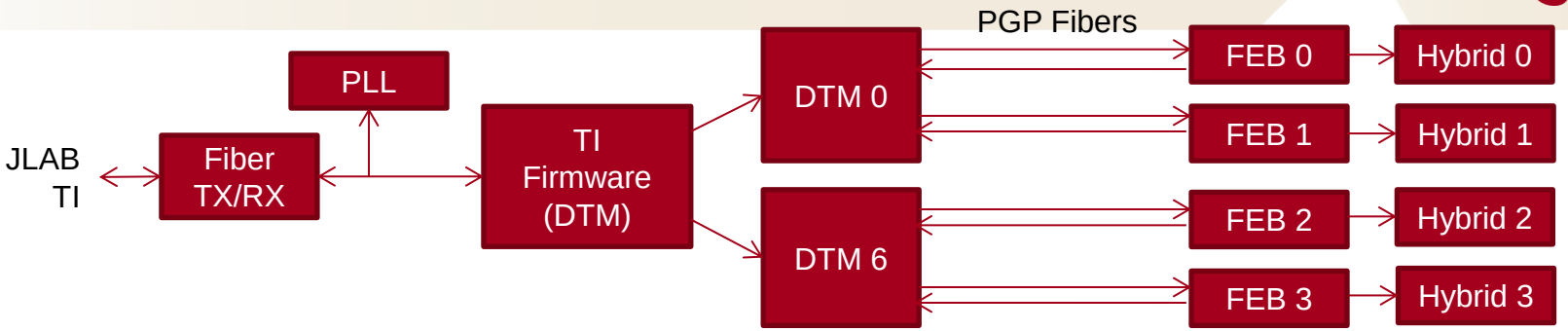
- RCE platform is fully configurable
  - Number of front end boards per Data RCE?
  - 1 COB model:
    - 7 data RCEs and 1 ROC RCE
    - 4 for layers 0 – 3 (1 front end per data RCE, 3 hybrids per data RCE)
    - 3 for layers 4 – 6 (2 front ends per data RCE, 8 hybrids per data RCE)
    - 1 DTM RCE for trigger interface
  - 2 COB model:
    - 10 data RCEs and 2 ROC RCEs
    - 1 front end per RCE
    - 2 DTM RCEs for trigger interface
- Data RCE processes raw ADC data
  - Event builds data at full trigger rate (50Khz)
  - Packs events into blocks defined by buffer size
    - Estimate 32 – 40 events per block
    - Blocks are then forwarded to ROC DPM over Ethernet
  - May be able to run Linux but RTEMS will have better performance
- ROC RCE accepts event blocks from data RCE nodes and trigger RCE node (DTM)
  - Operates at lower rate of trigger rate / block size (~1 – 2 Khz)
  - Arm Linux

SVT DAQ Software



- ROC application
  - Pre-compiled JLAB software
  - Can either run on ROC RCE or ATCA Intel server blade
    - Preferred location is ROC RCE (direct link to hardware)
    - Depends on success of ROC port to Arm Linux
- Readout List Application
  - Front end specific code developed by SLAC
  - Shared memory interface to control and data modules
    - Replaced by network interface when ATCA server blade used
- SVT Control & Monitoring Core Software
  - Interface to data processing RCEs, front end boards & APV25s
  - Configurations pulled from XML files
  - Local control & monitoring GUI
  - Slave to ROC and readout out list applications during run
- Event builder software
  - Interface to event building firmware layer
  - Hooks for SVT specific debug display
  - Handoff to read out list application

Timing Distribution



- System timing provided by JLAB Trigger Interface
  - 250Mhz base clock
  - Synchronized reset for derived clocks
  - Trigger signal and timestamp
  - Fiber and PLL hardware on RTM daughter board
  - JLAB firmware and driver in DTM
    - Hope to use true subset of JLAB TI firmware
    - Simplified SLAC implementation used in test run
- DTM distributes timing to DPMs on local COB
  - 12Mhz clock
  - PLL reset (used for 41Mhz clock generation)
  - Trigger pulse
  - Trigger timestamp and status to ROC DPM
- DPMs forward timing information to front end boards over PGP
  - Clock encoded into serial data stream which the front end board recovers
  - Fixed latency path for encoded PLL reset and trigger signals
  - Upstream link echoes encoded clock and encoded signals back to DPM
  - Round trip latency is measured and compensated for by adjusting delay elements in FEBs
    - Front end boards aligned in time domain

Conclusions

- Improvements since test run
  - ATCA power supply problems
    - Added external ADC layer inside chamber
    - Fiber optic interface to front end allows greater distance from beam line
  - Reflections on analog interface to APV25s
    - Internal ADC boards with improved internal cabling
  - Sample clock phase
    - See Ben's talk
  - Data rates
    - High rate event processing done in RTOS/firmware
    - ROC and readout list application running at lower rates
      - Determined by event block size
  - General stability
    - More run time in test stands!!!!
- Other issues
  - How do we handle calibrations?
    - Need to adjust APV25 settings periodically during run
    - Need to know which channel was selected during data analysis
    - Lots of options, need to pick the correct one