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FAST FEEDBACK SYSTEM FOR ENERGY AND BEAM STABILIZATION*

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Abstract

The electron beams being delivered to targets of the Continuous Electron Beam Accelerator Facility (CEBAF) at Thomas Jefferson National Accelerator Facility (Jefferson Lab) are plagued with undesirable positional and energy fluctuations. These fluctuations primarily occur at harmonics of the power line frequency (60, 120, 180, etc. hertz), and their cause is rooted in electromagnetic fields generated by accelerator electronic equipment. It is possible to largely nullify these deviations by applying real time corrections to electromagnets and RF verniers along the beam line. This concept has been successfully applied at Jefferson Lab by extensively modifying the existing Beam Position Monitor (BPM) system with the integration of an algorithm that computes correction signals targeted at the power line harmonics. Many of the modifications required were due to the existing CEBAF BPM system not having the data acquisition bandwidth needed for this type of feedback system. This paper will describe the techniques required to transform the CEBAF standard BPM system into a high speed practical fast feedback system that coexists with the large scale control system - the Experimental Physics and Industrial Control System (EPICS) - that runs the CEBAF accelerator in daily operation.

1 INTRODUCTION

Spectral density studies of both beam energy fluctuation and transverse motion have shown densities primarily at power line harmonics up to 720 Hz. Uncorrected RMS energy fluctuations of about 10^{-4} and motion of 0.2 mm are common. The beam motion and energy stability required by experimenters are about ten times lower.

Both analog and digital feedback systems were considered to solve this problem. Generally, an analog system is less susceptible to electronic noise. However, with averaging and proper filtering of digital data, the noise level of the digital system can be reduced to acceptable levels. In addition, a digital system suggested a number of other advantages. First, it offered the possibility of spurious input rejection, which an analog system would not. Second, it could be built by modifying the existing BPM system [1], thereby saving a large portion of the cost developing an analog system would have incurred. Third, a digital system could also offer greater flexibility for possible future enhancements and modifications. For these reasons, it was decided to implement a digital system.

The EPICS based control system provides a graphic operator interface running on UNIX workstations connected via a Local Area Network (LAN) to a VME bus embedded processor [2]. An embedded processor, referred to as an Input/Output Controller (IOC), performs all BPM data acquisition using a VME bus interface to a combination of commercial and locally developed hardware. After data acquisition and initial processing by the IOC, BPM data are transferred over the LAN to the operator interface for visualization.

The BPM IOCs modified for feedback are configured to house a maximum of eight BPM channels, each composed of two perpendicular pairs of antennae from which horizontal and vertical beam position can be calculated. Raw BPM data are acquired using multiple four-channel 2 MHz 12-bit VMIC-3115 analog to digital converter (ADC) cards.

The computers used for BPM IOCs are 50 MHz Motorola 68060 based Motorola MVME-177 single board computers. The BPM system operates on a 60 Hz frame rate synchronized with a digital accelerator global timing reference referred to as the *beam synch*. The beam synch initiates a previously armed data acquisition cycle within the BPM system hardware. This cycle proceeds autonomously until completion, causing the ADC to assert an interrupt to the IOC, further resulting in ADC data download, data processing, and LAN uplink to the operator interface workstations. The BPM IOC also respond asynchronously to configuration commands transmitted via the LAN from the operator interface.

2 FEEDBACK ALGORITHM

The spectral density of beam motion determines the required bandwidth of the system. On one hand, higher bandwidth results in better suppression of beam motion. On the other hand, it increases beam motion related to BPM noise, degrading performance at small beam currents (< 10 uA). To satisfy these contradictory options, the sampling frequency of the system was required to be in the range of 2-5 kHz, while additional noise rejection and suppression of power line harmonics were determined by the type of digital filter chosen. A realistic frame rate of 3 kHz was selected as an objective. Given the existing BPM system's frame rate of 60 Hz, 3 kHz still represented a significant implementation challenge.

The feedback algorithm is capable of computing corrections suppressing beam motion from 0 to 80 Hz and also provides narrow band suppression of the first three

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power line harmonics [3]. This algorithm is based on a recursive digital filter. An additional feedforward loop, integrated with the feedback algorithm, is capable of suppressing narrow band motion from the forth to twelfth power line harmonics and also improves the suppression of the first three harmonics.

The processing frame of the feedback system is composed of BPM hardware data acquisition, ADC data fetch and preprocessing, correction computation, and output of the corrections to Digital to Analog Converters (DAC) that drive beam energy and position correction hardware.

For the feedback algorithm to reject beam motion at power line harmonics, the processing frame requires phase synchronization with the power line's 60 Hz. Therefore frame rates are to be harmonic multiples of 60. Processing of the first frame within a group of this multiple begins upon receipt of the beam synch signal. The feedback computations must complete within each processing frame.

The feedback algorithm requires DAC outputs to occur with temporal determinism relative to the start of a processing frame in order to function with stability. This presents a challenge given the asynchronous nature of LAN interrupt processing within the BPM EPICS IOC. In order to implement the feedforward loop, DAC outputs are required at a higher rate than the data acquisition. Three times the frame rate was chosen as an objective. These outputs are evenly spaced in time and again are fixed with respect to the frame.

3 BPM SYSTEM MODIFICATIONS

3.1 Goals

The standard BPM system required modification to both hardware and software in order to function as an operational feedback system. Achieving the requirements of the feedback algorithm as stated in the previous section were the primary goals of the modifications. Additionally, the core functionality of the standard BPM system, including the display of beam orbit, needed to be maintained during feedback operation. Potentially, the feedback system would be operated continuously and therefore needed to be reliable in its operation and require minimal user intervention.

Since the desired data acquisition rate of the feedback system was fifty times that of the standard BPM system, real time frequency and time domain data visualization would significantly extend applications of the system.

3.2 Implementation

In order to allow correction of beam energy fluctuations, the beam line optics were modified to create a highly dispersive region near one of the feedback system's BPMs. Using position data from this BPM, beam energy information is calculated.

Figure 1 depicts a schematic representation of the fast feedback BPM system. A dual computer approach was required in order to meet the system timing objectives. The first processor performs all EPICS functionality including asynchronous LAN communication. The second processor performs all fast feedback functions including BPM data acquisition and corrector output. The two computers are programmed to communicate command, status, and real time BPM data across a Chrislin Industries CI-VME80 32 megabyte VME shared memory board. BPM data is further processed by FFT on the EPICS computer for real time operator display without affecting the performance of the feedback computer.

The 60 Hz beam synch signal is fed into a Mizar 8310CTM digital timer card. This card is programmed to provide power line synchronized VME bus interrupts to the feedback computer at the desired frame rate. These interrupts are used by software to trigger frame start for the feedback data acquisition and processing.

The Mizar timer card, with the use of interrupts, also schedules the timing of feedback correction output. Feedback corrections are output to two 12-bit four-channel VMIC 4150 DAC cards. The resulting analog signals are filtered using a Frequency Devices VM8PF programmable low-pass filter. This filter rejects high frequency harmonics excited by step function dependence in DAC output voltage. Signals output from the filter card drive magnets for position correction and vernier inputs to RF cavities for energy correction.

Initially, the platform for the feedback computer was an MVME-177, identical to the EPICS processor. This platform provided a usable, but not optimal, feedback frame rate of 1500 Hz. This computer was eventually upgraded to a Motorola MVME-2700 utilizing a 366 MHz PowerPC 750 processor. Even the 1500 Hz rate using the MVME-177 was not achieved without first employing the techniques described below to maximize the real time performance of this system.

BPM digital data transfer, per frame, from the system's two ADCs consists of 128 16-bit words (12-bit data ex-

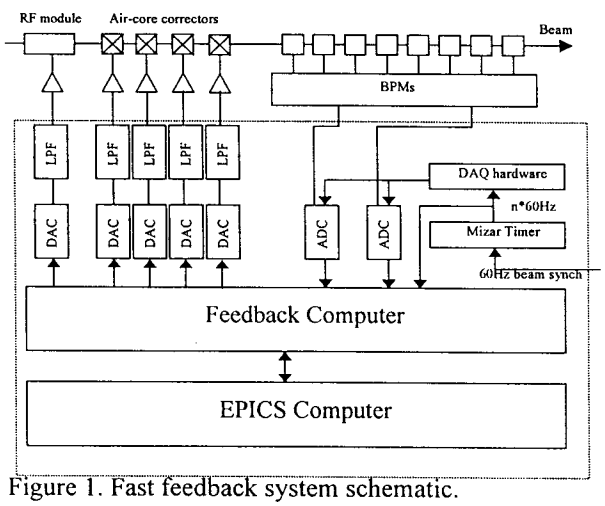

Figure 1. Fast feedback system schematic.

tended to 16-bit). The standard BPM system software simply performs a word-wise loop copy of this data across the VME bus into a local buffer. Using a VMETRO VBT-325 VME bus analyzer it was found that per word transfer time for this approach took approximately 2 microseconds, resulting in a total transfer time of over 500 microseconds. Obviously this placed severe restrictions on the ultimate performance of the feedback system. Analysis showed that the ADC card was able to place data on the bus 500 nanoseconds after a valid address strobe was asserted. Bus arbitration and loop processing were consuming the remaining 1.5 microseconds. This implied the potential of a four-fold increase in transfer speed. Expanding loops into inline code (loop unrolling) reduced the per word transfer time to 1.2 microseconds, still leaving room for improvement. The VME interface circuitry of the MVME-177 contains a direct memory access (DMA) engine that was then employed in place of the processor copy technique. A transfer time of 600 nanoseconds per word was achieved allowing a total transfer from both ADC's in 150 microseconds. The MVME-2700 computer also contains a VME DMA engine and similar transfer times were achieved with it.

For each frame, sets of eight 16-bit data values from each BPM antennae are averaged to produce a single value with reduced noise characteristics. As a result, the system can operate with a beam current as low as one uA.

This averaging imposed the potential for a large processing burden on the feedback system so steps were taken to minimize its impact. Averaging of data from the first ADC card is scheduled to occur while DMA from the second card is still underway. By doing this, it is possible to take advantage of otherwise unused processor cycles. Both the Motorola 68060 and PowerPC 750 processing units are capable of 32-bit integer arithmetic. By performing 32-bit arithmetic using two 16-bit data values simultaneously, the time required for averaging is reduced by half. Carry effects from one word to the other are eliminated by placing the ADC into an offset binary mode (-10V:0V:10V represented as 0:2048:4095 ADC counts, respectively) thereby assuring the upper four bits of each word remain zero.

Since this system is not memory bound, loop unrolling offers processing performance improvements. This technique could potentially be detrimental to performance if cache misses increase as a result of the expanded code size, but for this system the code segment completely fits within the MVME-2700 level two cache and almost entirely within the PowerPC 750 level one cache.

Software for this system is written in the C programming language. Perhaps going against the grain of modern software engineering practices, function usage is often avoided in favor of in-line code in order to avoid even the minimal call overhead. Similarly, global variable references are preferred to formal parameter passing as a means of function data passing in order to minimize stack push references.

The C language keyword *register* is employed for repetitively used data and constants as much as practical. Analysis of disassembled object code was often necessary in order to judge the effectiveness of this technique.

Wind River Systems' VxWorks real time operating system is used for this system. A small bootstrap program located in non-volatile memory loads the VxWorks code image across the LAN prior to booting. It was therefore impractical to disconnect the LAN from the feedback processor in order to eliminate asynchronous responses to their interrupts. Instead, the feedback software disables LAN interrupts after startup. The LAN interrupt can later be re-enabled for diagnostic purposes via an operator selected EPICS command. This allows remote login capability using telnet.

The feedback data acquisition and algorithm executes within a VxWorks task spawned with the highest system priority. This eliminates preemption of all but interrupt service routines. BPM data gathered by this task are copied to the VME shared memory by a separate task of lower priority. Enough spare time is available while the high priority feedback task waits for timer interrupts in order to allow completion of the VME copy. This copied data are then processed as required by the EPICS computer.

Significant effort was placed into the design of EPICS control screens for the feedback system. The goal was to place all commonly utilized controls on a single screen, while allowing more complicated expert screens to be readily available. Comments were solicited from the accelerator operators regarding prototype versions of these screens prior to completion of the current version. A very useful screen developed for the feedback system displays FFT plots of beam position in real time with continuous updates.

4 RESULTS

The system is now fully operational in two of the three CEBAF experimental hall beam lines and offers good suppression of energy and beam motion fluctuations at power line harmonics up to 720 Hz using a frame rate of up to 3 kHz. Energy correction of better than 10^{-4} and beam spot size of 20-30 microns RMS were achieved. The system is reliable and requires minimal operator intervention. This level of reliability would not have been easily possible without the use of the VME bus analyzer for detailed bus timing and computer-to-computer communication studies.

5 REFERENCES

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