MSELV Development Plan

Date: January 8, 2020
Time: 9:00AM– 9:30AM

Attendees: Aaron Brown, Ruben Fair, Probir Ghoshal, Pablo Campero, Tyler Lemon, Nick Sandoval

1. Goal of MSELV Chassis project
    - 1.1. Develop a sensor and voltage tap readout that uses open-source software, is cost-effective, and is modular.
    - 1.2. Use MSELV for several upcoming projects (Moeller, JLEIC)

2. Discussed current status.
    - 2.1. Specification for "next-generation" MSELV defined and under review.
        - 2.1.1. Will be distributed once reviewed.
    - 2.2. DSG has investigated DE0-Nano-SoC with Cyclone series FPGAs and found problems with FPGA-HPS bridge needed to communicate between MSELV and Ethernet devices.
        - 2.2.1. A different FPGA board will be investigated since DE0-Nano-SoC does not seem to be working as expected.
    - 2.3. DSG has started looking at and developing with a National Instruments single-board compact RIO (sbRIO) as a potential replacement for Cyclone FPGAs.
        - 2.3.1. Concerns expressed over sbRIO still being a National Instruments platform relying on LabVIEW and since presently used LV cRIO has been a weak point in the magnet controls system.

3. MSELV chassis with presently used components will be procured.
    - 3.1. Chassis could be used a spare and for projects in near future.