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RICH-II Hardware Interlock System

I am working on the LabVIEW program for the RICH-II hardware interlock system. I worked on ensuring that the channel mapping for sensor readout lets us read the sensors in sequential order, relative to where the sensors are connected to the backplane PCB. This makes it significantly easier to correlate sensor numbering schemes. For example, Sensor 1 will be read by Port 1 on the backplane PCB and so on.

I addressed the channel mapping by first seeing the order (respective to the backplane PCB) that the sensors are read in and therefore what sbRIO digital input/outputs (DIOs) are used for each port. This did not necessarily correlate to Sensor # *X* being read by Port # *X*, since the ordering of channels was determined by signal traces during PCB design – the signal traces were routed in ways that prevented any issues (shorts between traces, more direct traces without a lot of maneuvering around parts, etc.). After determining what sbRIO DIOs are used for each sensor, I reassigned the order of readout for the DIOs to ensure that the sensors are read out sequentially on the backplane PCB.

There were few, if any, problems encountered in this task. Mainly, the task was very tedious, since any mistake would require recompilation of the FPGA portion on the sbRIO, which takes ~20 minutes each time. I minimized the chance of mistakes by creating two subVIs, one for controlling the sensors' clock signals and one for controlling/reading from the sensors' data signals. Using these subVIs over the basic channel write/read controls let me only have to verify the channel assignment in two places (the subVIs) vs. everywhere the channel write/read is used.

As of January 18, 2022, this task has been completed and all channels are now read sequentially relative to the backplane PCB.

Next month, I plan to add in network shared variable and EPICS capabilities to the LabVIEW program to remotely monitor parameters measured by the hardware interlock system and also to provide data to existing EPICS infrastructure in Hall B for alarm handling and archiving.