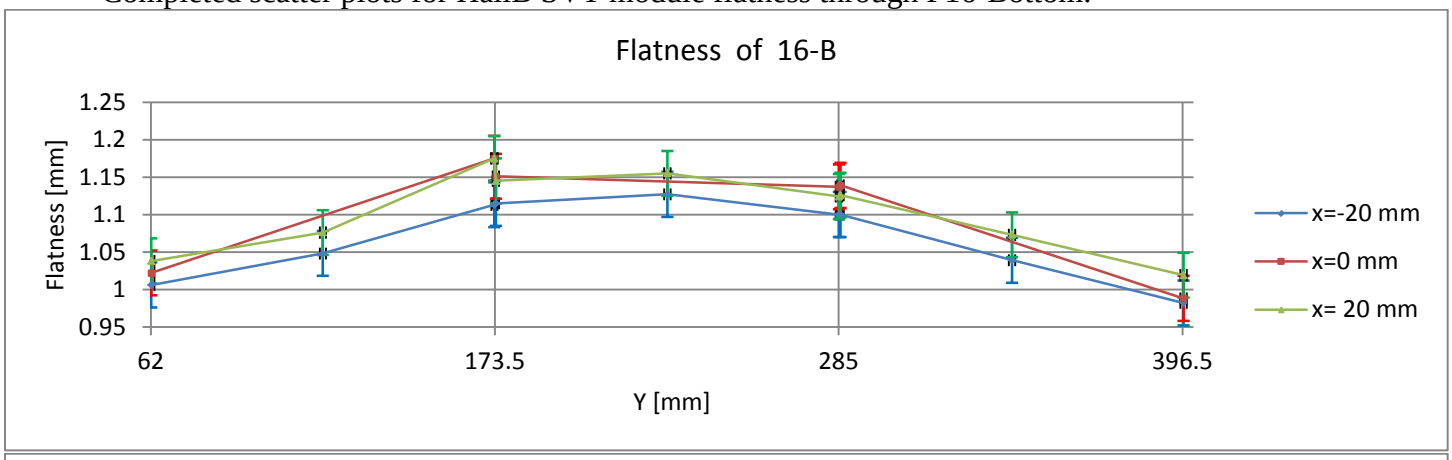
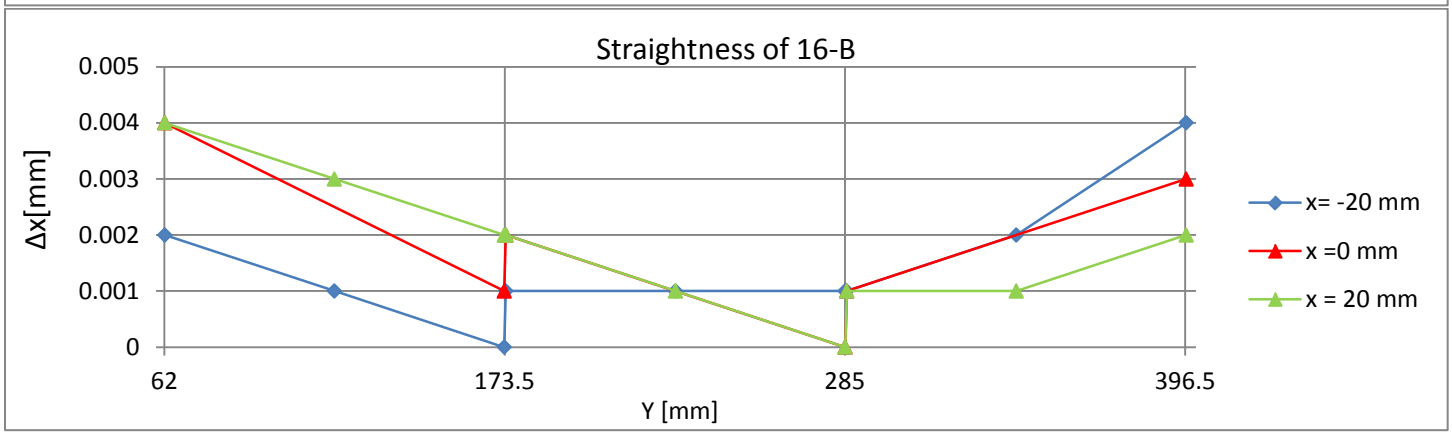
DSG Meeting Minutes – Wednesday, May 21, 2014

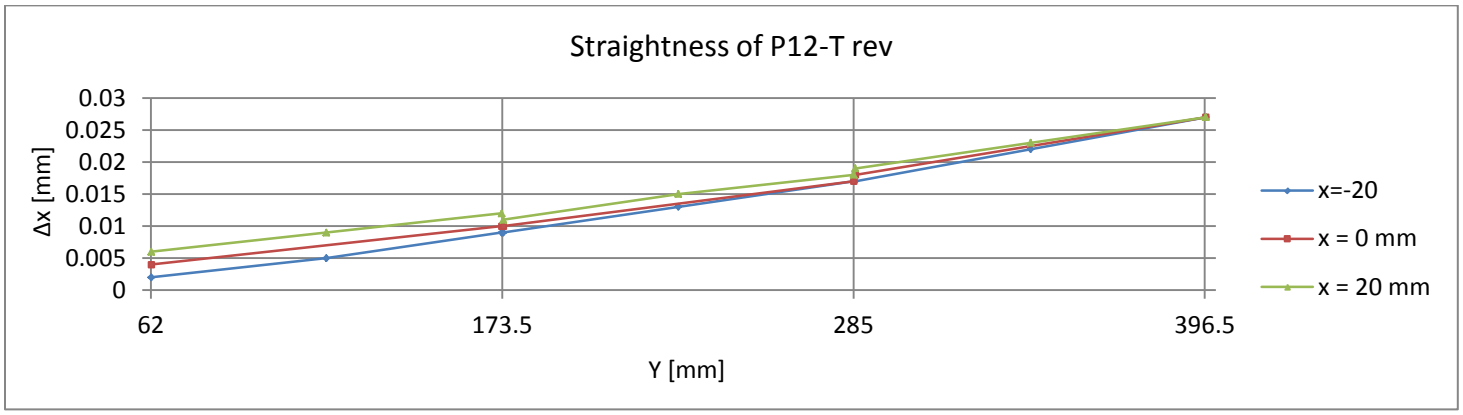
Antonioli, Mary Ann:

- Drew in Visio Fill-Target and Empty-Target flowcharts for Hall D slow controls.
- Completed scatter plots for HallB SVT module flatness through P16-Bottom.





  - The flatness and straightness of module 16-B are in spec.
- Made additional plots of delta x and delta y for P12-Top and P12-Top Rev.



  - The straightness of module 12 top is out of spec (Δx greater than 20 μm).
- Completed HV cables 4, 5, and 6.

Bonneau, Peter:

- Presented to Patrizia Rossi the advantages of PAC's over PLC's.
  - Showed that PAC's (cRio) improvements in hardware and software development tools make these systems superior to PLCs in all new control applications.
  - Provided supporting documentation regarding PAC advantages.

  - Provided information on how PACs are being used in other physics labs: CERN, Los Alamos, Fermilab, Oak Ridge, and Brookhaven.
  - Our group, DSG, has software, infrastructure, and experience with LabVIEW and PAC's.
- Continued compiling and writing requirements for the SVT EPICS-based slow controls system.
  - Includes a complete hardware list with module specifications.
- Attended the SVT project schedule variance meeting.
  - Reviewed and documented reasons for the 350K schedule variance on the SVT project.
  - About seventy percent of the variance is due to the manufacturer's delay in HFCB production, ~30% due to delayed mechanical P6 ID's.
- Organized Rockwell PLC training for Dave, Werth and I.
  - The training is on June 4-5 at the Greensboro N.C. Convention Center.
  - Travel has been approved and reservations have been completed.
- Coordinated and debugged programming on Hall D target PLC controls with Dave and Werth.
  - Activities included daily programming strategy meetings.
  - Participated in troubleshooting of the RTD readback between the PLC controller and the Lakeshore 336 Cryogenic Temperature Controller.
- Checked particle count readings in SVT cleanroom to ensure that the exposed SVT modules are in a clean environment.
  - Particle count readings were consistent with the previous measurements. The count for particle sizes larger than 0.05 µm was ~300/ cu-ft
- Discussed with Saptarshi and George the type of SVT gas system controls to procure.
  - Decided on a MKS 447C4R0N four-channel gas controller. This model is consistent with other units in CLAS12 and will have an RS232 interface to the slow controls system.
- Participated in FNAL shift preparation training with Sahin.

Butler, Dave:

- Prepared Hall D for open house.
  - Included FDC display with spare wireboards and cathodes.
- Installed temporary Argon/CO_2 mixture into CDC for flushing.
  - Pressure and flow is being monitored with PLC slow controls.
- Working to make EPIC screens by providing the proper PLC Tags (process variables).
- Refined requirements for the FDC/CDC gas system controls with Benni Zihlman and Mike Staib.
  - Therefore, currently revising the PLC code.
- Provided serial communication code from the FDC gas system to Werth to help with the target controls code scheme.
- Prepared a presentation on the FDC/CDC gas system for the Hall D biweekly controls meeting.

Eng, Brian:

Hall B SVT

- For solid model of cable strain relief on SVT assembly optical table, worked around NX issue of inability to extrude tangent circles.
  - Solution: trim tangent circles into multiple arcs.
- Started new SVT web page: https://www.jlab.org/Hall-B/svt.
- Tested L1C strain relief / mounting plates.
  - Need to change procedure to attach data cable before plates.
- Finally got approval from FM&L to order power strip with circuit breakers and an adapter cable to power chiller.
  - Waiting on parts to be shipped.
- Sent remaining 200 pitch adapters to FNAL (we still have a single sheet in dry box).
- Went over DAQ and L1C cabling with Sahin.
- Re-verified that the interlock capability of MPOD crate is disabled by default, and requires using USB software in Admin mode for enabling. Once enabled, TTL signal high is required to turn on channels, otherwise channels will be inhibited/ramp down.
- Changed elog and testchan programs functionality.

- The testchan program (which creates all the plot files) now saves a summary file for each chip and the elog program doesn't print to the screen messages from testchan, only the summary files.

Jacobs, George:

Hall B

- Requested and received quotes for new DCGAS solenoids.
- Applied for and received new hot work permit to continue welding Hall B DCGAS piping.
  - From 96B into the hall
- QA on R1S1 and R1S2.
  - HV soldering, HV testing, DCRB tests.
- Meeting with Saptarshi about N_2 purge for SVT.
- Started to organize drawings for DCGAS, LTCC, gas, and HTCC gas system piping, components, and controls in order to assign Jlab drawing numbers to them.
- Began planning the layout of the Hall B DCGAS valve panel and associated controls and safety system components.
- Met with Peter about the SVT N_2 purge hardware and controls.
- Updated the plan for DC cleanroom transition from stringing to instrumentation and testing, the critical path for the R1 survey, and the cleanroom floor plan for R1 survey.
- Did two HBlist entries, one for when I am on travel in June to designate a supervisor for the stringers, the other for transporting the R3S4 from the ESB to EEL room 124 cleanroom.
- Closed out the CATS item for EEL clean room.

Leffel, Mindy:

Hall B

- Completed four humidity/temperature sensor boards, up to the plug portion of the disconnect.
- Started working on patch panel layout, marking positions of rails, and verifying that the layout will accommodate the modules.
- Discussed with Peter supplies needed to make a V450 test cable, began research and ordering of components.
- Reworked six PMTs.
- Helped Tina organize work space.

Mann, Tina:

- Worked on Hall B Drift Chambers Region 1 Sector, 1 Region 1 Sector 2
  - Verifying voltages on boards from guard, field, and sense wires to quad connectors.
  - Repairing any quad connectors that need pins replaced due to damage.
  - Trained on connecting signal cables to Drift Chamber and learning to read the Drift Chamber readout plot for troubleshooting connection
- Working on 25-D-Sub for Hall B SVT VME to patch panel.
  - 7 completed
- Installed work station drawers with Mindy.

McMullen, Marc:

Hall B SVT

- Started resistance testing with the Keithley 2002 multimeter and at 250 V on Keithley 237 source meter, 8 of 9 Bus Cable Panels (BCP)
  - Shipped 8 BCPs to Fermi for module production.
- QA-ed 11 HFCBs using the SVT slow controls tests and a Keithley 2002 bench multimeter.
  - Shipped all HFCBs to Fermi for module production.
- Made spreadsheet of HFCBs and Bus Cables.
  - Spreadsheet tracks the delivery of shipments by dates, amounts, and purchase order number.
- Demonstrated the operation of testing a populated HFCB with the SVT slow controls test stand.

Sitnikov, Anatoly:

- Assembled 3 boards (panels): soldered 432 Lemo PCB connectors and 432 Flat Chip resistors.
  - Finished all three boards

Teachey, Werth:

Hall D Target

- Wrote code for the Compact Logix PLC controller, in structured text, to read back the 4 temperature RTDs that are connected to the Lakeshore 336 Temperature Controller.
  - Can read back all 4 channels but still trying to debug why on random read iterations, the PLC return tag gets some "garbage" text.
- Wrote code to set the temperature set points for the "Target Fill" command on the Lakeshore 336 Temperature Controller.
- Writing code to set the temperature set points for the "Empty Target" command on the Lakeshore 336 Temperature Controller.
- Reviewed the "Fill Target with Liquid" flow chart from Mary Ann.

SVT

- Debugged the cRIO temperature read back issue on module slot 4 at Fermilab via SKYPE
  - The slot was reading back the wrong temperature because the negative side of the slow controls cable at the cRIO ADC module was not tied to common.
- Fixed the temperature read back issue
  - All 4 slots were reading back the wrong temperature on the JLab SVT reception test stand. Problem was because all negative sides of the slow controls cables were not tied to the cRIO ADC common.