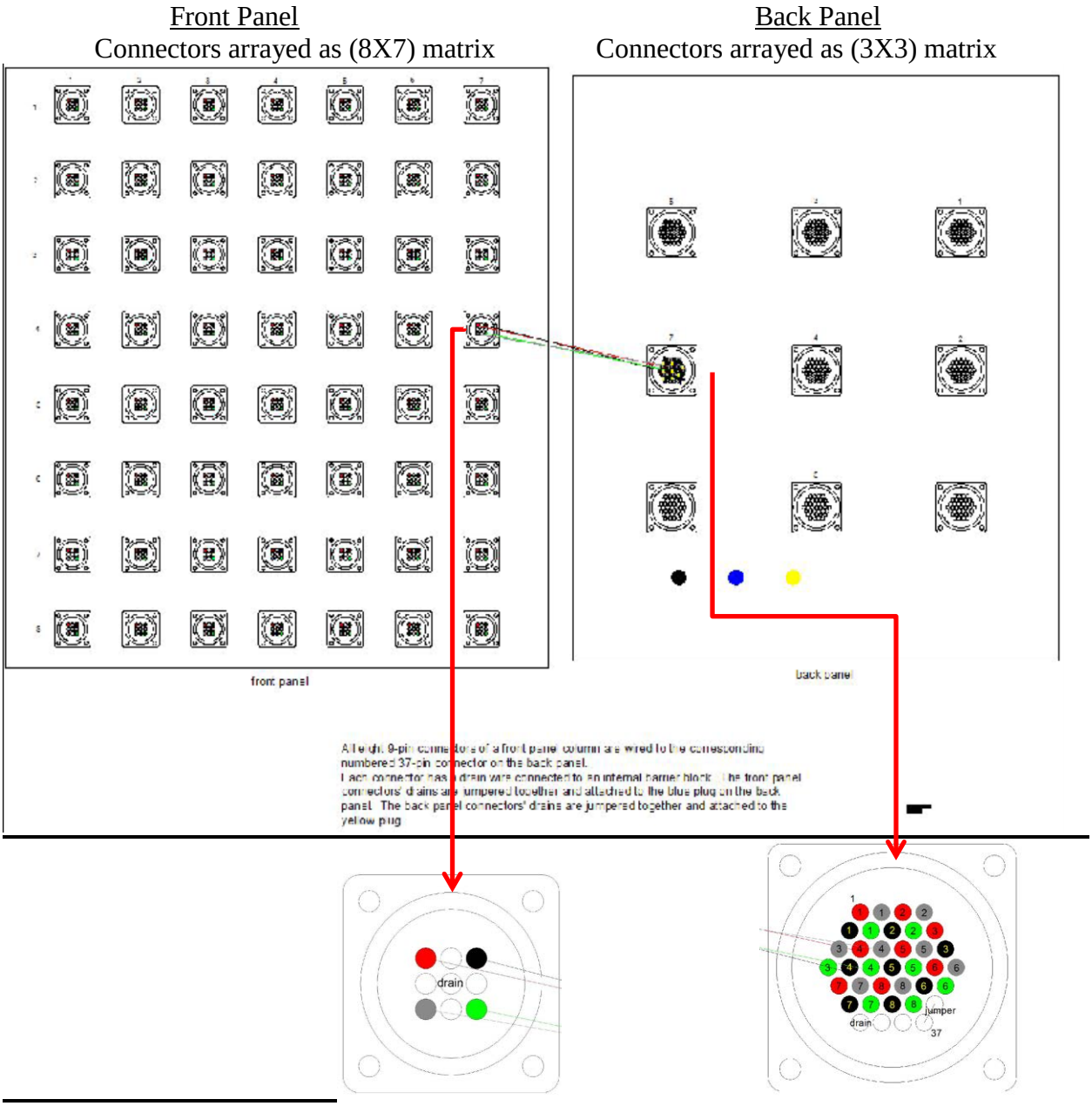
DSG Meeting Minutes – Wednesday, October 8, 2014

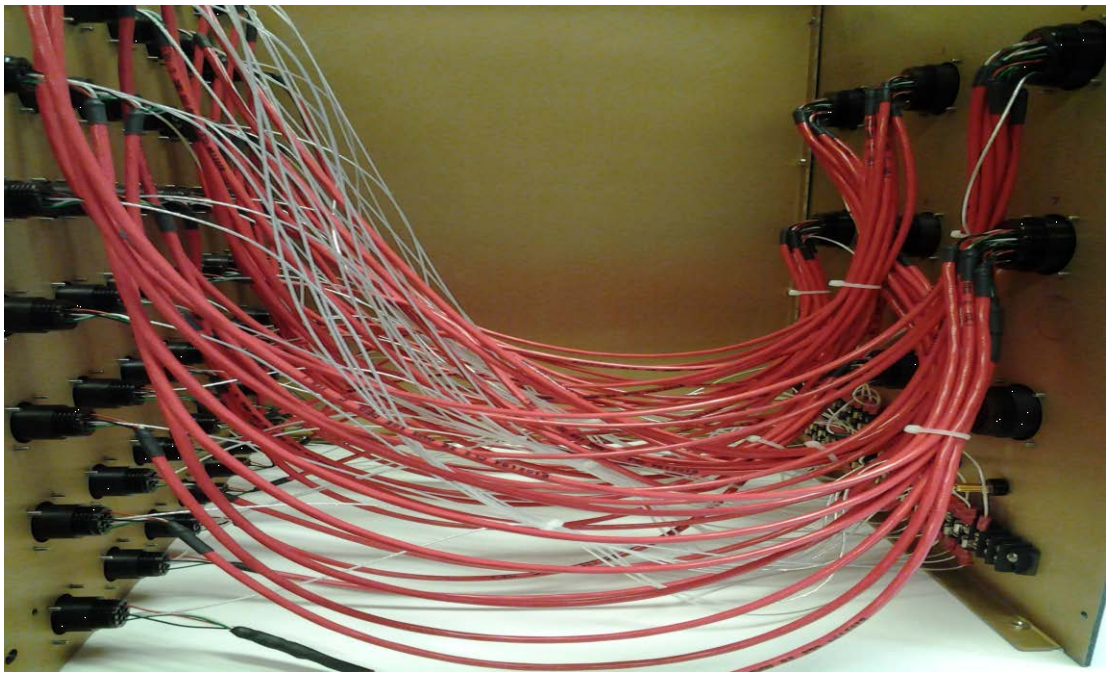
Antonioli, Mary Ann:

Hall B

- Continued data analysis of reflectivity test results for **LTCC**.
- Completed fabrication of **SVT** HV distribution box #4.
- Continued drawing in AutoCAD the design and wiring of **SVT** HV distribution box, to facilitate debugging.



Autocad design of the HV distribution box. In the example above, the front panel connector in row # 4, column # 7 is connected to the pins marked as 4 in the back panel connector #7 located in row # 2, column # 1.



Front Panel Back Panel

Photo of wiring inside the HV distribution box. The red wires contain two *hot* and two *return* wires, a pair for each side of the silicon module; the white wires are the shield wires connected to the terminal block on the back panel.

Arslan, Sahin:

Hall B

- Reception testing, with Brian and Marc, of **SVT** module P8.
- Tested **DC** R3S4 HV and signals with DCRB.
  - HV currents are below 1 µA.
- Laid out and soldered HV cables for **DC** R1S3.
- Installed jumper cables on **DC** R1S3 STB.

Hall D

- Attended **CDC/FDC** presentation.

Bonneau, Peter:

Hall B

- Added requested new feature—*option allowing comparison between a run taken at the end of the day with the first run on the following day*—to the **LTCC** test station.
- Corrected **SVT** sensor database due to assembly mistake at FNAL.
  - The sensors (hybrid, intermediate, far) that were originally assigned to module P56 top were mounted on P57 bottom. To correct the error, the sensors originally designated for P57 bottom were assigned to P56 top. The expected module current calculations in the database were updated to reflect this change.
- Met with and showed Valeri Sytnik the **SVT** Slow Controls System.
  - Instructed and advised Valerie on how to set up the hardware test station configuration which consists of an MVME5500 IOC, mini VME crate, and ADC. Additionally, explained the working of the VXworks boot configuration, V450 driver code implementation, EPICS record types and

fields, ADC initialization settings, and calculations for temperature and humidity, and answered all his questions regarding this matter.

- Started initial testing of **SVT** Slow Controls alarm handler.
  - System responses will be compared to the interlock fault charts for proper operation.
  - R1S10 is the only sector that has some process variables in MyA database; noticed that the response time was 1 min 23 sec for humidity and temp faults to start ramp-down of HV, which typically is a response time of a few of seconds; ramp-down sequence will be investigated.
- Completed re-configuration of Linux test station that was used for **SVT** DAq system testing and troubleshooting with logic analyzer to be used to debug HFCBs and modules.
  - The computer had previously been used as a test station, however due to increased network security, the computer could not communicate with the embedded Linux controllers on the Hall B subnet (86).
  - Problems to debug are: an HFCB that has differential line issues; three modules for which *Out1* fails the register test. The problem appeared first time at the late stage in module assembly; P45 (U3) - after bottom sensors were bonded; P46 (U3) and P55 (U1) - after top sensors were bonded.

Hall D

- Reviewed with Dave the **Solenoid's** LabVIEW with EPICS interface code requirements for the PXI system.
  - To work on this project, another Ethernet/IP LabVIEW add-on package for communication with PLCs is needed.

Butler, Dave:

Hall B

- Discussed with Peter the **SVT** slow controls interface screens and database structure.

Hall D

- Updating **FDC** code to change flow controller set points remotely.
- Gave Mindy an overview of the **FDC** (using the spare package in EEL 126).
- Attended several collaboration talks, including the overall status, engineering update, **slow controls, electronics, and tracking chamber** updates.

Eng, Brian:

Hall B

- Set up cosmic test stand in EEL 231 to test **SVT** modules with pulser line issues (P32, P30).
  - Currently P30 is in the stand taking data with VME controller SVT6. Need to get additional network-based controllers from Sergey when he returns.
- Tested + and - lines on distribution box **SVT** HV 4.
- Began evaluating **SVT** Alarm Handler from ACC group; initial check shows most functions work properly, i.e. modules ramp down on fault. Before connecting modules, more formal testing is needed.

Hall D

- Attended **CDC/FDC** presentation.

Jacobs, George:

Hall B

- Met with David Anderson about internal pipe and hose fittings for **LTCC** detectors.
- Created the gas system piping diagram for internal gas lines and external gas line connections for **LTCC** detectors.
- Updated Bob Miller and Maurizio Ungaro on Hall B **LTCC** gas system installation status.
- Ordered internal pipe and hose fittings for Hall B **LTCC** detectors.
- Mapped out the **gas lines** on L1 Space frame South.

Hall D

- Attended the **Tracking session** of the GlueX Collaboration.

Leffel, Mindy:

Hall B

- Working on 15' jumpers for **Humidity Temperature Sensor Board (HTSB)** cables.
  - Finished one, working on the second one.
- Used the microscope to take pictures of Anatoly's boron silicone fiber for **CTOF**, with both white light and a green laser, shining through the fibers.
- Documented supplies and procedures for the **HTSB** cables/jumpers, for future reference.
- Worked with Sahin in the clean room on the procedure for soldering wires to the **DCs**.

Hall D

- Received an overview of the **FDC** from Dave.

DSG

- Completed the last two, of nine, **network cables**.

Mann, Tina:

Hall B

- Calibrating and testing small Winston cones of the **LTCC**.
  - Tested 27 small Winston cones with UV light.
  - Unpacked and staged small cones for testing in the darkbox.

Hall D

- Checked **FDC-CDC** Gas Panel System.

McMullen, Marc:

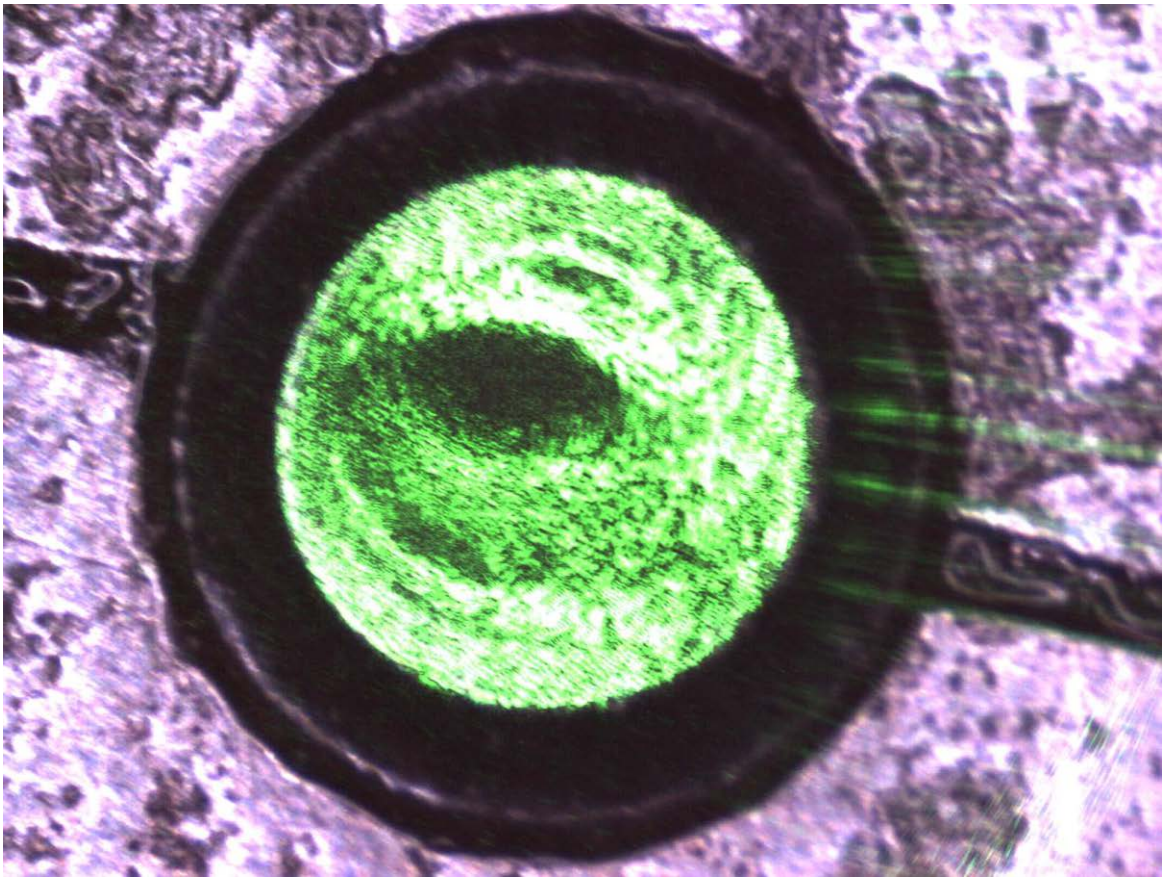
Hall B

- Completed **travel** to Compunetics/Compunetix.
  - Held meeting to discuss the restart of HFCB production.
- QC-ed the repair of **SVT** module P8, HFCB63, 7 bare HFCBs, and 8 populated HFCBs.
  - Sent all 8 HFCBs to Fermi for module production.
- Assisted on reception test training on **SVT** module P8.

Sitnikov, Anatoly:

Hall B

- Completed polishing 124 (diameter 1.4 mm, 29 mm long) boron silicone fibers for **CTOF** calibration system.
- Setting up for cutting 5 m long, 0.3 mm diameter, boron silicone fibers for **CTOF** calibration system.
- Setting up three arrangements for connecting signal connectors with ADC connectors for **PRAD** experiment.



Surface quality of a polished fiber as seen under a microscope. Magnification is ~x10. Dark area indicates transmission loss due to opacity, needs more polishing in that area. Overall quality quite good.

Teachey, Robert Werth:

Hall B

- Reviewed HV wire soldering procedure of the **DC** STBs with Sahin.
- Changed Fermi and Jlab **SVT** module test stand LV current / voltage label swap on the monitor tab.

DSG

- Installed LabVIEW 2013 with updated cRIO drivers to turn cRIO chassis into an **EPICS IOC**.
- Compiled and ran **EDM** on Linux.