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Analog "Latch" Circuit - Operation / Specifications

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Analog "Latch" Circuit
Operation / Specifications

Physics Fast Electronics Group
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Operation
The purpose of the analog "latch" circuit is to pass through a +/-10v signal unaltered and optionally "latch" or hold the signal by applying a TTL latch signal. The circuit provides a glitch free in-line hold function by digitizing the input with a 16-bit ADC then regenerating the signal with a 16-bit DAC. The hold function is implemented digitally by suspending the 55kHz sample clock during the acquisition stage. This latches the digital state thus holding the analog output. The latch command is a positive true, logic high, level sensitive TTL signal that is internally synchronized with the sample clock. The latch input is pulled low with a 5K resistor allowing operation with the TTL source disconnected. The latch input must remain high to maintain the latch, and the latch is released when the latch input is brought low. Gain and offset adjustments are provided at the output stage to correct intrinsic circuit errors. The analog signal can over-range by 0.4v thus extending the dynamic range to +/-10.4v.

Calibration
Calibration is performed after a ½ hour warm-up time. All tests are performed with a 10k-ohm load. Gain and offsets are adjusted to <0.1mV with approx. 5VDC input. The resolution limit of the test equipment is 0.1mV. Offset is first determined by symmetry around 5VDC. Gain is then adjusted to match the input voltage level to less than 0.1mV. Gain and offset are checked at +/-10VDC and offset is checked at 0VDC. Over-range is then verified. Output current is verified at 5mA and 10mA at 5VDC. AC characteristics are then checked with 1kHz, 20Vpp sine and square function inputs. The stability of the latched signal is measured over a 1-hour period.

Specifications / Measurements

+15V supply current	34mA
-15V supply current	34mA
+5V supply current	60mA
Input signal range	+/- 10.48VDC
Gain adjustment	+/- 0.005, 25-turn potentiometer
Offset adjustment	+/- 40mV, 25-turn potentiometer
Input impedance	200K
Input filtering	2-pole, -3db at 4kHz
Output voltage droop at 5VDC	0.0mV at 10K load (0.5mA) 0.5mV at 1K load (5.0mA) 1.0mV at 0.5K load (10.0mA)
Offset calibration error at 5VDC	<0.1mV
Offset error at +/-10VDC	<0.2mV
Offset at 0VDC	<0.4mV
Gain calibration error at 5VDC	<0.1mV
Gain error at +/-10VDC	<0.7mV
Propagation delay with 1.0kHz sine	80uS
Step response time to approx. 100% transition	<200uS
Stability of latched signal over 75min.	<0.1mV
Measured output noise	<1mV
Sample clock period	18uS
16-bit resolution limit over +/-10.4V	320uV
Recommended operating frequency for <10ppm f.s. filter attenuation (calculated)	<50Hz

Figure 1:

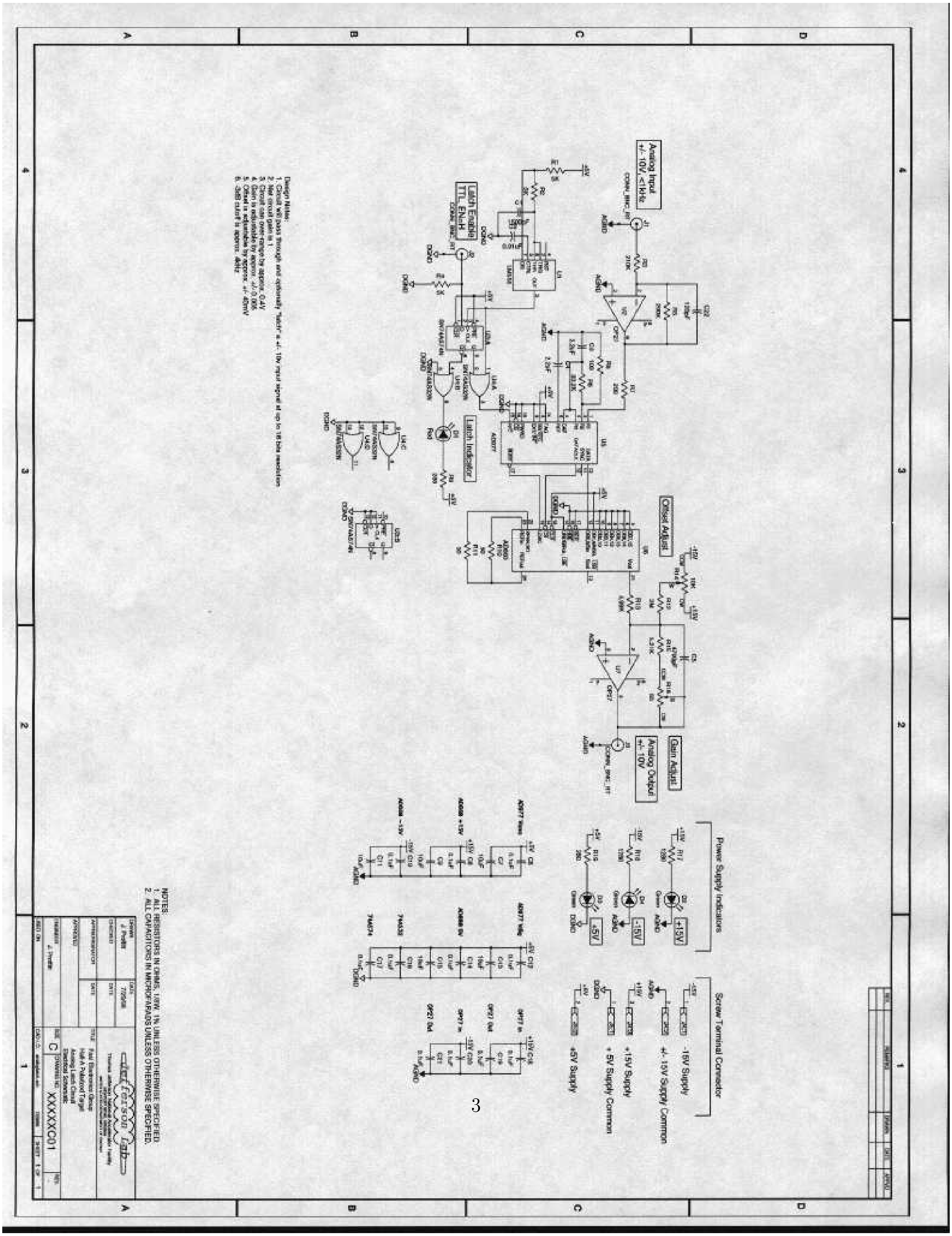
Analog Input +/- 10V, <1kHz
Latch Enable TTL EN=H
Latch Indicator
Offset Adjust
Gain Adjust
Analog Output +/- 10V
Power Supply Indicators
Screw Terminal Connector
XXXXXC01

Figure 2:

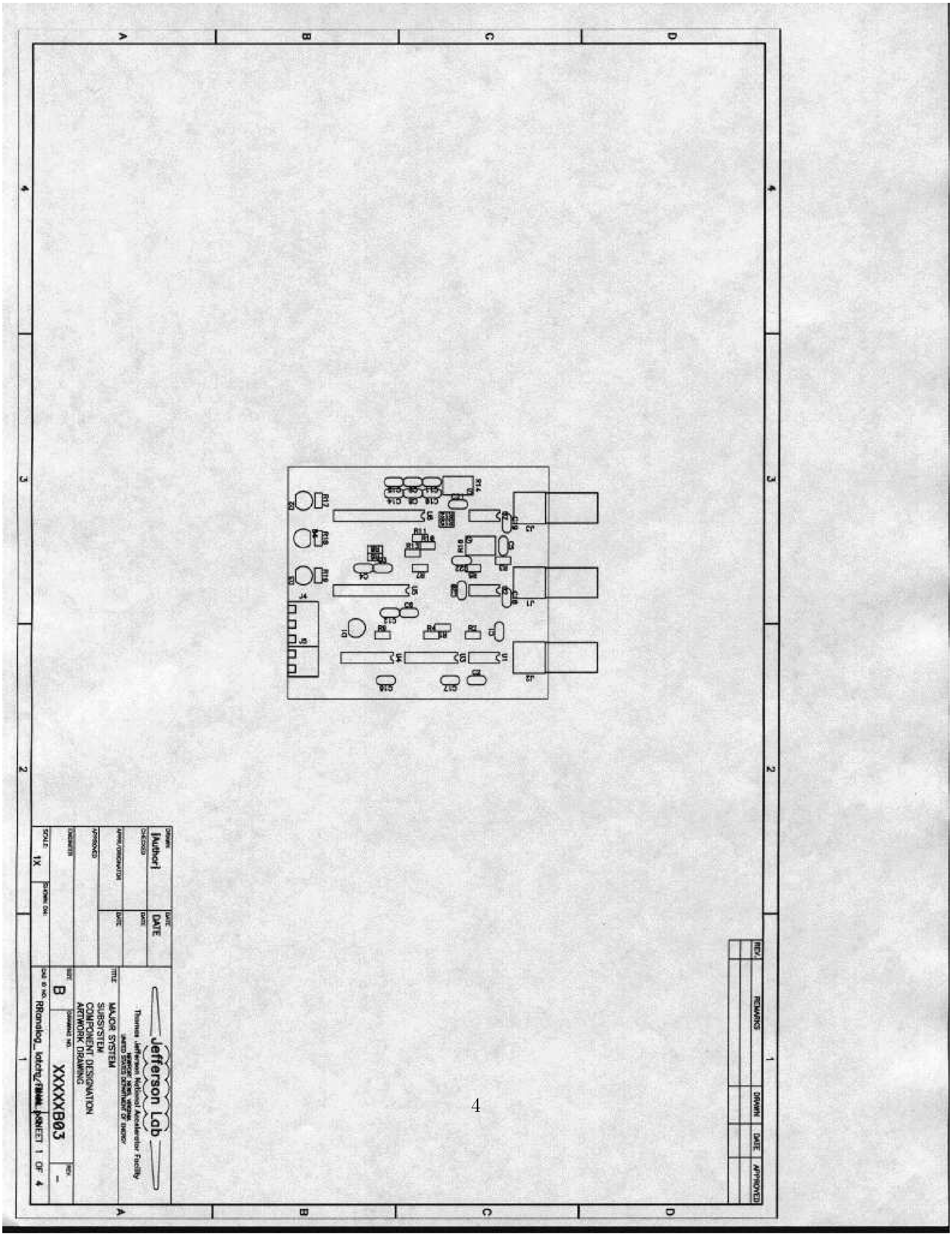
Jefferson Lab
Thomas Jefferson National Accelerator Facility
MAJOR SYSTEM
SUBSYSTEM
COMPONENT DESIGNATION
ARTWORK DRAWING
XXXXXB03
[Author]
DATE
SCALE: 1X
REV.
REMARKS
DRAWN
DATE
APPROVED

Figure 3:

analoglatch.bom

ACCEL Bill of Materials analoglatch.sch

Report Header

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File Design Information:

Title: Analog Latch Circuit
Author: J. Proffitt
Date: 7/29/98
Revision: -

Type	Pattern	Value	Designators
CAP_TA100	CAP100	0.01uF	C2
Qty = 1			
		0.1uF	C6 C8 C10 C12 C14 C16 C17 C18 C19 C20 C21
Qty = 11			
		2.2uF	C3 C4
Qty = 2			
		10uF	C7 C9 C11 C13 C15
Qty = 5			
		120pF	C22
Qty = 1			
		1500pF	C1
Qty = 1			
		4700pF	C5
Qty = 1			
CONN_BNC_RT	CONN_BNC_RT		J1 J2 J3
Qty = 3			
CONN_S2	CONN_S2		J5
Qty = 1			
CONN_S3	CONN_S3		J4
Qty = 1			
LM555	DIP8		U1
Qty = 1			
OP27	DIP8		U2 U7
Qty = 2			

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Figure 4:

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SN74AS32N Qty = 1	DIP14		U4
SN74AS74N Qty = 1	DIP14		U3
AD977 Qty = 1	DIP20		U5
AD660 Qty = 1	DIP24		U6
LED Qty = 3	LED100	Green	D2 D3 D4
Qty = 1		Red	D1
POT_3299Y Qty = 1	POT6T	10K	R14
Qty = 1		50	R16
RES Qty = 1	RES300	2M	R12
Qty = 1		4.99K	R13
Qty = 3		5K	R1 R2 R4
Qty = 1		5.21K	R15
Qty = 1		33.2K	R6
Qty = 2		50	R10 R11
Qty = 1		100	R8
Qty = 1		200	R7

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Figure 5:

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	200K	R5
Qty = 1		
	210K	R3
Qty = 1		
	280	R9 R19
Qty = 2		
	1280	R17 R18
Qty = 2		

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Figure 6: