

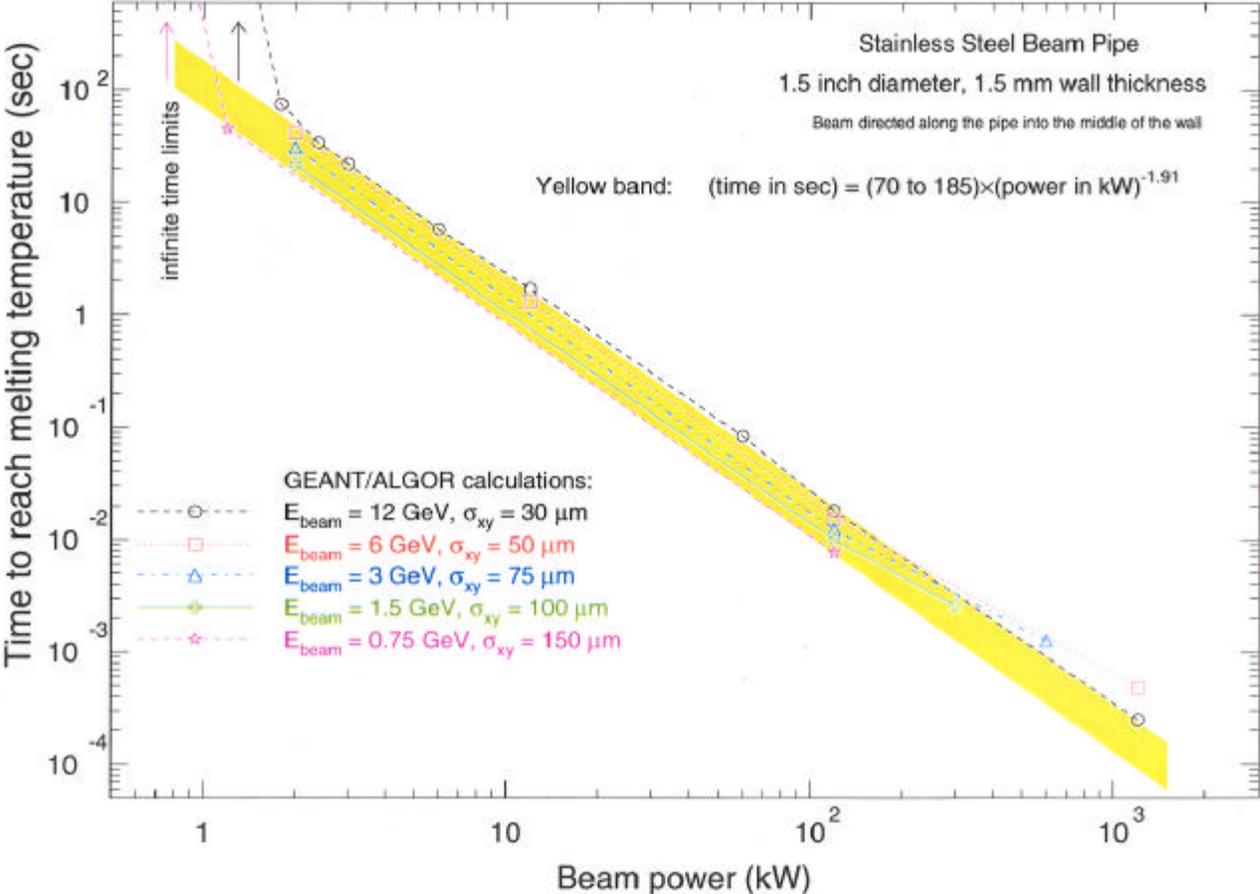
Digital Receivers at Jefferson Lab

John Musson
EID Group

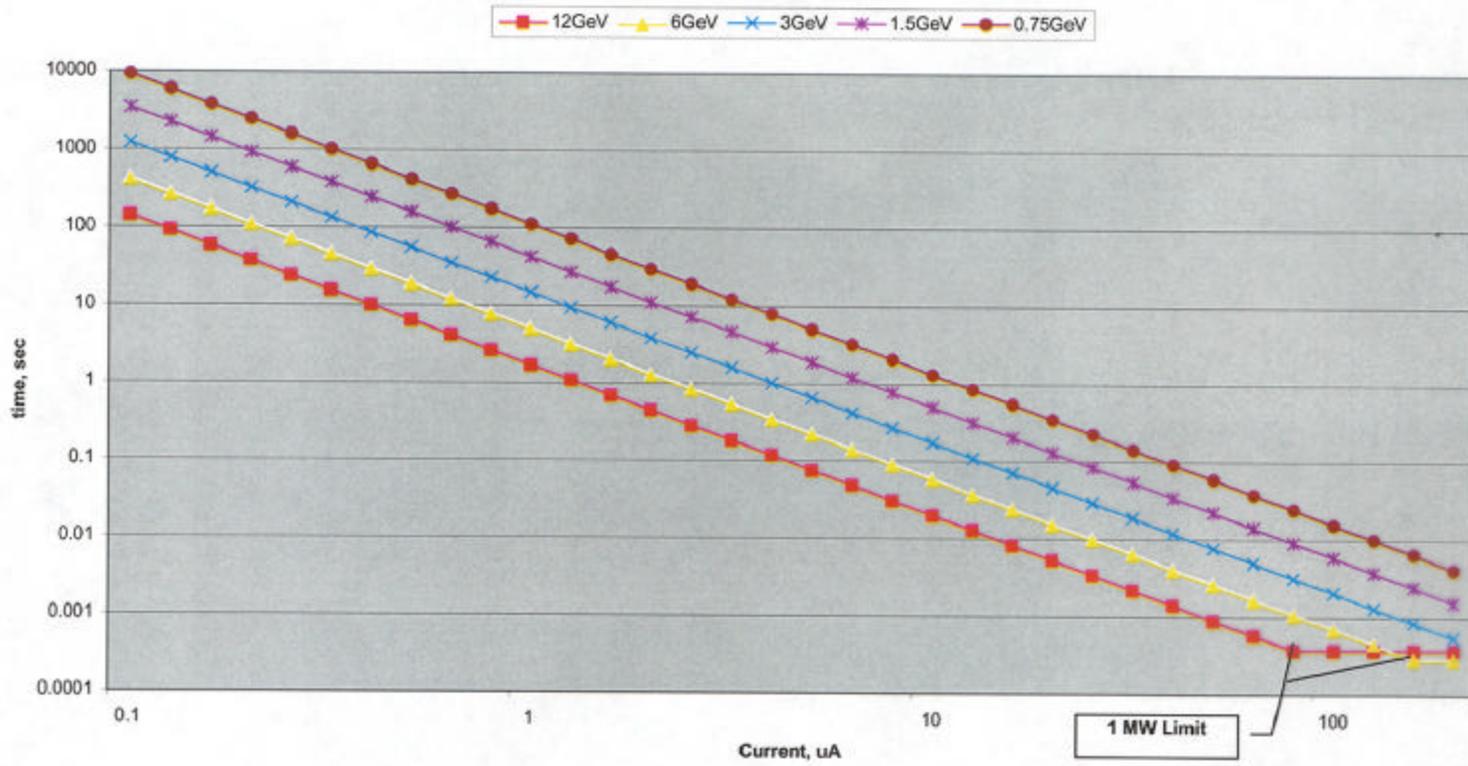
Genesis.....

- **BLA BCM System upgrade**
 - Current system 100 % analog
 - Linearity > 1%
 - High maintenance
 - No stationkeeping or calibration
 - Eroding operator confidence
 - Clunky EPICS interface

Electron beam incident on a beam pipe

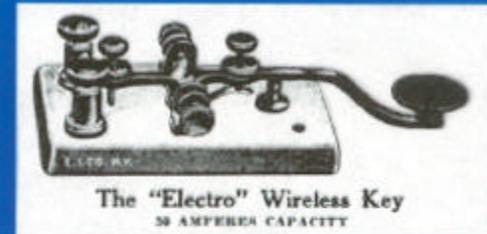


Burn Through Time vs. Current



Old Dogs, New Tricks.....

- Educating "Sparkys!"
 - Collaboration with local University
 - CNU-taught DSP Fundamentals
 - TI DSP Workshops
 - Eval kits, tools
 - Vendor assistance
 - DSK Board + related tools
- Shop around, and dive in!!!



Hybrid System

- Analog RF downconverter
 - Radiation concerns
- Oversampled 3 Mhz IF
- Intentional 1 kHz mistuning
 - Facilitate adaptive filtering in DSP
- VME bus
 - Limited IOC and EPICS interface
- JTAG
 - Full RX and DSP control

The Receiver

- 14 bits < 0.01 % linearity F.S.
- MDS (@ 13 dB S/N) < 100 nA
- Dynamic range > 77 dB (> 400 uA I max)
- 50 MHz input sample rate
 - Expands dynamic range, minimizes N.F.
- On-board noise reference
 - Permits absolute calibration
 - N.F. monitoring (between FSD events)

Detailed Description

Control Interface

The CLC5902 is configured by writing control information into 148 control registers within the chip. The contents of these control registers and how to use them are described in Table 5. The registers are written to or read from using the D[7:0], A[7:0], CE, RD and WR pins (see Table 1 for pin descriptions). This interface is designed to allow the CLC5902 to appear to an external processor as a memory mapped peripheral. See Figure 14 for details.

The control interface is asynchronous with respect to the system clock, CK. This allows the registers to be written or read at any time. In some cases this might cause an invalid operation since the interface is not internally synchronized. In order to assure correct operation, SI must be asserted after the control registers are written.

The D[7:0], A[7:0], WR, RD and CE pins should not be driven above the positive supply voltage.

Master Reset

A master reset pin, MR, is provided to initialize the CLC5902 to a known condition and should be strobed after power up. This signal will clear all sample data and all user programmed data (filter coefficients and AGC settings). All outputs will be disabled (tri-stated). ASTROBE and BSTROBE will be asserted to initialize the DVGA values. Table 5 describes the control register default values.

Synchronizing Multiple CLC5902 Chips

A system containing two or more CLC5902 chips will need to be synchronized if coherent operation is desired. To synchronize multiple CLC5902 chips, connect all of the sync input pins together so they can be driven by a common sync strobe. Synchronization occurs on the rising edge of CK when SI goes back high. When SI is asserted all sample data will be flushed immediately, the numerically controlled oscillator (NCO) phase offset will be ini-

tialized, the NCO dither generators will be reset, and the CIC decimation ratio will be initialized. Only the configuration data loaded into the microprocessor interface remains unaffected.

SI may be held low as long as desired after a minimum of 4 CK periods.

Input Source

The input crossbar switch allows either AIN, BIN, or a test register to be routed to the channel A or channel B AGC/DDC. The AGC outputs, AGAIN and BGIN, are not switched. If AIN and BIN are exchanged the AGC loop will be open and the AGCs will not function properly. AIN and BIN should meet the timing requirements shown in Figure 7.

Selecting the test register as the input source allows the AGC or DDC operation to be verified with a known input. See the test and diagnostics section for further discussion.

Down Converters

A detailed block diagram of each DDC channel is shown in Figure 15. Each down converter uses a complex NCO and mixer to quadrature downconvert a signal to baseband. The "FLOAT TO FIXED CONVERTER" treats the 15-bit mixer output as a mantissa and the AGC output, EXP, as a 3-bit exponent. It performs a bit shift on the data based on the value of EXP. This bit shifting is used to expand the compressed dynamic range resulting from the DVGA operation. The DVGA gain is adjusted in 6dB steps which are equivalent to each digital bit shift.

The exponent (EXP) can be forced to its maximum value by setting the EXP_INH bit. If $x_{in}(n)$ is the DDC input, the signal after the "FLOAT TO FIXED CONVERTER" is

$$x_2(n) = x_{in}(n) \cdot \cos(\omega n) \cdot 2^{EXP} \quad \text{EQ. 1}$$

for the I component. Changing the 'cos' to 'sin' in this equation will provide the Q component.

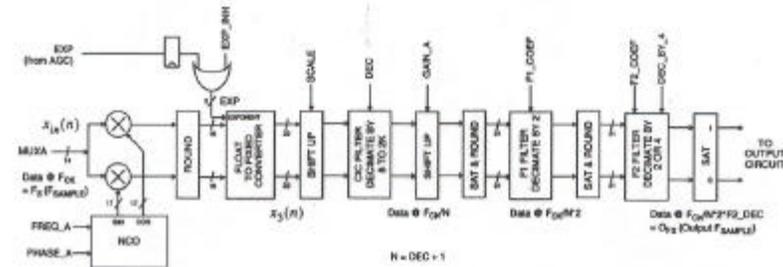
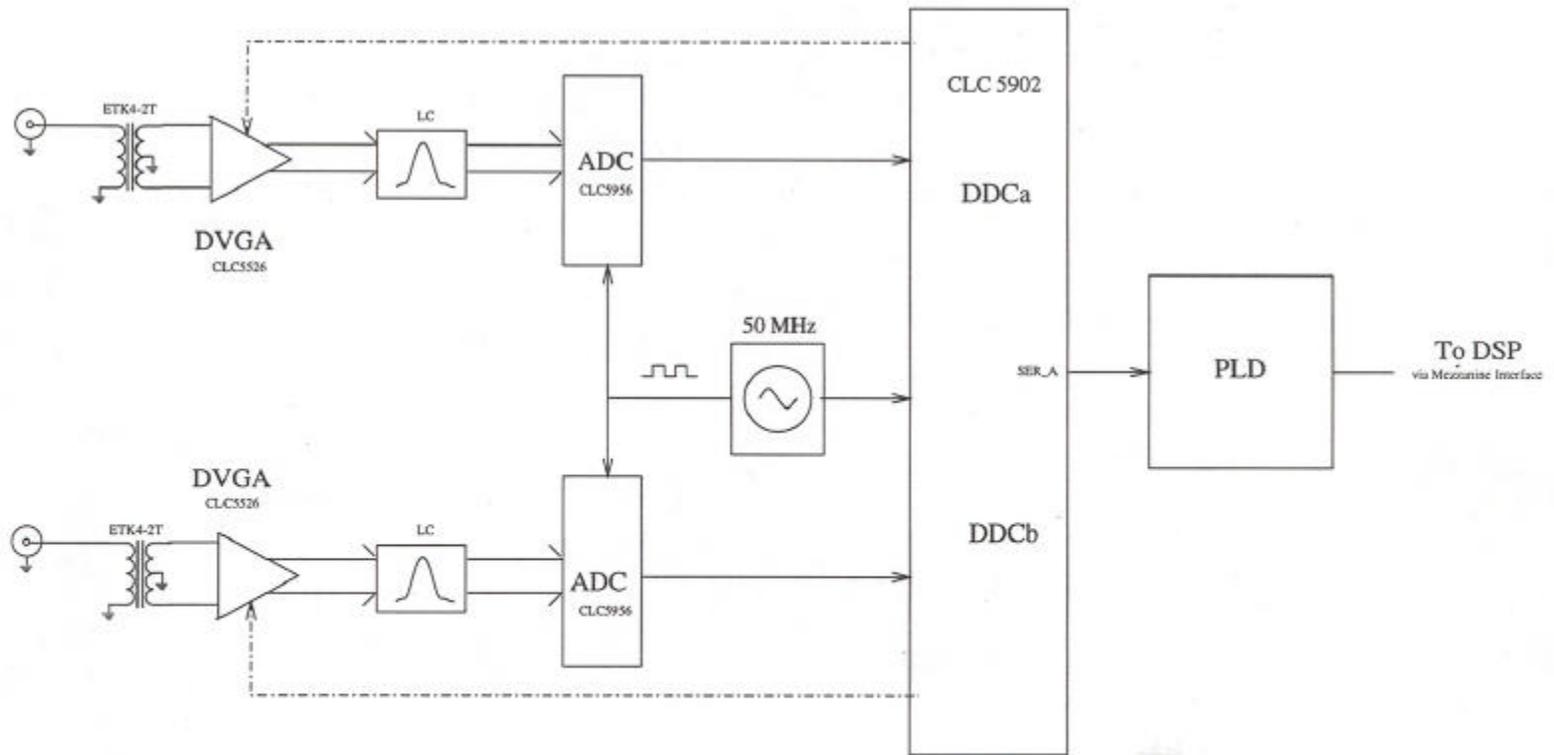


Figure 15 CLC5902 Down Converter, Channel A (Channel B is identical)



Group Delay

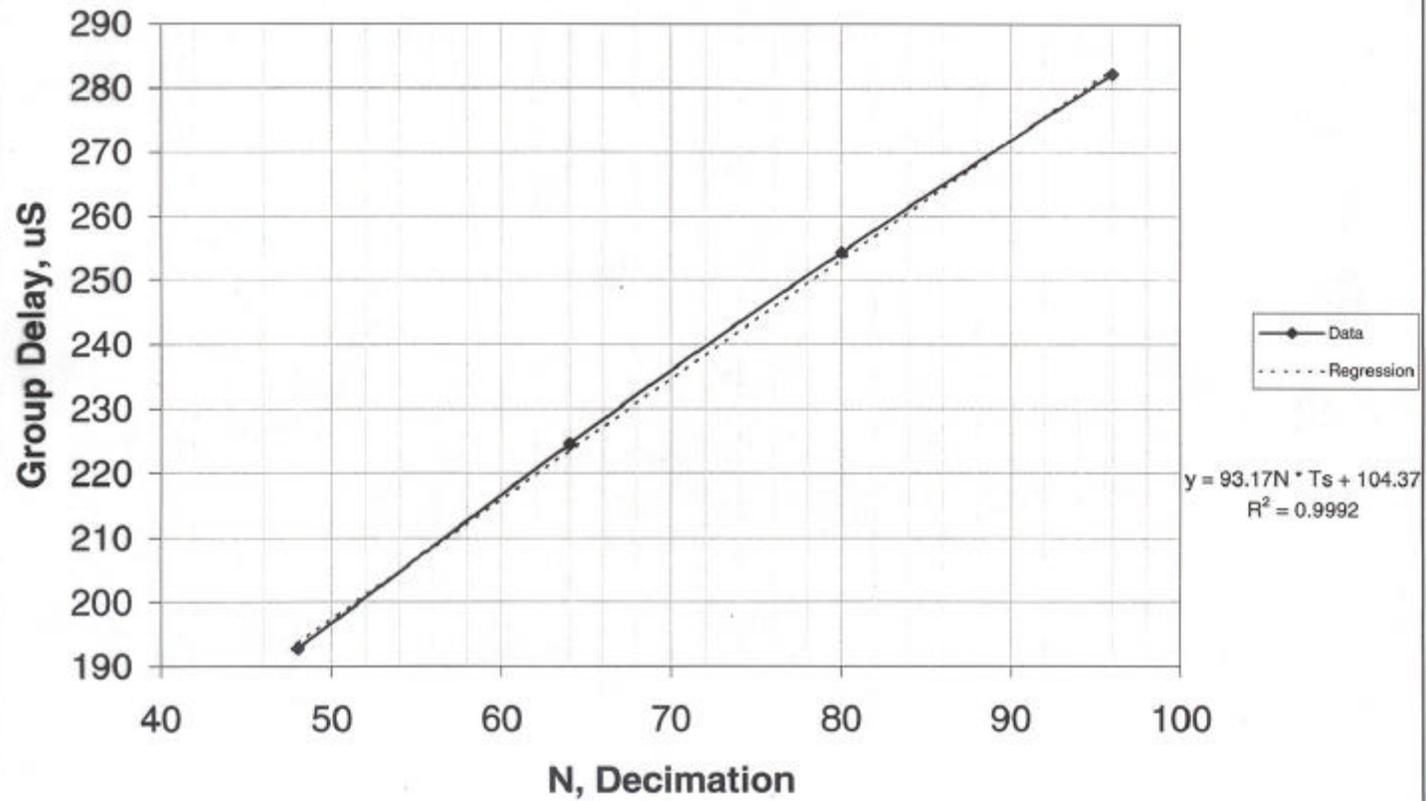
62 nS

1.8·N uS

CLC5956: $1.6 \text{ nS} + 3 \cdot T_s$
 CLC5902: $90 \cdot N \cdot T_s$

Group Delay vs Decimation

$T_s = 20 \text{ nS}$



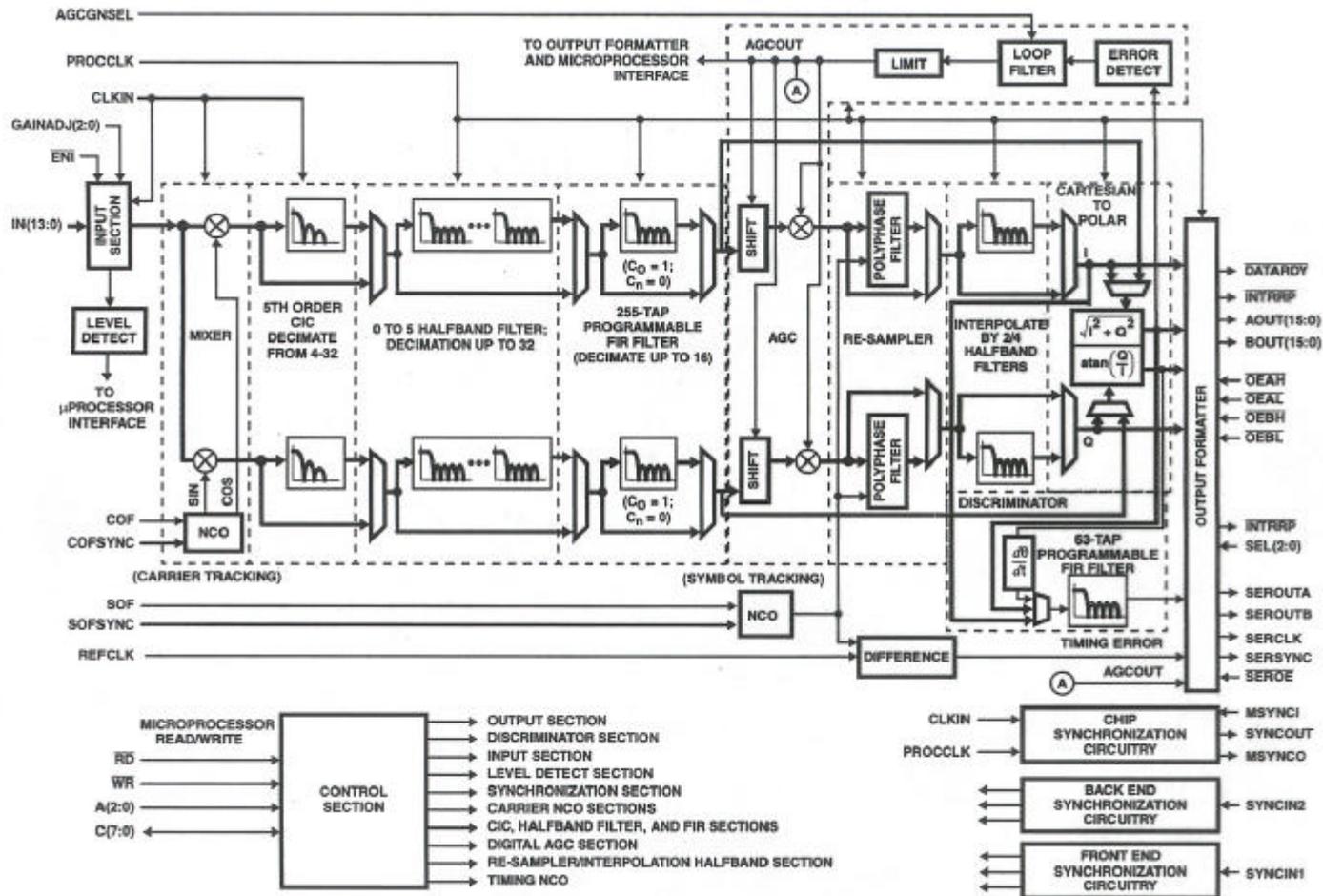
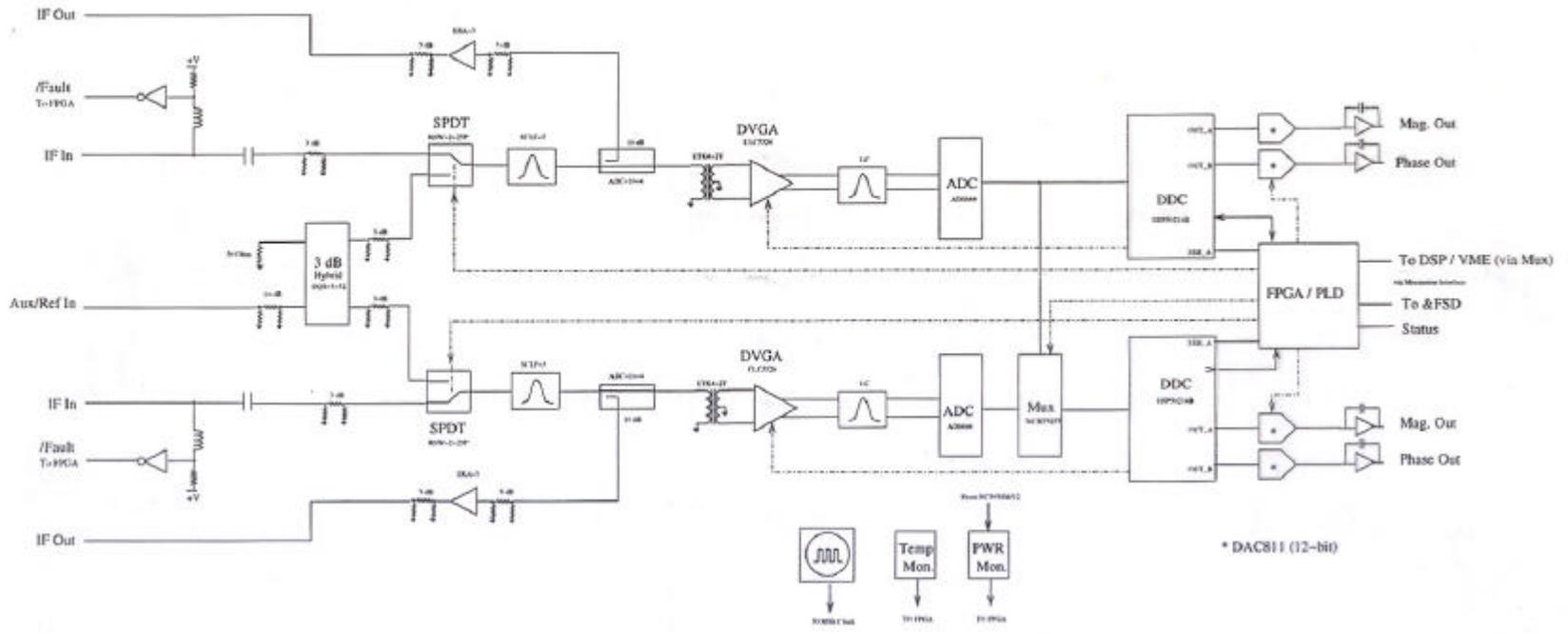


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE HSP50214B PROGRAMMABLE DOWNCONVERTER

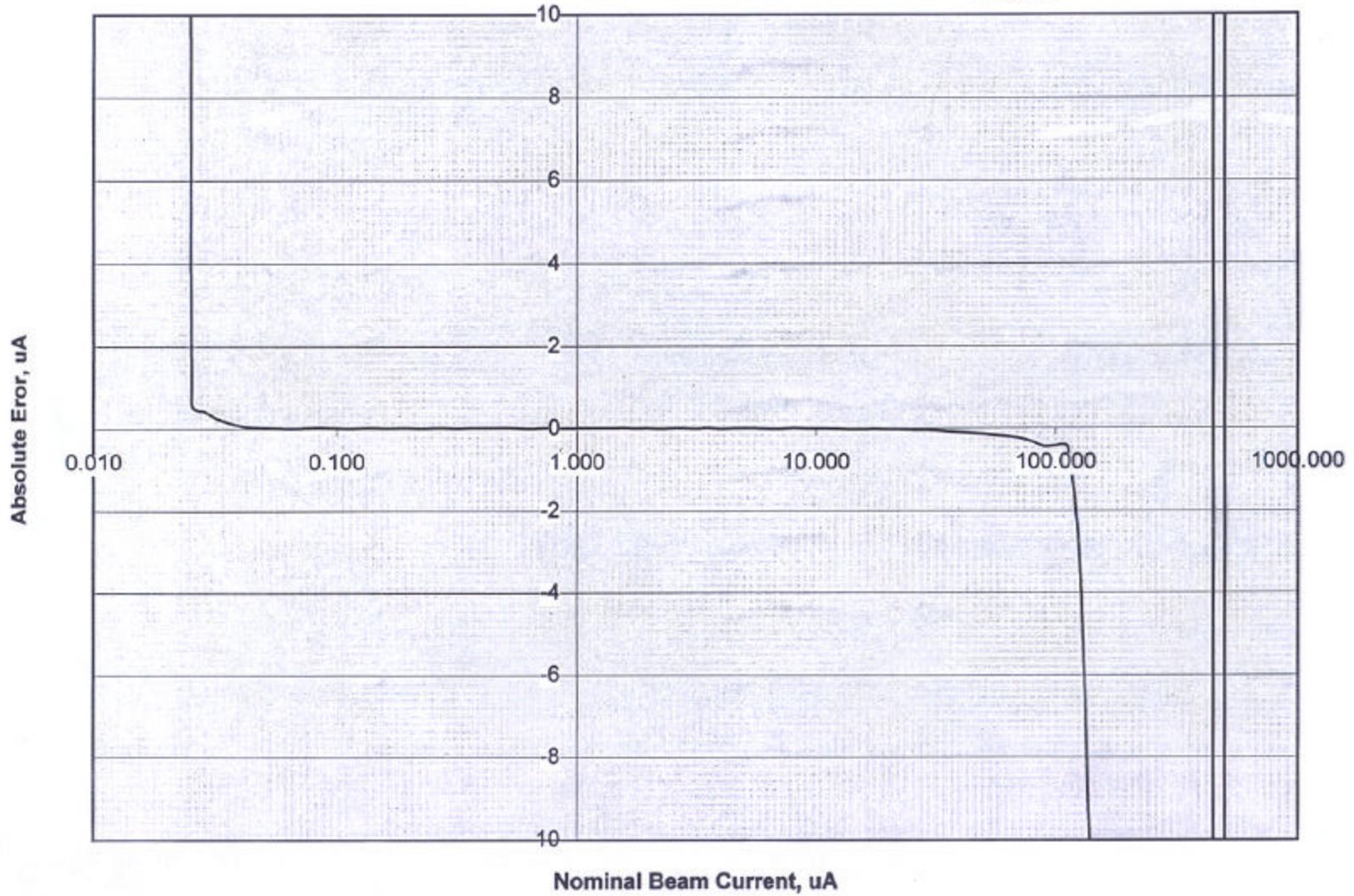
BCM Receiver



Absolute Error vs Nominal Ibeam

Gain = 30 dB

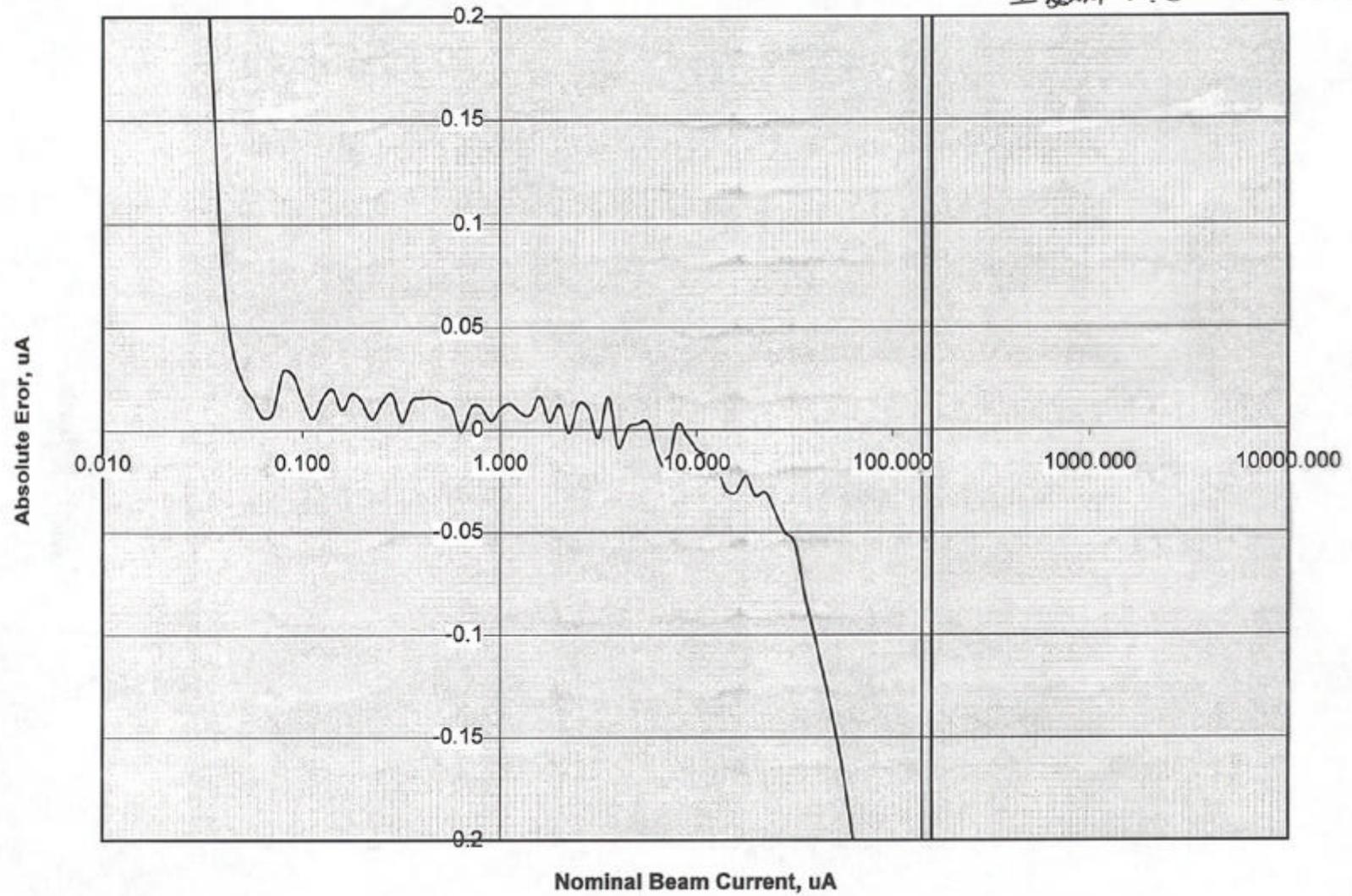
$I_{Beam} F.S. = 2000 \mu A$



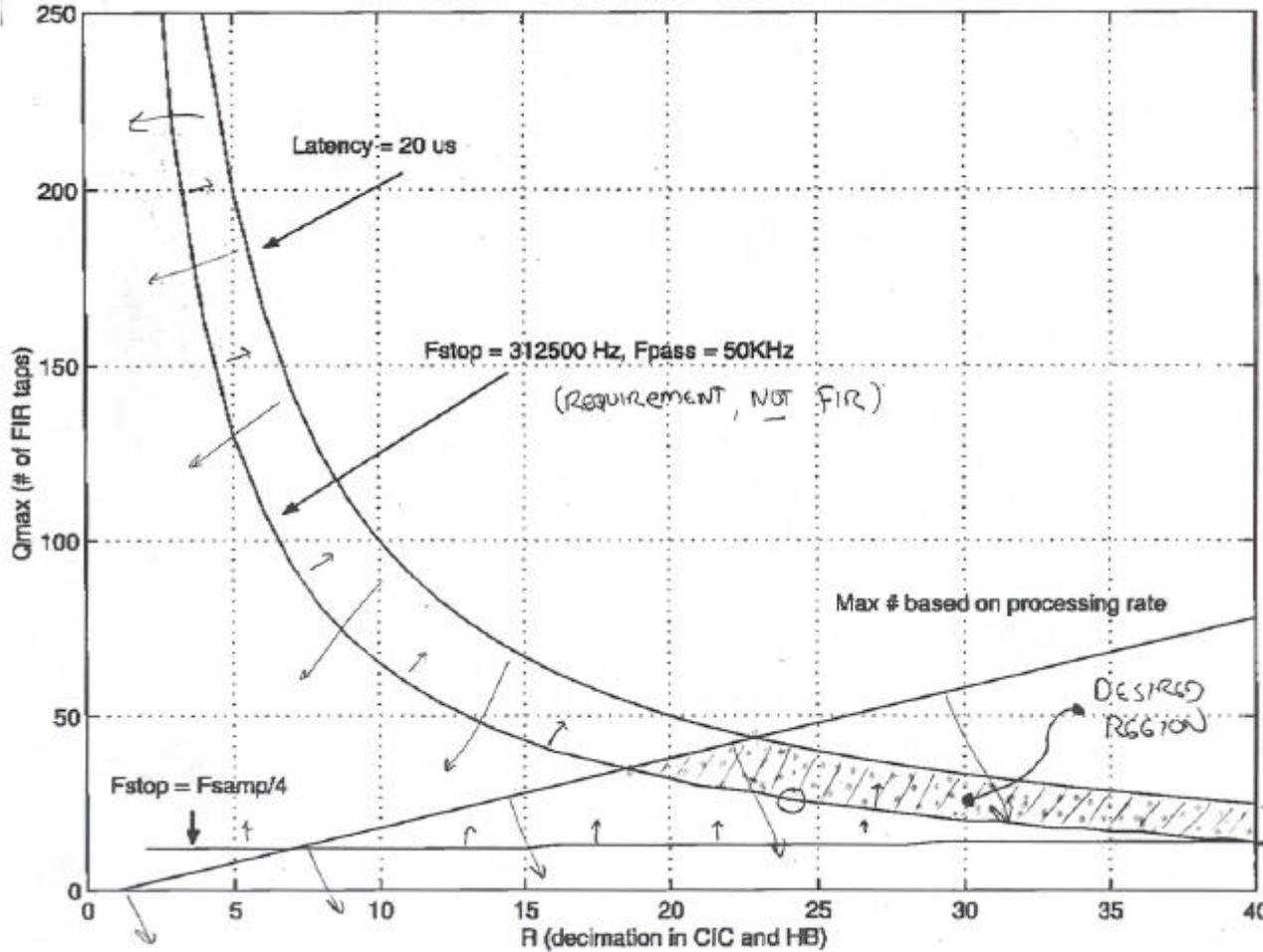
Absolute Error vs Nominal Ibeam

Gain = 30 dB

I_{beam} F.S. = 2000 mA



FIR filter order comparison, 28 Feb 2001, James Herford



R, Q E J

Ripple = 0.01 dB
 $\epsilon_{stop} \sim 60$ dB

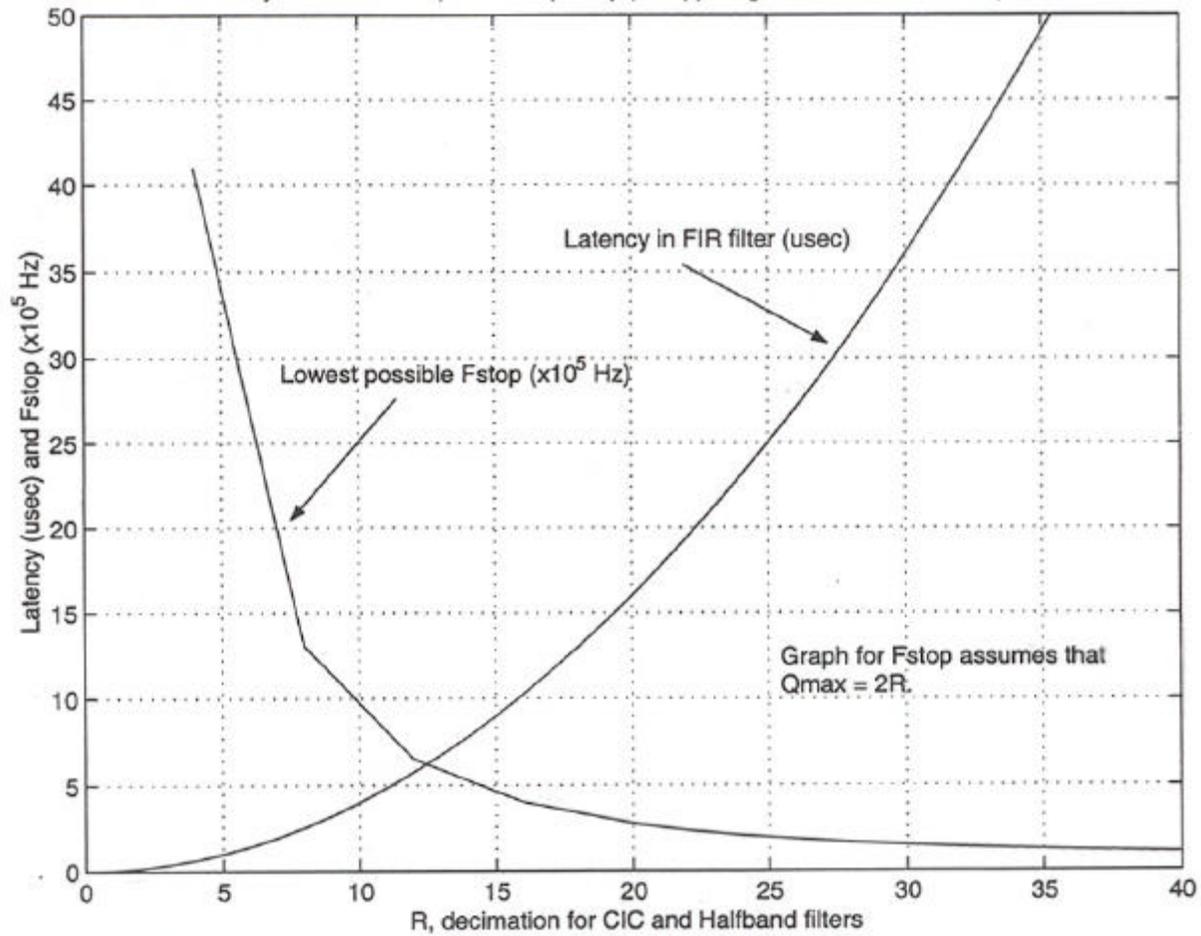
Start $\sim R=24$

$M_{cic} = 12$

1/2-BAND

Taps = 25

Latency and lowest stopband frequency (Fstop) for given decimation, 17 Apr 2001



Digital Receiver Features

- DSP board stand-alone
- Floating-point math
 - > 600 MFLOPS
- Generic mezzanine interface to facilitate various receivers, ADCs, audio, video, etc.
 - Several standards researched...TI selected
 - Supports fastest data rates
 - Specifically tailored for DSPs, 'C540 and DSK
 - Small footprint

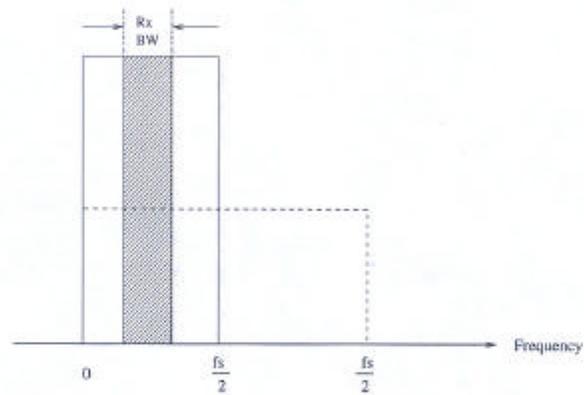
Features (cont.)

- Multiple I/O
 - TTL, fiber, analog
- Self-calibration
- Uniform production
 - No adjustments
- Multiple tools
 - Code Composer Studio (C++ development)
 - System View (RF, analog, mixed)
 - MatLab / Simulink

A word regarding A/D converters.....

Quantization noise dependent on:

1. # of bits
2. V full-scale
3. Sampling rate, f_s



1 & 2 set RMS voltage fluctuation level
3 determines how quickly "bit bounce" occurs, ie. over what bandwidth

An equivalent noise figure (1 Hz BW) can be developed for an A/D:

	<u>AD6640</u>	<u>AD6644</u>
# Bits:	12	14
ΔV	5.4E-4	1.3E-4
Rin	50 Ohms	50 Ohms
f_s	50 MHz	50 MHz
NF	37 dB	25 dB

DSP

- Facilitates algorithm development
 - Interfaces interactively with development tools
- Performs filtering
- Adaptive integrate-and-dump
- Self-calibration of receiver
 - Applies amplitude correction based on N.F. measurement
- Calculates cavity resonance
- Receives pilot tone for integrity monitoring

Processing + Timing

- Burn-through time is current-dependent
 - Utilize additional time for processing gain
- Optimize group delay
 - FIR vs decimation vs data processing
- Adaptive filtering
 - Short term = integrate-and-dump
 - Long term = LMS adaptive FIR, etc.

Tutorial

A typical application for adaptive systems is the separation of stochastic and periodic (deterministic) contributions in a signal. An example is the separation of speech and whistle (e. g. a short wave radio receiver).

Fig. 1 shows the method of working in principal. In this case speech is the stochastic signal r_k and whistle is the method deterministic signal s_k . The sum of both

$$x_k = s_k + r_k$$

is delayed d times, filtered by a ***N-tap FIR filter***²

$$y_k = \sum_{i=0}^{N-1} b_i x_{k-d-i}$$

and compared with the undelayed x_k

$$e_k = x_k - y_k.$$

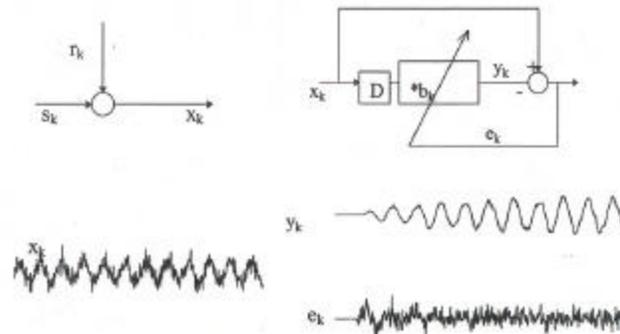


Fig. 1: Adaptive predictor. Noise r_k is added to a periodic signal s_k . The output y_k of the adaptive filter is an optimal estimate of s_k and the error signal e_k is an estimate of noise r_k .

¹ x_k denotes a digital sample of the signal $x(t)$ at time $t=k$ *samplingdistance

² FIR - finite impulse response (nonrecursive)

Dual Digital Signal Processing Board

Author: Hai Dong, ext 6543
Project: Beam Current Monitor (BCM)
First release:
Revised:

Features

- Dual TI 320C6711 floating point DSP
- Interface to VME bus using 64Kx16 dual port memory
- Support VME D16, D08(E0), BLT, RMW, ADO, AP, and IRQ cycles
- On board DSPs communicate via 64Kx16 dual port memory
- Serial link provides board to board DSP communication
- Support JTAG 1149 and TI CCS for ease of programming
- Support Altera FPGA programming chain
- Independent Watch Dog timer
- Programmable Temperature Sensor
- Board status indicator
- 8 digital inputs, 8 digital outputs, 2 DACs, 2 ADCs per channel
- 256Kx32 FLASH ROM (expandable to 1Meg)
- 4Mx32 SDRAM (expandable to 16Meg)
- Selectable DSP and IO clocks' frequency
- Support push button, VME, and power on reset
- Expansion is provided via dual 80 pins Mezzanine connectors
- Critical DSP data is available at VME P2 connector
- Support power on self test

Overview

The Dual Digital Signal Processing Board developed for BCM project is a general-purpose digital signal processing board that interfaces to VME bus. As shown in Figure 1, it contains two independent TI 320C6711 floating point DSPs. Each DSP has one 512x32 FLASH for program storage, 4Mx32 SDRAMs, 8 digital inputs, 8 digital outputs, one watch-dog timer, two DACs, and two ADCs.

Communication with the host is made via VME bus. Altera FPGA provides the interface between the DSPs and the VME bus. The FPGA is programmed to support VME 16 bits slave transfer (D16), even/odd byte transfer (D08(E0)), block transfer, read modified write cycle (RMW), address only cycle (ADO), address pipelining, and interrupt cycles. Commands from the host are passed to the DSPs through the dual port memories. The DSPs can either poll for new command or be interrupted. The interrupt level is selectable. In addition to handle the VME interface, the FPGA also monitors the temperature sensor, controls the status display, implements rotating buffers, and outputs critical DSP data to VME P2 connector.

The two DSPs communicate with each other through a 64Kx16 dual port RAM and with external DSPs (or other devices) via TI serial link using Round Robin protocol.