Making Fastbus Faster

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I. Sparsification
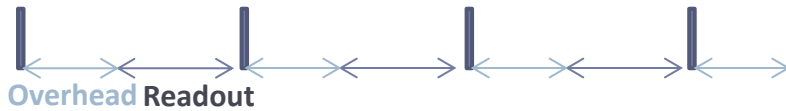Throws out background hits

window 0-32 µs

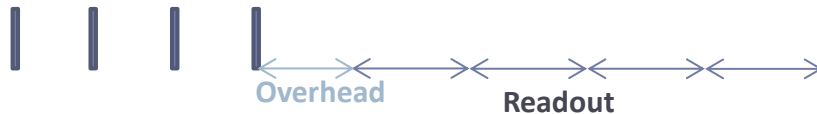**background**

signal

Gate

sparsify

Common Stop
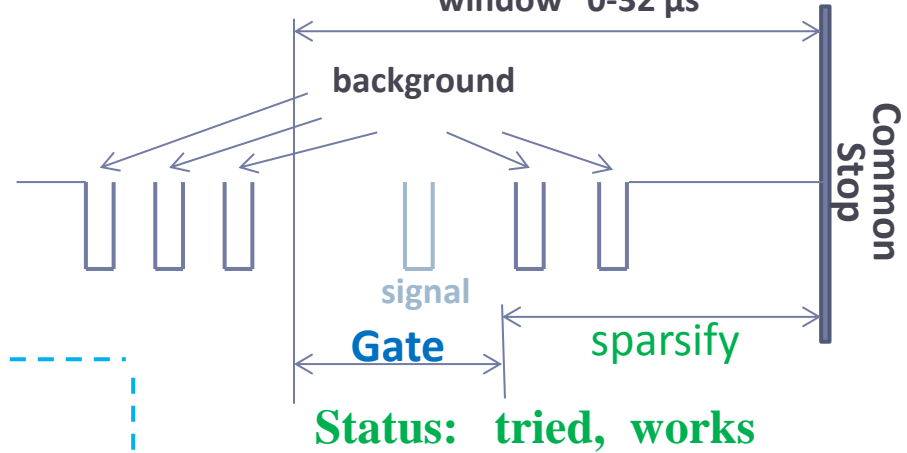
Status: tried, works

II. Event Blocking
Blocklevel=4 should work with pipelining VME

Triggers

Overhead **Readout**

Buffers the deadtime
and reduces overhead

Triggers

Overhead

Readout

Status: tried, works

III. Event Switching
3 parallel crates reduces rate by 3
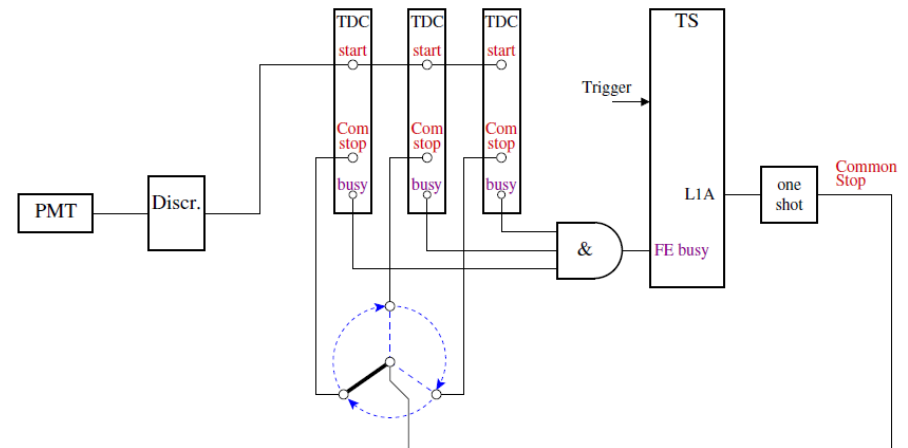
Status: test about to start

Deadtime fraction vs Trigger Rate (Hz)

Fastbus Performance on HRS Spectrometer

DATA Points

MODEL curve
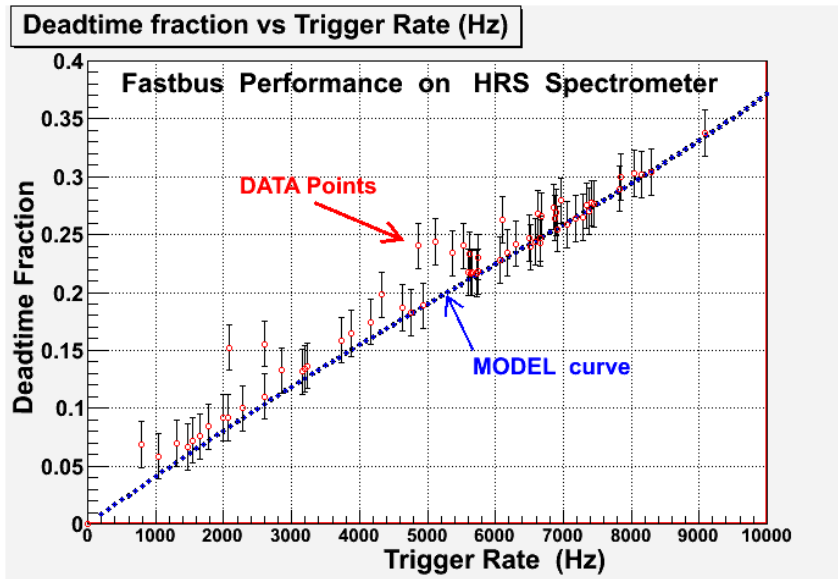
Based on **experience**

with Fastbus we can predict the performance of the

SBS Fastbus system

For a simple level-1 trigger

We can merge Fastbus with the rest of the DAQ if

- All components use blocklevel = 4

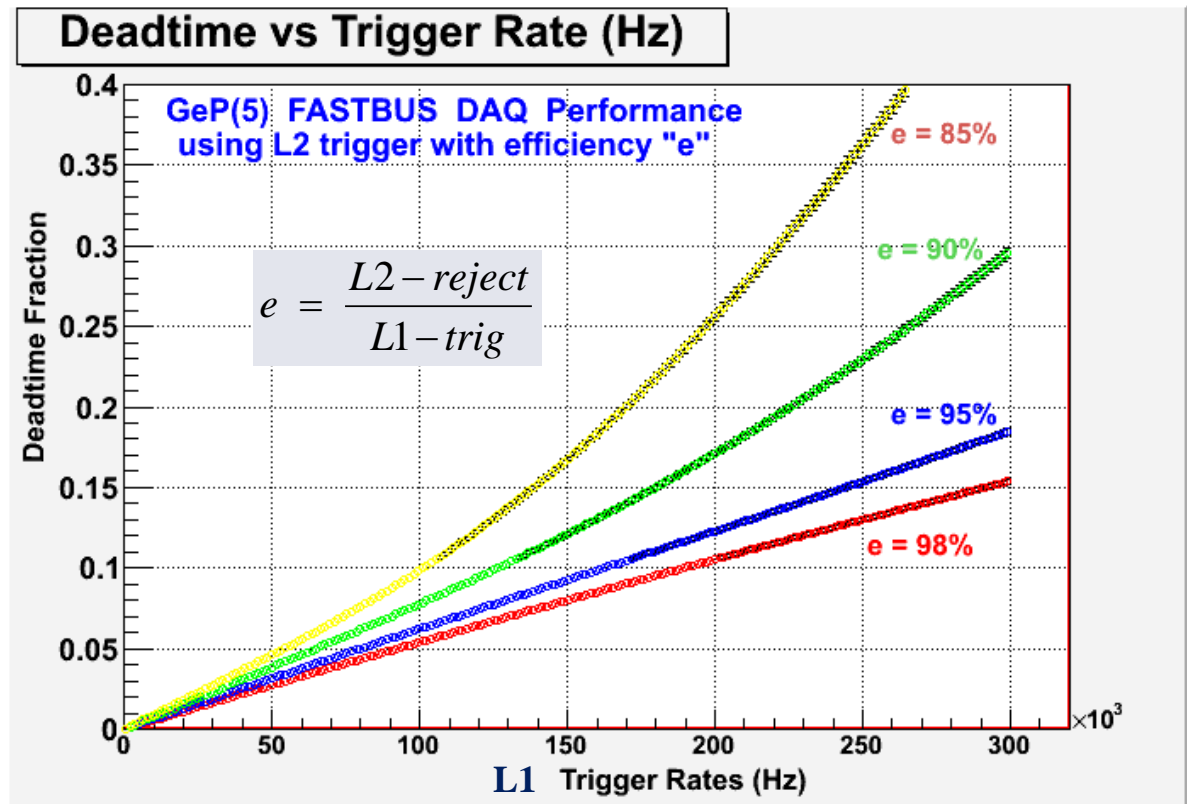- All crates conform to the CODA standard.

This needs to be tested

Deadtime Fraction vs Trigger Rate (Hz)

SBS Fastbus Performance Model

No Blocking

~10% deadtime at 20kHz

with Event Blocking
module switching, and sparesification

GeP(5) is the most demanding

For Fastbus, the plan is to use second-level (L2) triggers to
issue a fast clear.

Singles L1 trigger rate 100 – 300 kHz depending on thresholds.
L2 rejection 80% or greater.

Deadtime vs Trigger Rate (Hz)

GeP(5) FASTBUS DAQ Performance
using L2 trigger with efficiency "e"

$$e \; = \; \frac{L2 - reject}{L1 - trig}$$

e = 85%
e = 90%
e = 95%
e = 98%

Deadtime Fraction

L1 Trigger Rates (Hz)

Fastbus Status

- Have sufficient TDCs, ADCs, crates, aux. cards

  | | have 236 | have 113 | have 30 |
  | | need 124 | need 94 | need 21 |

- Like to scrounge ~3 more SFI (Struck Fastbus Interface)

  (have ~0 spare SFI; backup plan: reduced num crates, reduced performance)

- Making FB faster

  - sparsification – works
  - event blocking – works
  - event switching -- to be tried, looks feasible
  - merging with pipelining VME -- to be tried

- Two large fastbus systems are being assembled for test in the test lab.