Status of the Clas12 MVT electronics

Irakli MANDJAVIDZE

IRFU, CEA Saclay,
91191 Gif-sur-Yvette, France

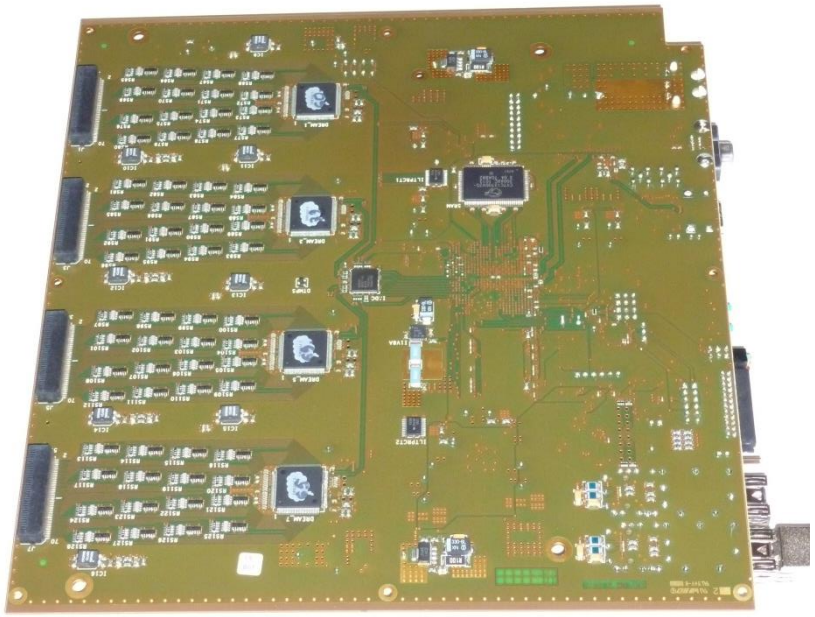
Dream V1 Production

- Submitted on March 10, 2013
- 6 wafers with 62 chips produced = 372 chips
  - → Packaged chips expected in June
  - → 3 more wafers (186 chips) to be produced after validation
    - No extra cost if no modification needed
- Production of 15 more wafers can be started already this summer
- Automatic Dream test bench almost ready for large scale Dream validation tests

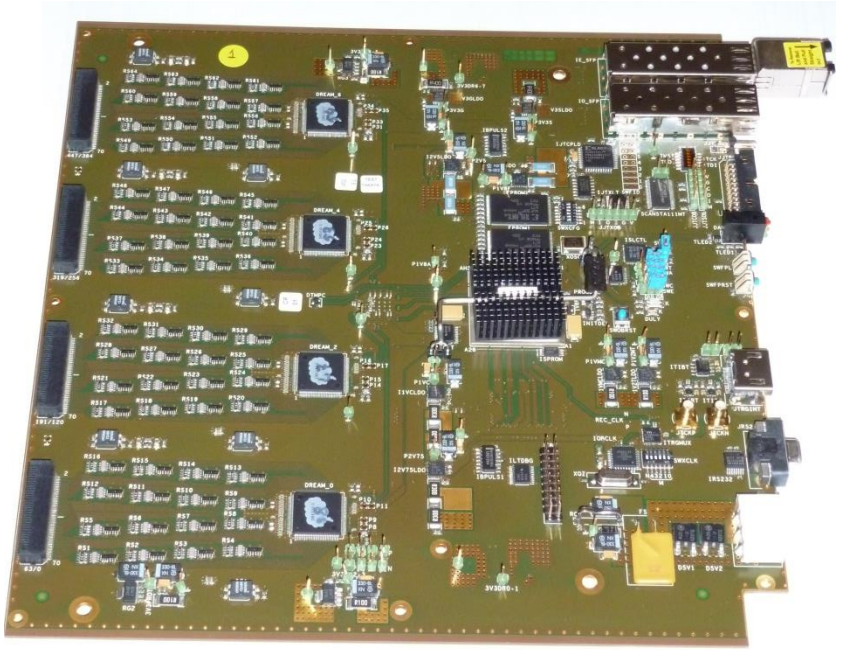
FEU prototypes

- Two prototype boards received
  - → 6U high (233 mm) x 220 mm deep board
  - → 1.6 mm thick 12-layer board: 6 power and 6 signal layers
  - → With Dream0 chips and Virtex-6 LX75T FPGA

ADC side



FPGA side



FEU prototypes

- Power consumption ~20W as expected
  → 4.8A @ 4.3V (with all 8 Dream-s on, optical and Ethernet transceivers)

- Tests in progress
  → The 3 JTAG chains accessible
  → FPGA and 2 FPROMs programmable
    - Multiple compressed firmware versions possible
  → Embedded micro-processor system @ 62.5MHz
    - External 512 KB synchronous RAM OK
    - 1G Ethernet OK
  → 2.5 Gbit/s optical link with backend OK
  → ADC and Dream slow control OK

  → Data acquisition tests ongoing
    - Baseline measurements w/ & w/o micro-coaxial cables

Backend hardware loan

- Backend hardware expected at Saclay next week
  - → VXS crate
  - → Trigger Interface (TI) and Signal Distribution (SD) modules
    - To be used as is
  - → Sub-System Processor (SSP) modules
    - Firmware adaptation / modification / development in progress
- Loan of a crate controller single board CPU under approval
  - → Hope to be ready by end of June
    - Can be picked-up by the Saclay team on trip at JLAB