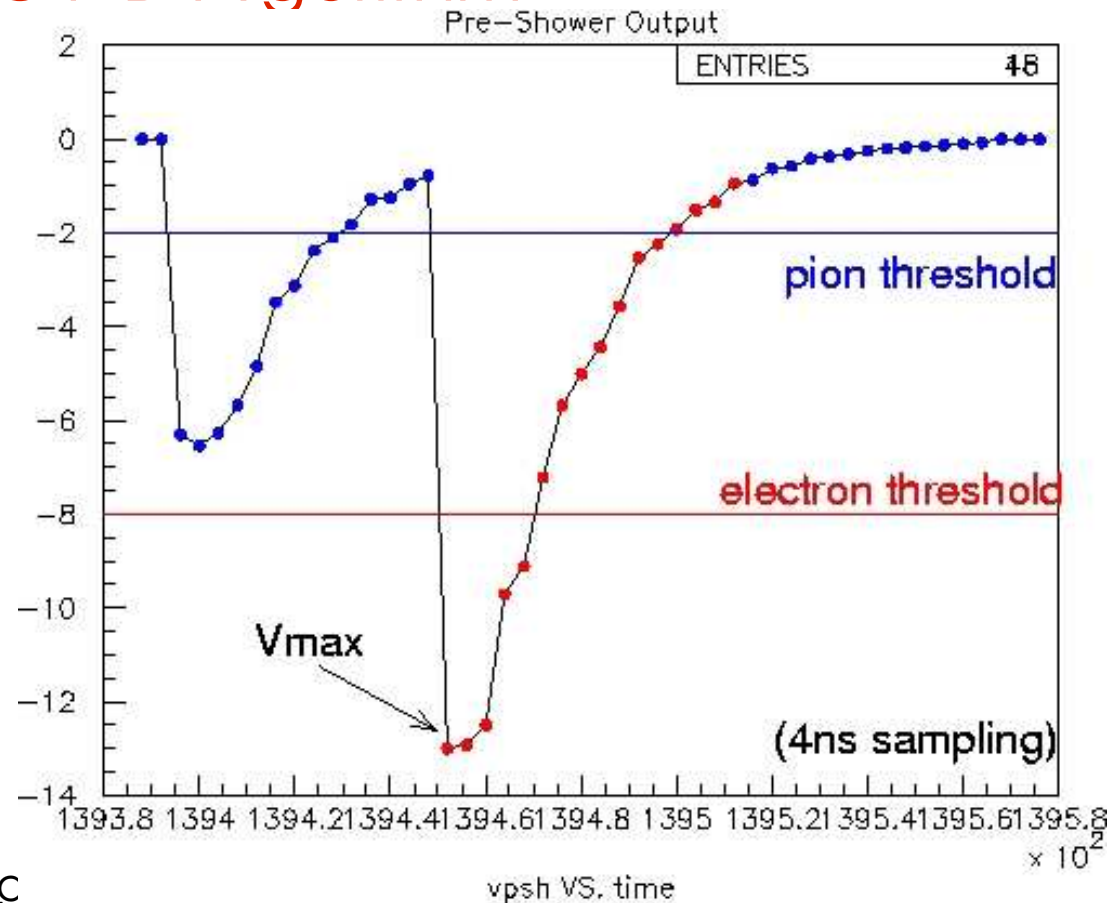


# Basic FADC PID Algorithm

- If ( $V_{in} > \text{threshold}$ ) then
  - ◆ Find edge of the peak;
  - ◆ Calculate sum and maximum;
  - ◆ Calculate width( $\Gamma$ )=sum/max;
- If ( $V_{max} > V_{min}^e$ ) & ( $|\Gamma - \Gamma_0| / \Gamma_0 < 50\%$ )
  - then  $n_e++$ ;
- If ( $V_{max} > V_{min}^\pi$ ) & ( $V_{max} > V_{min}^e$ )
  - & ( $|\Gamma - \Gamma_0| / \Gamma_0 < 50\%$ ) then  $n_\pi++$ ;
- If  $\Gamma / \Gamma_0 < 0.5$  then noise? => sampling
- If  $\Gamma / \Gamma_0 > 1.5$  then pileup? => sampling?
  - ◆ Separate peaks;
  - ◆ Identify pileup type (e-e, e- $\pi$ ,  $\pi$ -e,  $\pi$ - $\pi$ )



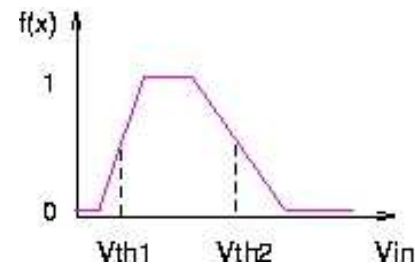
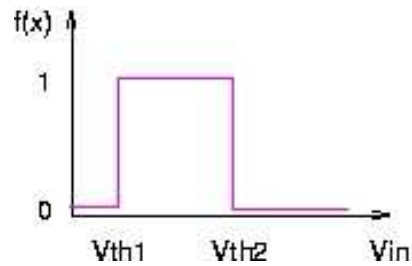
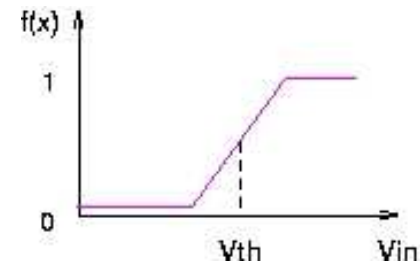
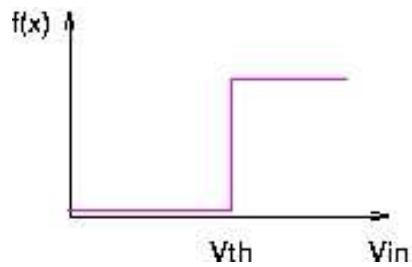
# Lot of room to make it more complicated

- Discriminating:

- CFD;

- “Membership” function:

- ★ for each detector signal:



Step functions

More complicated

- Combine 4 signals:  $g^e = f_1^e + f_2^e + f_3^e + f_4^e = (0, 1)$

- Judgement/Algorithm for noise/pileups
- Multi-channel triggering:
  - ◆ Each detector has 48-80 PMTs, cannot do analog sum of all one-time;
  - ◆ Grouping, triggering algorithm;
- Self-learning? (offline/online)
  - ◆ Use low-frequency full event sampling
  - ◆ Determine threshold, peak width
  - ◆ Determine membership function;

- What types of calculation can FPGA perform?
- How many FPGA? Coordinate problem?
- Speed of FPGA (break down to operations)?
- Anything else?