X-Ray Lithography towards 15 nm
2nd Meeting

The report of a meeting held November 5, 2003
At BAE Systems, Manassas, Virginia, USA in collaboration with
Jefferson Lab (Newport News, Virginia), which is Operated by
the United States Department of Energy under contract DE-
AC05-84-ER40150
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- *John Rodgers, BAE Systems* 21
- *Maureen Roche, BAE Systems* 25
- *Gwyn Williams, Jefferson Lab.* 30
Summary

This group met once before, on January 24, 2003 and a meeting report is available on line at: http://www.jlab.org/FEL/xrl_report_1.pdf. The group comprises a consortium of key technical executives representing a broad range of advanced lithography disciplines. At the previous meeting it was concluded that “it is essential that a modest x-ray lithography (XRL) program be developed as soon as possible to re-define a road-map for x-ray processes to assure the maintenance of US competitiveness”. The group further concluded that “there are no show-stoppers”.

Given this background, this second meeting decided to focus on a specific product or products, to try to define a project that might re-ignite XRL within the semiconductor industry. In order to accomplish this, representatives from all the necessary technologies, sources, steppers, masks, and manufacturing, were present.

The meeting began with an introduction to NGL by Martin Richardson, (University of Central Florida), at which the key issues were related to the semiconductor technology road map. Current goals are 40 wafer levels per hour with 300mm wafers, and with EUV insertion in 2008-2009 at the 35 nm level. Within the context of EUVL, details of source intensity and collimating mirror survival problems were presented. This was followed by a presentation by Bob Selzer (JMAR) on the situation pertaining to x-ray masks. Current capability exists to produce 25 masks per year on 2 micron SiC membranes with 500 nm TaSi absorbers. The masks have a surface flatness of < 5 microns. John Rodgers (BAE Systems, Manassas) then presented a proposal to develop C-RAM chips using x-ray lithography to reduce the current dimensions so that, for example, a 64 Mbit or greater C-RAM might be produced. C-RAMs use chalcogenide phase-change technology for non-volatile radiation hardened memory switchable with 3.3 volts and accessible within a few 10’s of nanoseconds. Maureen Roche (BAE Systems, Nashua) then presented details of programs involving XRL to MMIC chips and phase arrays. Finally Gwyn Williams (Jefferson Lab) presented details of current synchrotron sources at Wisconsin, Brookhaven and Jefferson Lab, including delivered power, brightness and costs of operation.

A discussion followed, which initially considered whether the scope of any BAE Systems projects was large enough, by itself, to drive an initiative to set up a synchrotron-based XRL facility as an enabling cost-effective technological solution. Clearly none of the existing projects is sufficient to drive such a large ($30m over 2 years) venture.

The discussion then focused on methods of convincing the industry of the value and advantages of XRL. The group learned from Fred Dylla (Jefferson Lab) that Sematech had expressed interest in XRL to him at the AVS 50th Symposium this week, and specifically had asked for a report of this meeting at their meeting in January 2004.

Marty Peckerar then made a bold proposal, namely that of initiating a project to make C-RAMS at 30 – 50 nm design rules, thereby demonstrating the capability of XRL in a product that the industry might find particularly attractive, and one that could not be manufactured today in quantity by any other method. Such a product would yield at least a 64 Mbit radiation hardened, non-volatile memory chip requiring only 3.3 volts, and with access times in the 10’s of nanoseconds, and lifetimes in the 10^9 cycle range.

This proposal was enthusiastically supported and seemed achievable with low risk. Bob Selzer stated that if a request for a mask were made before November 19, 2003, then a
mask could be manufactured by mid-December. It seemed clear that since the mask would be based on scaling from an existing prototype, this request was achievable. Therefore it would be reasonable to think of making exposures starting in mid-December. It was decided that Mitch Burte would refine this outline plan and present details to a DARPA review in 2 weeks.

The plan would involve scaling existing masks to smaller design rules, therefore the initial products would be small-scale versions of existing ones. The plan would be to have the first product ready in January 2004.
Appendix A – Agenda

X-Ray Lithography, towards 15nm
2nd Meeting November 5, 2003
Bldg. 110, BAES Manassas, Virginia

8:00 Continential Breakfast

9:20 Welcome Steve Schnur, BAE Systems
9:30 Introduction to NGL Martin Richardson, University of Central Florida

10:15 XRL masks Bob Selzer, JMAR
10:45 C-RAMs John Rodgers, BAE Systems
11:15 GaAs MMIC applications of XRL Maureen Roche, BAE Systems
11:45 Synchrotron Sources Gwyn Williams, Jefferson Lab

12:15 Lunch

1:00 Discussions

Brainstorming topics
· What does a synchrotron-based x-ray lithography program need to be successful?
  – 1a. Resolution
  – 1b. Overlay
  – 1c. Throughput
  – 1d. Realistic Insertion Date
  – 1e. Reliability
  – 1f. Cost Benefit
· What needs to be done to meet the above specifications?
· What can each party do to contribute to bringing HELIOS back on-line?
· What other equipment is needed in addition to the ring and a stepper?
  Photoresist Processing Capability
  Environmental Stability

· What would each party use the ring and a stepper for if it were back on line?
  · Would BAE Systems lead one or more programs from Manassas and/or Nashua?

· Are there other parties who would want to use and should be allowed to use the ring?
  · Corporations?
  · Universities?
  · Government Labs?

· How will we fund the project to build a building and install the ring and stepper?
· How will we fund lithography demonstrations and device demonstrations using x-ray lithography?

3:00 Adjourn
## Appendix B – Participants

<table>
<thead>
<tr>
<th>Name</th>
<th>Company</th>
<th>Email</th>
</tr>
</thead>
<tbody>
<tr>
<td>Andy Pomerene</td>
<td>BAE Systems</td>
<td><a href="mailto:andrew.pomerene@baesystems.com">andrew.pomerene@baesystems.com</a></td>
</tr>
<tr>
<td>Tom McIntyre</td>
<td>BAE Systems</td>
<td><a href="mailto:thomas.mcintyre@baesystems.com">thomas.mcintyre@baesystems.com</a></td>
</tr>
<tr>
<td>Peter Spreen</td>
<td>Leica Microsystems</td>
<td><a href="mailto:peter.spreen@leica-microsystems.com">peter.spreen@leica-microsystems.com</a></td>
</tr>
<tr>
<td>Steve Schnur</td>
<td>BAE Systems</td>
<td><a href="mailto:steven.schnur@baesystems.com">steven.schnur@baesystems.com</a></td>
</tr>
<tr>
<td>Heinz Siegert</td>
<td>JMAR Systems</td>
<td><a href="mailto:Hsiegert@nanolitho.com">Hsiegert@nanolitho.com</a></td>
</tr>
<tr>
<td>Bob Selzer</td>
<td>JMAR Systems</td>
<td><a href="mailto:BobSelzer@nanolitho.com">BobSelzer@nanolitho.com</a></td>
</tr>
<tr>
<td>Maureen Roche</td>
<td>BAE Systems</td>
<td><a href="mailto:maureen.roche@baesystems.com">maureen.roche@baesystems.com</a></td>
</tr>
<tr>
<td>Antony Bourdillon</td>
<td>UhrlMasc</td>
<td><a href="mailto:bourdillon@prodigy.net">bourdillon@prodigy.net</a></td>
</tr>
<tr>
<td>Martin Richardson</td>
<td>UCF/CREOL</td>
<td><a href="mailto:mcr@creol.ucf.edu">mcr@creol.ucf.edu</a></td>
</tr>
<tr>
<td>Gwyn Williams</td>
<td>Jefferson Lab</td>
<td><a href="mailto:gwyn@mailaps.org">gwyn@mailaps.org</a></td>
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<tr>
<td>Ari Tuchman</td>
<td>Technoventures/UMD</td>
<td><a href="mailto:ari@technoventures.com">ari@technoventures.com</a></td>
</tr>
<tr>
<td>Marty Peckerar</td>
<td>U of MD</td>
<td><a href="mailto:peckerar@eng.umd.edu">peckerar@eng.umd.edu</a></td>
</tr>
<tr>
<td>Yuli Vladimirsky</td>
<td></td>
<td><a href="mailto:vvladimirsky@juno.com">vvladimirsky@juno.com</a></td>
</tr>
<tr>
<td>Marty Polavaradu</td>
<td>BAE Systems</td>
<td><a href="mailto:marty.polavaradu@baesystems.com">marty.polavaradu@baesystems.com</a></td>
</tr>
<tr>
<td>John Rodgers</td>
<td>BAE Systems</td>
<td><a href="mailto:john.Rodgers@baesystems.com">john.Rodgers@baesystems.com</a></td>
</tr>
<tr>
<td>Mitch Burte</td>
<td>BAE Systems</td>
<td><a href="mailto:Mitchell.j.burte@baesystems.com">Mitchell.j.burte@baesystems.com</a></td>
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<tr>
<td>Nadim Haddad</td>
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<td><a href="mailto:nadim.haddad@baesystems.com">nadim.haddad@baesystems.com</a></td>
</tr>
<tr>
<td>Glenn Marshall</td>
<td>NAVAIR</td>
<td><a href="mailto:glenn.marshall@navy.mil">glenn.marshall@navy.mil</a></td>
</tr>
<tr>
<td>Fred Dylla</td>
<td>Jefferson Lab</td>
<td><a href="mailto:dylla@jlab.org">dylla@jlab.org</a></td>
</tr>
<tr>
<td>Dave Patterson</td>
<td>DARPA/MTO</td>
<td><a href="mailto:dpatterson@darpa.mil">dpatterson@darpa.mil</a></td>
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Perspective on X-ray Lithography

Martin Richardson
Laser Plasma Laboratory
School of Optics/CREOL, University of Central Florida,
Orlando,
Tel 407 823 6819  Fax 407 823 3570  email: mcr@creol.ucf.edu

Manassas, November 5, 2003

Trends

The SubWavelength™ Gap

G-Line: Contact Exposure 7µ
G-Line: 1:1 Projection 3-5 µ
G-Line: 5:1 Projection 2.0-.75 µ
I-Line: 5:1 Projection 750 – 350 nm
DUV: 4:1 Projection 250-130 nm  193 Projection 130 – 90 nm

~20 yrs  ~10 yrs  ~5 yrs

Courtesy of Numerical Technologies
A roadmap re-written – many times

**Early 90’s**  
*Four NGL’s*  
XRL, EBL, IBl and ‘soft X-ray Lithography* 
*Insertion at the 180 nm node*  
*130 nm*  
*10W (2π at the source) required*  
*XRL...and EUVL*  
*XRL with SRS the most robust*  

**End of 90’s**  
*DUV extended, 157 nm on the scene*  
*ISMT ‘prioritizes’ EUVL, then EBL....IBL and XRL*  
*40 w/lh, 300 mm dia. wafers*
A roadmap re-written – many times

Early 90’s        Four NGL’s       XRL, EBL, IBl and ‘soft X-ray Lithography
130 nm
insertion at the 180 nm node
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XRL with SRS the most robust

End of 90’s        DUV extended, 157 nm on the scene
ISMT ‘prioritizes’ EUVL, then EBL....IBL and XRL
40 w/lh, 300 mm dia. wafers

Now        EUVL is the ‘NGL’....157 ....but immersion, imprint and PM?

EUVL insertion at 35 nm…” need for investment stage”

CRITICAL ISSUES
1. Source power    100 W at IF
    - this means 400 W (2π) at source LP , 700 W for DP
2. Mirror erosion...from ions of source
3. Mask repair
Optical Lithography IS now coming to an end

One-size-fits all…is this true?

Moore’s Law aside …the future may not look like the past

NGL’s in Si only required for some critical elements….

New Materials….GaAs, InP….
…different markets, different requirements…

Is there room for a more flexible strategy?

XRL - a resurgence of interest?

What are the prospects for XRL?
- with or without a Si option
- new materials, new devices, processes…

Are there near-term needs for XRL?
- GaAs ?
- MMICs and interconnects…. 

Role of academic research…..

An open XRL SRS facility at Jefferson?
- what needs would it serve?
- would it spur increased interest in XRL?
- performance, facilities, costs, etc…
Infrastructure - Status of U.S. mask-making capabilities

Bob Selzer – JMAR Systems
November 5, 2003
9:00AM-3:00PM

CPL/XRL Mask Status

- Program Overview
- Mask Manufacturing Equipment
- Mask Requirements
- Mask Deliveries
- Opportunities
- Summary
**CPL/XRL Mask Status**

**Program Overview**

-DARPA/NAVAIR has funded in 2002-2003, the continuation of X-ray mask technology. Future years will be supported through congressional plus ups or directly by customers. 2004 now funded.

-Through Dec 2003 a cooperative effort with IBM Mask Operations in Essex Junction, VT. has provided ~25 masks per year. - Each of the first two years IBM has been contracted to build per JMAR defined criteria.

- Year 1: 130nm requirements
  - MMIC like devices, test patterns for litho POC
- Year 2: 100nm requirements
  - MMIC like devices, test patterns for litho demo

-Most masks were laid out by JMAR mask designers and submitted to IBM for writing.

---

**Mask Manufacturing Equipment**

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<tr>
<th>Tool</th>
<th>Function</th>
<th>Location</th>
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<tr>
<td>Sputter Films Endeavor PVD</td>
<td>Absorber deposition</td>
<td>IBM Essex Jct. VT</td>
</tr>
<tr>
<td>Eaton Summit RTA</td>
<td>Absorber anneal</td>
<td></td>
</tr>
<tr>
<td>PlasmaTherm SLR 730 PECVD</td>
<td>Hard mask deposition</td>
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</tr>
<tr>
<td>SUSS ACS 200 Resist Coater</td>
<td>Resist Coat</td>
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<tr>
<td>IBM EL-4+ E-beam Writer</td>
<td>Pattern Writing</td>
<td></td>
</tr>
<tr>
<td>APT</td>
<td>Develop</td>
<td></td>
</tr>
<tr>
<td>PlasmaTherm SLR 700</td>
<td>Descum; Hard mask etch</td>
<td></td>
</tr>
<tr>
<td>PlasmaTherm ECR</td>
<td>Absorber Etch</td>
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<tr>
<td>AMRAY 2040 CD-SEM</td>
<td>Image Size</td>
<td></td>
</tr>
<tr>
<td>Leica LMS 2020</td>
<td>Image Placement</td>
<td></td>
</tr>
<tr>
<td>KLA SESSpec</td>
<td>Defect Inspection</td>
<td></td>
</tr>
<tr>
<td>Micron 8000 FIBS</td>
<td>Mask Repair</td>
<td></td>
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</table>
Mask Requirements

- NIST Ring format – bonded wafer to ring
- Membrane SiC
  - Nominal thickness 2um
  - +/- 2.5% thickness variance
  - Optical transmission @ 500-600nm - 50%
- Absorber material thickness
  - 450 - 500nm TaSi or equivalent
  - +/- 2.5% thickness variance
- Flatness
  - Membrane
    - < 3um TIR
  - Mask surface
    - < 5um TIR

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<th>Specification</th>
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<th>tolerance / range</th>
<th>comments</th>
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<td>Membrane size</td>
<td>35 x 35mm</td>
<td>25- 50mm^2</td>
<td>range is for usable membrane sizes</td>
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<tr>
<td>Membrane centrality</td>
<td>center</td>
<td>+/- 0.25nm</td>
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<tr>
<td>Outlying Windows</td>
<td>na</td>
<td>na</td>
<td></td>
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<tr>
<td>Image size - isolated</td>
<td>100nm</td>
<td>10nm 3sigma</td>
<td>line and contact hole</td>
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<tr>
<td>Nested to Isolated delta</td>
<td>10nm</td>
<td>10nm 3sigma</td>
<td></td>
</tr>
<tr>
<td>Edge roughness</td>
<td>&lt; 10%</td>
<td>na</td>
<td></td>
</tr>
<tr>
<td>Corner rounding</td>
<td>&gt; 60%</td>
<td>na</td>
<td>% of 100nm feature to be square</td>
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<tr>
<td>Nested to Isolated delta</td>
<td>10nm</td>
<td>10nm 3sigma</td>
<td></td>
</tr>
<tr>
<td>Line end shortening</td>
<td>10nm</td>
<td>10nm 3sigma</td>
<td>provide measurements to minimum</td>
</tr>
<tr>
<td>Linearity</td>
<td>100-200nm</td>
<td>10nm 3sigma</td>
<td>resolved feature</td>
</tr>
<tr>
<td>Image Placement</td>
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<td>50nm</td>
<td>Mean ± 3-sigma</td>
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<td>This design does not require, What are capabilities?</td>
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<td>Image Magnification correction</td>
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<td>Mask contrast</td>
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<td>Dark Field</td>
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<tr>
<td>Defect specification</td>
<td>25% of feature size down to 90nm features</td>
<td>Feature spec, no breaks in gates</td>
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<td>Surface defect specification</td>
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<tr>
<td>Data mirror</td>
<td>na</td>
<td>na</td>
<td>Data is E-beam ready</td>
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<tr>
<td>V-notch orientation</td>
<td>na</td>
<td>na</td>
<td>Data is E-beam ready</td>
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<tr>
<td>Average transmission, cleared areas</td>
<td>&gt; 50%</td>
<td>na</td>
<td>average value 400-580nm light</td>
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</table>
Mask Requirements

- Nominal feature 130-100nm, statistical sample.
  - Image size
  - Line end shortening
  - Corner rounding
  - Edge roughness
- Linearity, Statistical sample nested & isolated.
  - Minimum resolution to 200nm
- Placement, Systematic errors
  - Across membrane sample
  - Across data sample
  - Tool specific contribution sample
  - Sub field metrology for shape beam writers
- SEM images of nominal & best can do resolution
  - Edge roughness
- SEM images of defects.
- Transmission
- Centrality

130nm Contacts – Year 1
130nm mixed site
100nm Contacts – Year 2
X-Ray Mask Request Form

Order Date: 9/4/2003
Quantity: 2
Requested Delivery Date: 8/2003

Mask Name: CNTech2003B
Instance: #1&2
Level(s): Prime

Customer Name: JMAR
E-mail: bgrenon@together.net
Telephone: 802-862-4551

For complete design and build requirements, refer to Mask design guide and associated drawings.

**Mask Product Specifics**

- Image Size Specification for mask quality definition.
  (Nominal 100nm, mean from nominal _25nm-3s)
- Nested to Isolated maximum delta (Optimize 100nm contact quality)
- Image size X-Y (_15nm-3s)
- Customer specified bias (None)
- Image Placement Specification (50nm-3s)
- Centrality, Chip to NIST ring (500 um)
- Membrane dimensions Chip area (X: 35mm, Y: 35mm)
- Membrane center placement, Chip area (X: 0mm, Y: 0mm)
- Membrane placement accuracy Chip area (+/-500um)
- Membrane dimensions Outlying areas (none)
- Membrane center placement, Outlying area (none)
- Membrane placement accuracy outlying area (none)
- Defect Specification (no gross defects or raised defects over 2um)
- Image Placement Magnification Corrections (none)
- Systematic Tolerance, SF: 2.0ppm; Ortho: 2.0ppm
- Mask Contrast (Dark field)
- Chip Size (X: 28mm Y: 28mm)
- Stepping Periodicity, Number of Die (na)
- V-notch orientation: down when mask name is readable backside
- Data mirror (data will be ready for E-beam, no flips required PRIME cell)
- Edge Roughness (None)
- Corner rounding – feature size / radius (best can do)
- Line end shortening, IS – Shortening, (na)
- Linearity, IS range – max variance (na)
- Transmission through alignment areas (>50%) Clear all targets.

**Input Data Format**

- GDS-II
- Prime Cell _PRIME_
- Reticle Layout map (attached .jpg)
- JMAR Supplied data
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<td>Sampler1</td>
<td>2/10/03</td>
<td>2/17/03</td>
<td>5/9/03-6/18/03</td>
<td>6/16/03</td>
<td></td>
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<tr>
<td>17</td>
<td>Sampler1</td>
<td>2/10/03</td>
<td>2/20/03</td>
<td>5/9/03</td>
<td>7/24/03</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>GridT30</td>
<td>5/22/02</td>
<td>4/18/03</td>
<td>7/3/03</td>
<td>8/12/03</td>
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<tr>
<td>19</td>
<td>GridT30</td>
<td>5/22/02</td>
<td>4/18/03</td>
<td>7/3/03</td>
<td>8/18/03</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Ironman</td>
<td>5/16/03</td>
<td>2/14/02</td>
<td>6/27/03</td>
<td>6/19/03</td>
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</table>

**Mask Orders - Year 2**

<table>
<thead>
<tr>
<th>Slot</th>
<th>Mask</th>
<th>Order Date</th>
<th>GDS Data Ready</th>
<th>Commit Date</th>
<th>Ship Date</th>
<th>Status</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>ZONEMASK</td>
<td>5/27/03</td>
<td>5/20/03</td>
<td>7/14/03</td>
<td>6/6/03</td>
<td>Mask 93A2 shipped</td>
</tr>
<tr>
<td>2</td>
<td>ZONEMASK</td>
<td>5/27/03</td>
<td>5/20/03</td>
<td>7/14/03</td>
<td>6/12/03</td>
<td>Mask 97B6 shipped</td>
</tr>
<tr>
<td>3</td>
<td>GRID100</td>
<td>8/22/03</td>
<td>8/22/03</td>
<td>10/03/03</td>
<td>10/10/03</td>
<td>Mask 9904 @ repair</td>
</tr>
<tr>
<td>4</td>
<td>GRID100</td>
<td>8/22/03</td>
<td>8/22/03</td>
<td>10/03/03</td>
<td>10/10/03</td>
<td>Mask 102C4 @ repair</td>
</tr>
<tr>
<td>5</td>
<td>IronMaiden</td>
<td>9/10/03</td>
<td>8/26/03</td>
<td>10/22/02</td>
<td>11/03/03</td>
<td>Mask 97B4</td>
</tr>
<tr>
<td>6</td>
<td>IronMaiden</td>
<td>9/10/03</td>
<td>8/26/03</td>
<td>10/22/03</td>
<td></td>
<td>Mask 97B6</td>
</tr>
<tr>
<td>7</td>
<td>CNT2003</td>
<td>9/04/03</td>
<td></td>
<td>Data under review</td>
<td></td>
<td>Data under review</td>
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<tr>
<td>8</td>
<td>CNT2003</td>
<td>9/04/03</td>
<td></td>
<td>Data under review</td>
<td></td>
<td>Data under review</td>
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<tr>
<td>9</td>
<td>DMS 277</td>
<td>10/27/03</td>
<td>10/6/03</td>
<td>12/8/03</td>
<td>11/03/03</td>
<td>In mask build</td>
</tr>
<tr>
<td>10</td>
<td>DMS 256</td>
<td>10/27/03</td>
<td>10/29/03</td>
<td>12/10/03</td>
<td>In mask build</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>DMS256</td>
<td>10/27/03</td>
<td>10/29/03</td>
<td>12/10/03</td>
<td>In mask build</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>IronMaiden V2</td>
<td>10/27/03</td>
<td>10/27/03</td>
<td></td>
<td>In mask build; ALX70 coordinates needed</td>
<td></td>
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</tbody>
</table>
## Mask Data - Year 1

<table>
<thead>
<tr>
<th>Slot</th>
<th>Mask</th>
<th>Lot</th>
<th>Image Size (nm)</th>
<th>Uniformity (15nm)</th>
<th>Image Placement (50nm)</th>
<th>Defects (None)</th>
<th>Trans.</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Throughput Mask</td>
<td>94C5</td>
<td>126</td>
<td>8</td>
<td>58nm,42nm</td>
<td>N/A++</td>
<td>50.0-51.1%</td>
<td>IBM test pattern; AM's; relaxed spec</td>
</tr>
<tr>
<td>2</td>
<td>Throughput Mask</td>
<td>95B5</td>
<td>134</td>
<td>8</td>
<td>49nm,45nm</td>
<td>N/A++</td>
<td>51.0-52.2%</td>
<td>IBM test pattern; AM's; relaxed Spec</td>
</tr>
<tr>
<td>3</td>
<td>Throughput Mask</td>
<td>98A6</td>
<td>138</td>
<td>8</td>
<td>68nm,45nm*</td>
<td>N/A++</td>
<td>52.0-52.4%</td>
<td>IBM test pattern; AM's; relaxed Spec</td>
</tr>
<tr>
<td>3A</td>
<td>Throughput Mask</td>
<td>98B4</td>
<td>132</td>
<td>7</td>
<td>54nm,50nm*</td>
<td>N/A++</td>
<td>53.7-54.0%</td>
<td>IBM test pattern; AM's; relaxed Spec</td>
</tr>
<tr>
<td>4</td>
<td>Ironman</td>
<td>97A1</td>
<td>126</td>
<td>12</td>
<td>38nm,39nm</td>
<td>N/A+</td>
<td>52.4-53.1%</td>
<td>JSAL Design</td>
</tr>
<tr>
<td>5</td>
<td>DMS 173 MMIC</td>
<td>98C2</td>
<td>138</td>
<td>6</td>
<td>31nm,27nm</td>
<td></td>
<td>50.1-50.8%</td>
<td>BAE Gate mask</td>
</tr>
<tr>
<td>6</td>
<td>ROBOMASC</td>
<td>98B3</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A++</td>
<td>51.9-52.5%</td>
<td>Resolution mask</td>
</tr>
<tr>
<td>7</td>
<td>ROBOMASC</td>
<td>97B1</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A++</td>
<td>53.0-53.0%</td>
<td>Resolution mask</td>
</tr>
<tr>
<td>8</td>
<td>Ironman</td>
<td>97B5</td>
<td>126</td>
<td>13</td>
<td>29nm,45nm</td>
<td>N/A++</td>
<td>TBD</td>
<td>JSAL Design</td>
</tr>
</tbody>
</table>

*PSE send ahead to assure 50nm image placement were waived by JSAL to assure faster TAT
++Mask returned to IBM  ++No KLA inspection required; gross defect spec only

## Notes

- Trans. Defects: (None)
- Uniformity (15nm)
- Image Size (130nm)
- CD Mean Target 220nm**CD Mean Target 450nm

**No brakes in gates; Nothing larger than 5um ++No KLA inspection required; gross defect spec only

---

## Mask Data - Year 1

<table>
<thead>
<tr>
<th>Slot</th>
<th>Mask</th>
<th>Lot</th>
<th>Image Size (130nm)</th>
<th>Uniformity (15nm)</th>
<th>Image Placement (50nm)</th>
<th>Defects (None)</th>
<th>Trans.</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>F22 M72</td>
<td>99A06</td>
<td>218nm*</td>
<td>14</td>
<td>50nm,44nm</td>
<td>None***</td>
<td>52.2-52.4%</td>
<td>BAE Gate Mask</td>
</tr>
<tr>
<td>11</td>
<td>F22 M75</td>
<td>99B03</td>
<td>221nm*</td>
<td>12</td>
<td>45nm,45nm</td>
<td>None***</td>
<td>52.7-53.6%</td>
<td>BAE Gate Mask</td>
</tr>
<tr>
<td>12</td>
<td>F22 M71</td>
<td>99B05</td>
<td>224nm*</td>
<td>9</td>
<td>34nm,23nm</td>
<td>None***</td>
<td>52.1-52.4%</td>
<td>BAE Gate Mask</td>
</tr>
<tr>
<td>13</td>
<td>F22 M33</td>
<td>97A3</td>
<td>433nm**</td>
<td>10</td>
<td>46nm,49nm</td>
<td>None***</td>
<td>50.9-51.6%</td>
<td>BAE Gate Mask</td>
</tr>
<tr>
<td>14</td>
<td>Ironman IBBI</td>
<td>94B3</td>
<td>136</td>
<td>16</td>
<td>48mm,50mm</td>
<td>N/A++</td>
<td>49.8-51.0%</td>
<td>Optimize Contacts; CD mean off-spec</td>
</tr>
<tr>
<td>15</td>
<td>Ironman IBBI</td>
<td>97A4</td>
<td>140</td>
<td>13</td>
<td>32nm,34nm</td>
<td>N/A++</td>
<td>50.7-50.9%</td>
<td>Round Contacts</td>
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<tr>
<td>16</td>
<td>Sample1</td>
<td>95C4</td>
<td>138</td>
<td>18</td>
<td>31nm,49nm</td>
<td>No defects in contacts</td>
<td>50.5-50.9%</td>
<td>Optimize contacts</td>
</tr>
<tr>
<td>17</td>
<td>Sample1</td>
<td>99B03</td>
<td>121</td>
<td>14</td>
<td>69mm,38nm</td>
<td>1 defect</td>
<td>53.1-53.5%</td>
<td>Optimize Contacts; IP off-spec</td>
</tr>
<tr>
<td>18</td>
<td>GRID130</td>
<td>102C6</td>
<td>102</td>
<td>12</td>
<td>70nm,51nm</td>
<td>2 defects</td>
<td>51.9-52.1%</td>
<td>Characterization Mask; IP off-spec</td>
</tr>
<tr>
<td>19</td>
<td>GRID130</td>
<td>102C6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same as 18</td>
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<tr>
<td>20</td>
<td>Ironman</td>
<td>99B06</td>
<td>122</td>
<td>12</td>
<td>32mm,44nm</td>
<td>N/A++</td>
<td>52.3-52.6%</td>
<td>IBBI Design Rev 4</td>
</tr>
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</table>

*CD Mean Target 220nm**CD Mean Target 450nm

**No brakes in gates; Nothing larger than 5um ++No KLA inspection required; gross defect spec only

---
### Mask Data – Year 2

<table>
<thead>
<tr>
<th>Slot</th>
<th>Mask</th>
<th>Lot</th>
<th>Image Size (100nm)</th>
<th>Uniformity (15nm)</th>
<th>Image Placement (50nm)</th>
<th>Defects (None)</th>
<th>Trans.</th>
<th>Notes</th>
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<tbody>
<tr>
<td>1</td>
<td>Zonemask</td>
<td>93A2</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>52.1-52.6%</td>
<td>IBBI Alignment marks Characterized</td>
</tr>
<tr>
<td>2</td>
<td>Zonemask</td>
<td>97B6</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>51.6-52.0%</td>
<td>IBBI Alignment marks Characterized</td>
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<tr>
<td>3</td>
<td>GRID2</td>
<td></td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td></td>
<td>100 nm Grid pattern</td>
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<td>N/A</td>
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<td>N/A</td>
<td>N/A</td>
<td></td>
<td>100 nm Grid pattern</td>
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<td>6</td>
<td>Iron Maiden</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
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<td></td>
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</tr>
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<td>9</td>
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<td></td>
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<td></td>
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<td></td>
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</tr>
</tbody>
</table>

### Mask Market Opportunities

- **CPL/ XRL Masks**
  - JMAR demos, testing, customers
  - BAES demos, product devices
  - Jefferson Lab (future?)
  - Canadian Customers - CLS
  - “Contacts” customers - <100 nm contacts
  - Overseas - process development customers
- **LEEPL**
- **EPL**
Serpentine pattern composed of 200,100, and 80nm features in a 3000Å initial thickness of CAP112.

90nm LINE/SPACE PAIRS ZIG ZAG ON 45 DEGREE ANGLE in 3000Å initial thickness OF CAP112
Summary

- CPL/XRL Mask activities will continue to be funded.

- JMAR will continue to market CPL/XRL systems and technology.

- Masks will be required by other customers.

Chalcogenide Random Access Memory Technology (C-RAM) and the Need for Micro-Lithography

5 November, 2003

J. Rodgers
BAE SYSTEMS

Chalcogenide Phase Change Memory Technology

- Mature thin film technology, compatible with CMOS processing
- Memory state stored as material phase change, not local charge storage
- Radiation hard - reflects response of base technology
- Large dynamic range
- Compact cell (1T1R)
- Excellent retention (10 years 120°C)
- No special packaging considerations
- Low programming current ~1mA / bit
- Low voltage operation: 3.3V, no high voltage supply, no charge pump
- Fast read / write (40 ns read / 400 ns write)
- Endurance (>10⁹ cycles demonstrated)
C-RAM Integration with CMOS

• C-RAM cell is inserted after transistor processing is completed but before first metal

• Volume of programmed material is small - presently 100 nm diameter circle, 50 nm thick

C-RAM Programming Current

• Current required to program the device is a function of material volume

• Scaling in thickness has limits and also affects other parameters

• Present method prints 350 nm hole which is reduced to 100 nm in etch

• Next generation scaling should go to 60 nm with direct printing

• Ultimate goal of 25 nm if printing uniformity OK

From Ovonyx website, www.ovonyx.com
Reducing C-RAM Cell Size

• 1.2 mA programming current drives overall cell size and therefore die size

• 4 Meg die in .25 µm RH-CMOS technology with 100 nm diameter pores will be approximately 10 mm x 10 mm

• Next generation projection is 16 Meg die in .15 um RH-CMOS
  – If 50 nm printing available and across die uniformity good then we can maintain 10 mm x 10 mm die size, assuming 75% reduction in current
  – 64 Meg die would be 17.4 mm x 17.4 mm under same assumptions

• Concern is uniformity across field of view because this drives programming current variation
  – Variation in present lithography process creates spread in required current and lowers yield

Reducing C-RAM Cell Size

• Fail bit-maps of large area memory array would be used as an indicator of image size uniformity and field of view fidelity
  – Mapping individual cell yield as a function of applied current indicates achieved image size (assuming uniform etch)

• Programming current also has effect on endurance
  – Smaller programmed volume requires less input power to heat to 600ºC
  – Lower power means less temperature rise in surrounding materials
  – 1E9 temperature cycles in materials with mis-matched expansion coefficients leads to device failure
  – Smaller devices with lower power should last longer
  – Intel has reported 1E12 demonstrated cycle life
Conclusion

- Direct printing of 50 nm holes in a large area C-RAM memory array would be an excellent demonstration of capability while increasing yield and cycle endurance in .25 µm, 4 Meg or .15 µm, 16 Meg C-RAM

- Present art dose not support 64 Meg C-RAM in .15 µm RH-CMOS technology so this demonstration may open a path to a new product, a plus to RadHard space community

- Fail bit-maps would be the metric to evaluate uniformity and fidelity over the large number of holes and large field of view of a C-RAM memory array
Application of X-ray Lithography to MMIC Fabrication for Military Applications

Maureen Roche

November 5, 2003

Need for X-Ray Lithography

- MMIC chips are backbone of radar, EW, missile seeker and communication systems
- Highest performance MMIC chips require sub 100 nm feature sizes.
  - Ka, V and W band applications ultimately need sub 100 nm MMICs for highest possible power added efficiency and lowest possible noise figure
  - Availability of sub 100nm gate MMICs enable phased array applications at 140 and 220 GHz
  - Provide performance margin for high yield manufacturing
- Currently, fabrication of 100 nm MMICs accomplished through direct write electron beam lithography; sub 100 nm chips cannot be fabricated with available e-beam systems at high throughput
- Alternate approach uses X-Ray Lithography System
MMIC Performance Drivers

- **Required performance improvements**
  - Higher power per millimeter of periphery
  - Higher efficiency
  - Lower noise figure
  - Lower receive power dissipation
  - Smaller Size
  - Higher gain
  - Improved linearity

- **Required device improvement**
  - Reduced gate length
  - Advanced materials structures
    - PHEMT
    - InP HEMT
    - Metamorphic HEMT

---

Military Applications for 50 nm MMICs

<table>
<thead>
<tr>
<th>Application</th>
<th>Freq. (GHz)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Seeker</td>
<td>94/140</td>
<td>140GHz allows smaller beam, better signal/clutter ratios</td>
</tr>
<tr>
<td>Concealed Weapons Detection, (CWD), and Through the Wall Surveillance, (TWS)</td>
<td>94/140</td>
<td>Passive and active video rate imaging; lower noise at 94GHz allows lower cost sparser array; higher resolution at 140GHz for hand held units</td>
</tr>
<tr>
<td>Autonomous Landing System, (ASL), and Independent Landing Monitor, (ILM)</td>
<td>94/140</td>
<td>All weather aircraft operation using video rate passive imaging; low noise and high resolution advantages at 94/140 respectively</td>
</tr>
<tr>
<td>Passive Seeker</td>
<td>94/140/220</td>
<td>All weather, high resolution, difficult countermeasures, LPI, straight down, video rate, end game applications</td>
</tr>
<tr>
<td>Airborne Surveillance</td>
<td>94/140</td>
<td>All weather, adverse environment, passive video rate imaging, battlefield surveillance and detection of relocatable targets</td>
</tr>
<tr>
<td>Hazard Avoidance Radar</td>
<td>220</td>
<td>Helicopter hazard avoidance; high cross section of suspended cables at 220 GHz makes it ideal</td>
</tr>
<tr>
<td>Meteorological Satellite, (METSAT)</td>
<td>183</td>
<td>Ground state of water vapor molecules at 183GHz; ideal for profiling atmospheric water vapor; key to METSAT forecasts</td>
</tr>
<tr>
<td>Earth Observation Satellites, (EOS)</td>
<td>100 to 500</td>
<td>Many molecular transitions of key atmospheric species; ideal for atmospheric sounding and other remote sensing applications</td>
</tr>
<tr>
<td>Vehicle Radar</td>
<td>150</td>
<td>Autonomous collision avoidance applications; vehicle stylists want smaller sensors provided by 150GHz operation</td>
</tr>
</tbody>
</table>
Best Reported MMIC LNAs

Missile Seeker Radar

- Current radar based Missile Seekers use single T/R Module and twist plate beam steering
- High G force missiles for ABM application need strapped down seekers
- Low cost 140GHz MMICs will enable phased array missile seekers with greatly improved target differentiation capability
**X-Ray Lithography Impact for Phased Arrays**

- Military applications of phased array antennas have significant MMIC content
- Large arrays required for spaced based imaging or communications
  - 25,000 elements
  - 300,000 MMICs
- Very low power dissipation LNAs are required to reduce array power dissipation
- Low cost sub-100nm gate MMICs will provide the low power dissipation solution for large space based arrays

---

**Roadblocks**

- MMIC industry cannot afford synchrotron installation, need stand alone system
  - Existing point source systems are immature; more work needed to improve throughput, reliability
- Mask availability
  - IBM X-ray mask shop closing
  - 1X masks impede sub-100nm development
  - Phase shift reduction printing attractive but no commercial source for X-ray phase shift masks
Conclusions

• Military requirement exists for affordable high performance millimeter wave MMICs for missile seekers
• 50 nm Gate Lengths are required for 160 to 220 GHz operation
• X-ray lithography has potential for producing such MMICs
• More investment is needed to assure availability of masks and to mature existing point source systems
X-Ray Lithography
Helios as the Source

GWYN P. WILLIAMS
Basic Research Program Manager
Jefferson Lab
12000 Jefferson Avenue - MS 7A
Newport News, VA 23606
gwyn@mailaps.org

XRL Comparative Costs – 2 years of running

Brookhaven - assume use of VUV ring for $4m/yr
Wisconsin $10m for 2 steppers
$0.5m for beamlines
$0.5m for management
$2m for cleanroom

Total cost for 2 years $22m

Helios-1 – recommissioning and ops 2 years $14.5m
$10m for 2 steppers
$2m for cleanroom
$0.5m for management

Total cost for 2 years $27m

Gwyn Williams prepared for discussion Nov. 4, 2003
XRL – Throughput

**Synchrotron source** ~ one 300 mm wafer / minute

**Point source** ~ one 300 mm wafer / day

Plus synchrotron reliability is > 95%

Basis for above

Brightness

Assume that we have a 10 watt source.

Z-pinch or laser plasma is into $4\pi$ sr

Synchrotron is into $10^{-6}$ sr

Ratio of $\frac{4\pi}{10^{-6}} \approx 10^7$

7 joules per wafer* means that synchrotron exposes in ~ 4 secs

while point source exposes in ~ 2 days

* assume 300mm wafer, = 707 cm² @ 10mJ/cm² = 7 joules/wafer

---

XRL – Synchrotron Power

30 cm wafer

= 707 cm²

@ 10mJ/cm²

Exposure time per wafer = 0.7s

for 10 watts
XRL – Synchrotron Power

XRL Range

- ~ 10 watts
- ~ 4 watts
- ~ 2.5 watts

Watts into a 10% bandwidth 50 m r. hor.

Photon Energy (eV)

Helios – Recommissioning $$

All loaded numbers, not direct costs.
Re-commissioning: Includes bldg. modification for linac plus 100x100 foot 2 story addition, shielding. $K

Modify FEL bldg for injector and power supplies 500
Building addition including utilities 4000
Magnet power supplies and controls 1000
RF power supplies and controls 600
Labor – installation (basis 10 people/10 weeks, rigging) 450
Liquid helium line 200
Re-commissioning (basis 3 people/1 year) 750
Beamlines 500
Project management 500
Contingency 1000

TOTAL 9,500

Gwyn Williams prepared for discussion Nov. 4, 2003
<table>
<thead>
<tr>
<th>Item</th>
<th>$K</th>
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<tbody>
<tr>
<td>Maintenance and supplies</td>
<td>700</td>
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<tr>
<td>1 Operator 24 x 7 (6 FTE’s)</td>
<td>750</td>
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<tr>
<td>Liquid helium</td>
<td>200</td>
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<tr>
<td>Project management</td>
<td>250</td>
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<tr>
<td>Utilities (including low-conductivity water)</td>
<td>100</td>
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<tr>
<td>Contingency</td>
<td>500</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td>2500</td>
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