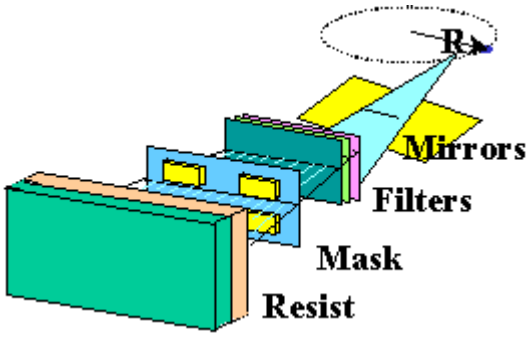
X-Ray Lithography towards 15 nm
2nd Meeting



The report of a meeting held November 5, 2003
At BAE Systems, Manassas, Virginia, USA in collaboration with Jefferson Lab (Newport News, Virginia), which is Operated by the United States Department of Energy under contract DE-AC05-84-ER40150

Table of Contents

Summary

This group met once before, on January 24, 2003 and a meeting report is available on line at: http://www.jlab.org/FEL/xrl_report_1.pdf. The group comprises a consortium of key technical executives representing a broad range of advanced lithography disciplines. At the previous meeting it was concluded that "it is essential that a modest x-ray lithography (XRL) program be developed as soon as possible to re-define a road-map for x-ray processes to assure the maintenance of US competitiveness". The group further concluded that "there are no show-stoppers".

Given this background, this second meeting decided to focus on a specific product or products, to try to define a project that might re-ignite XRL within the semiconductor industry. In order to accomplish this, representatives from all the necessary technologies, sources, steppers, masks, and manufacturing, were present.

The meeting began with an introduction to NGL by Martin Richardson, (University of Central Florida), at which the key issues were related to the semiconductor technology road map. Current goals are 40 wafer levels per hour with 300mm wafers, and with EUV insertion in 2008-2009 at the 35 nm level. Within the context of EUVL, details of source intensity and collimating mirror survival problems were presented. This was followed by a presentation by Bob Selzer (JMAR) on the situation pertaining to x-ray masks. Current capability exists to produce 25 masks per year on 2 micron SiC membranes with 500 nm TaSi absorbers. The masks have a surface flatness of < 5 microns. John Rodgers (BAE Systems, Manassas) then presented a proposal to develop C-RAM chips using x-ray lithography to reduce the current dimensions so that, for example, a 64 Mbit or greater C-RAM might be produced. C-RAMs use chalcogenide phase-change technology for non-volatile radiation hardened memory switchable with 3.3 volts and accessible within a few 10's of nanoseconds. Maureen Roche (BAE Systems, Nashua) then presented details of programs involving XRL to MMIC chips and phase arrays. Finally Gwyn Williams (Jefferson Lab) presented details of current synchrotron sources at Wisconsin, Brookhaven and Jefferson Lab, including delivered power, brightness and costs of operation.

A discussion followed, which initially considered whether the scope of any BAE Systems projects was large enough, by itself, to drive an initiative to set up a synchrotron-based XRL facility as an enabling cost-effective technological solution. Clearly none of the existing projects is sufficient to drive such a large ($30m over 2 years) venture.

The discussion then focused on methods of convincing the industry of the value and advantages of XRL. The group learned from Fred Dylla (Jefferson Lab) that Sematech had expressed interest in XRL to him at the AVS 50th. Symposium this week, and specifically had asked for a report of this meeting at their meeting in January 2004.

Marty Peckerar then made a bold proposal, namely that of initiating a project to make C-RAMs at 30 – 50 nm design rules, thereby demonstrating the capability of XRL in a product that the industry might find particularly attractive, and one that could not be manufactured today in quantity by any other method. Such a product would yield at least a 64 Mbit radiation hardened, non-volatile memory chip requiring only 3.3 volts, and with access times in the 10's of nanoseconds, and lifetimes in the 10^9 cycle range.

This proposal was enthusiastically supported and seemed achievable with low risk. Bob Selzer stated that if a request for a mask were made before November 19, 2003, then a

mask could be manufactured by mid-December. It seemed clear that since the mask would be based on scaling from an existing prototype, this request was achievable. Therefore it would be reasonable to think of making exposures starting in mid-December. It was decided that Mitch Burte would refine this outline plan and present details to a DARPA review in 2 weeks.

The plan would involve scaling existing masks to smaller design rules, therefore the initial products would be small-scale versions of existing ones. The plan would be to have the first product ready in January 2004.

Appendix A – Agenda

X-Ray Lithography, towards 15nm
2nd Meeting November 5, 2003
Bldg. 110, BAES Manassas, Virginia

8:00	Continental Breakfast	
9:20	Welcome	Steve Schnur, BAE Systems
9:30	Introduction to NGL	Martin Richardson, University of Central Florida
10:15	XRL masks	Bob Selzer, JMAR
10:45	C-RAMs	John Rodgers, BAE Systems
11:15	GaAs MMIC applications of XRL	Maureen Roche, BAE Systems
11:45	Synchrotron Sources	Gwyn Williams, Jefferson Lab
12:15	Lunch	
1:00	Discussions	

Brainstorming topics

·What does a synchrotron-based x-ray lithography program need to be successful?
- –1a. Resolution
- –1b. Overlay
- –1c. Throughput
- –1d. Realistic Insertion Date
- –1e. Reliability
- –1f. Cost Benefit

·What needs to be done to meet the above specifications?
·What can each party do to contribute to bringing HELIOS back on-line?
·What other equipment is needed in addition to the ring and a stepper?
Photoresist Processing Capability
Environmental Stability

·What would each party use the ring and a stepper for if it were back on line?
··Would BAE Systems lead one or more programs from Manassas and/or Nashua?

·Are there other parties who would want to use and should be allowed to use the ring?
- –Corporations?
- –Universities?
- –Government Labs?

·How will we fund the project to build a building and install the ring and stepper?
··How will we fund lithography demonstrations and device demonstrations using x-ray lithography?

3:00 Adjourn

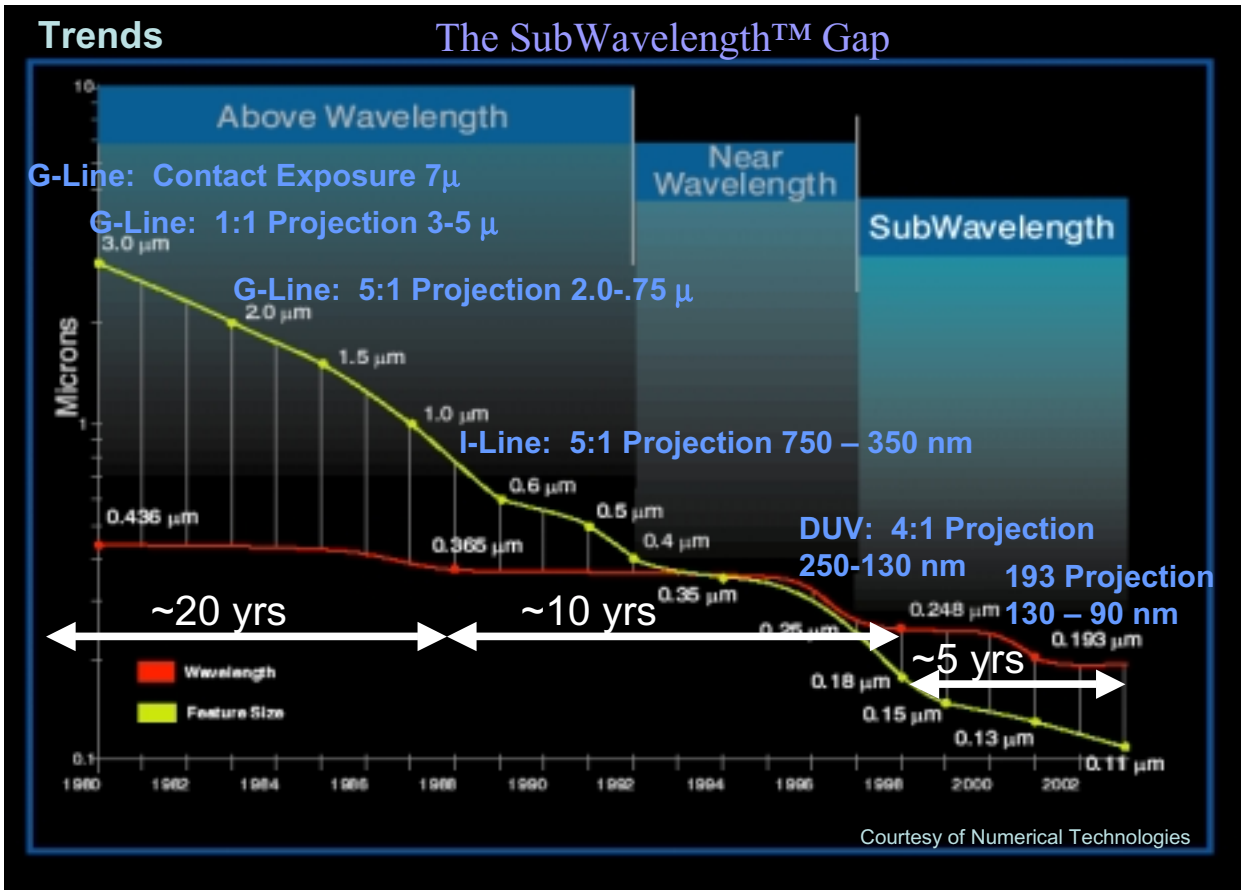
Appendix B – Participants

Andy Pomerene	BAE Systems	andrew.pomerene@baesystems.com
Tom McIntyre	BAE Systems	thomas.mcintyre@baesystems.com
Peter Spreen	Leica Microsystems	peter.spreen@leica-microsystems.com
Steve Schnur	BAE Systems	steven.schnur@baesystems.com
Heinz Siegert	JMAR Systems	Hsiegert@nanolitho.com
Bob Selzer	JMAR Systems	BobSelzer@nanolitho.com
Maureen Roche	BAE Systems	maureen.roche@baesystems.com
Antony Bourdillon	UhrlMasc	bourdillona@prodigy.net
Martin Richardson	UCF/CREOL	mcr@creol.ucf.edu
Gwyn Williams	Jefferson Lab	gwyn@mailaps.org
Ari Tuchman	Technoventures/UMD	ari@technoventures.com
Marty Peckerar	U of MD	peckerar@eng.umd.edu
Yuli Vladimirsky		yvladimirsky@juno.com
Marty Polavaradu	BAE Systems	marty.polavaradu@baesystems.com
John Rodgers	BAE Systems	john.Rodgers@baesystems.com
Mitch Burte	BAE Systems	Mitchell.j.burte@baesystems.com
Nadim Haddad	BAE Systems	nadim.haddad@baesystems.com
Glenn Marshall	NAVAIR	glenn.marshall@navy.mil
Fred Dylla	Jefferson Lab	dylla@jlab.org
Dave Patterson	DARPA/MTO	dpatterson@darpa.mil

Perspective on X-ray Lithography

Martin Richardson
Laser Plasma Laboratory
School of Optics/CREOL, University of Central Florida,
Orlando,
Tel 407 823 6819 Fax 407 823 3570 email: mcr@creol.ucf.edu

Manassas, November 5, 2003



A roadmap re-written – many times

Early 90's *Four NGL's* *XRL, EBL, IBI and 'soft X-ray Lithography* ~~*EUVL*~~

~~*130 nm*~~ *insertion at the 180 nm node*

10W (2π at the source) required XRL..and EUVL

XRL with SRS the most robust

A roadmap re-written – many times

Laser Plasma Laboratory School of Optics / CREOL

Early 90's *Four NGL's* *XRL, EBL, IBI and 'soft X-ray Lithography* ~~*EUVL*~~

~~*130 nm*~~ *insertion at the 180 nm node*

10W (2π at the source) required XRL..and EUVL

XRL with SRS the most robust

End of 90's *DUV extended , 157 nm on the scene*

ISMT 'prioritizes' EUVL, then EBL….~~*IBL*~~ *and* ~~*XRL*~~

40 wl/h, 300 mm dia. wafers

UCF "Perpspective on Lithography" M. Richardson, presented at BAE/Jefferson Lab Workshop Nov. 5, 2003

A roadmap re-written – many times

Early 90's *Four NGL's* *XRL, EBL, IBI and 'soft X-ray Lithography* ~~*130 nm insertion at the 180 nm node*~~ *EUVL*

10W (2π at the source) required XRL..and EUVL

XRL with SRS the most robust

End of 90's *DUV extended , 157 nm on the scene*

ISMT 'prioritizes' EUVL, then EBL….IBL and XRL

40 wl/h, 300 mm dia. wafers

Now ***EUVL is the 'NGL'….*** ~~***157***~~ ***….but immersion, imprint and PM?***

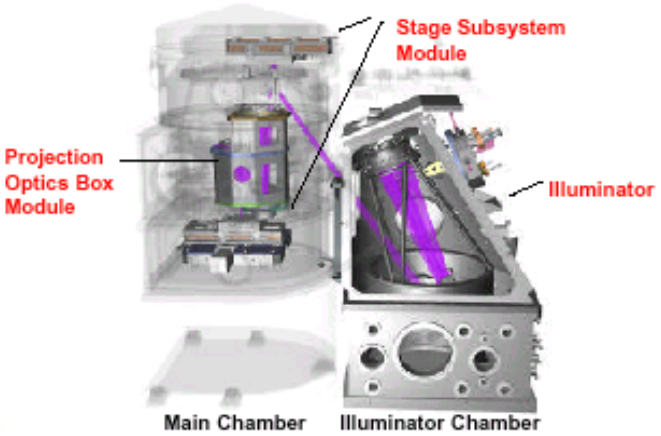
EUVL insertion at 35 nm…" need for investment stage"

EUVL - The status

Insertion in 2008 -2009

155 wl/h, 300 mm dia. wafers,
11 -14 layers,
2-3 level resists - 5mJ/cm²

13.5 nm Multilayer Mirrors
Mo/Si max R = 70%



CRITICAL ISSUES

1. ***Source power 100 W at IF -***
   - this means 400 W (2π) at source LP , 700 W for DP
2. ***Mirror erosion…from ions of source***
3. ***Mask repair***

A Reality check …and some questions

Optical Lithography IS now coming to an end

One-size-fits all…is this true?

Moore's Law aside …the future may not look like the past

NGL's in Si only required for some critical elements….

New Materials….GaAs, InP….
…different markets, different requirements…

Is there room for a more flexible strategy?

XRL - a resurgence of interest?

What are the prospects for XRL?
- *with or without a Si option*
- *new materials, new devices, processes…*

Are there near-term needs for XRL?
- *GaAs ?*
- *MMICs and interconnects….*

Role of academic research…..

An open XRL SRS facility at Jefferson?
- *what needs would it serve?*
- *would it spur increased interest in XRL?*
- *performance, facilities, costs, etc…*

BAE SYSTEMS

X-Ray Lithography Workshop
presented by
Jefferson Labs and BAE Systems
BAE Systems
Manassas, VA

Infrastructure - Status of U.S. mask-making capabilities

Bob Selzer – JMAR Systems

November 5, 2003
9:00AM-3:00PM

BAE SYSTEMS

CPL/XRL Mask Status

- **Program Overview**
- **Mask Manufacturing Equipment**
- **Mask Requirements**
- **Mask Deliveries**
- **Opportunities**
- **Summary**

CPL/XRL Mask Status

Program Overview

-DARPA/ NAVAIR has funded in 2002 - 2003, the continuation of X-ray mask technology. Future years will be supported through congressional plus ups or directly by customers. 2004 now funded.

-Through Dec 2003 a cooperative effort with IBM Mask Operations in Essex Junction, VT. has provided ~25 masks per year. - Each of the first two years IBM has been contracted to build per JMAR defined criteria.

Year 1: 130nm requirements
MMIC like devices, test patterns for litho POC
Year 2: 100nm requirements
MMIC like devices, test patterns for litho demo

-Most masks were laid out by JMAR mask designers and submitted to IBM for writing.

Mask Manufacturing Equipment

Tool	Function	Location
Sputter Films Endeavor PVD	Absorber deposition	IBM Essex Jct. VT
Eaton Summit RTA	Absorber anneal	
PlasmaTherm SLR 730 PECVD	Hard mask deposition	
SUSS ACS 200 Resist Coater	Resist Coat	
IBM EL-4+ E-beam Writer	Pattern Writing	
APT	Develop	
PlasmaTherm SLR 700	Descum; Hard mask etch	
PlasmaTherm ECR	Absorber Etch	
AMRAY 2040 CD-SEM	Image Size	
Leica LMS 2020	Image Placement	
KLA SEMSpec	Defect Inspection	
Micrion 8000 FIBS	Mask Repair	

Mask Requirements

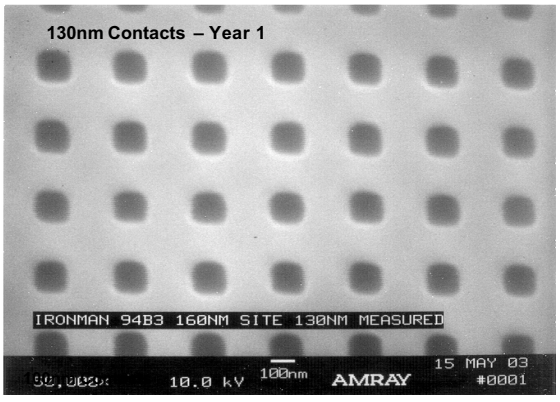
- NIST Ring format – bonded wafer to ring
- Membrane SiC
  - **Nominal thickness 2um**
  - **+/- 2.5% thickness variance**
  - **Optical transmission @ 500-600nm - 50%**
- Absorber material thickness
  - **450 - 500nm TaSi or equivalent**
  - **+/- 2.5% thickness variance**
- Flatness
  - **Membrane**
    - **< 3um TIR**
  - **Mask surface**
    - **< 5um TIR**

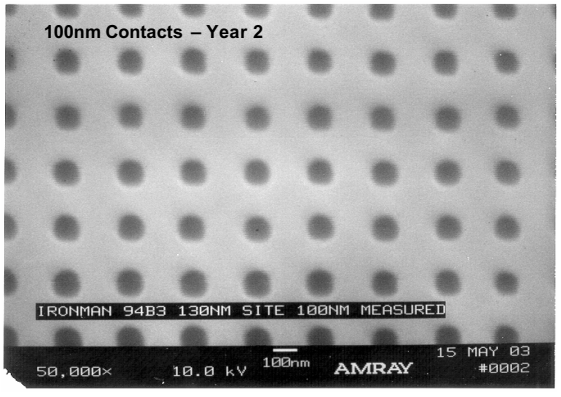
Mask Requirements

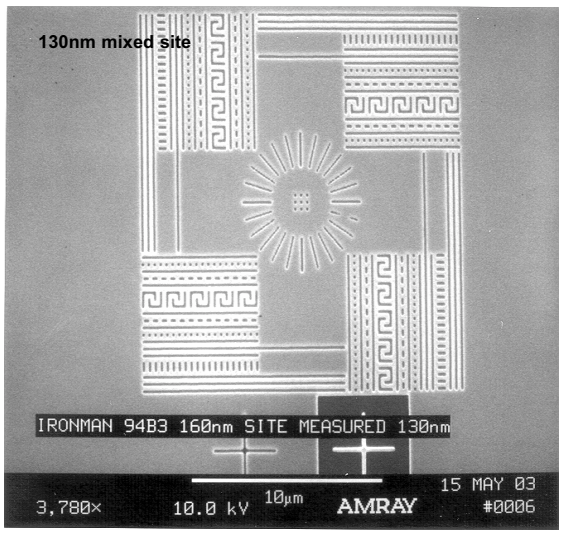
Specification	nominal	tolerance / range	comments
Membrane size	35 x 35mm	25- 50mm^2	range is for usable membrane sizes
Membrane centrality	center	+/- 0.25mm	
Outlying Windows	na	na	Capability? (AWIS doesn't require)
Image size - isolated	100nm	10nm 3sigma	line and contact hole
Nested to Isolated delta	10nm	10nm 3sigma	
Edge roughness	< 10%	na	
Corner rounding	> 60%	na	% of 100nm feature to be square
Nested to Isolated delta	10nm	10nm 3sigma	
Line end shortening	10nm	10nm 3sigma	provide measurements to minimum
Linearity	100-200nm	10nm 3sigma	resolved feature
Image Placement	50nm	50nm	Mean + 3-sigma
Systematic, X & Y scale, Ortho	1.5ppm	na	This design does not require, What are
Image Magnification correction	0ppm	na	capabilities?
Mask contrast		na	Dark field
Defect specification	25% of feature size	down to 90nm features	Feature spec, no breaks in gates
Surface defect specification	< 2um		
Chip size	24mm^2		single chip
Data mirror	na	na	Data is E-beam ready
V-notch orientation	na	na	Data is E-beam ready
Average transmission, cleared areas	> 50%	na	average value 400-580nm light

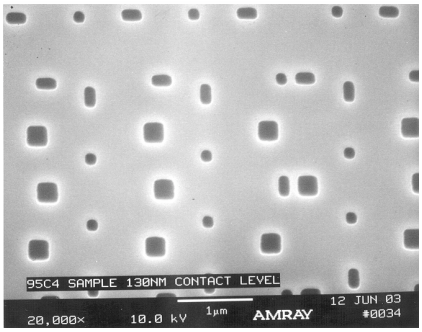
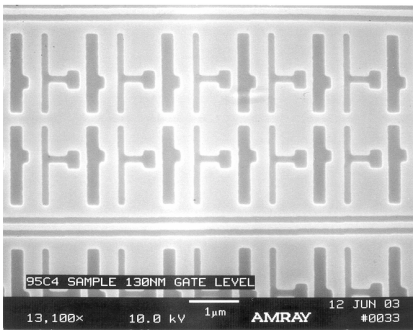
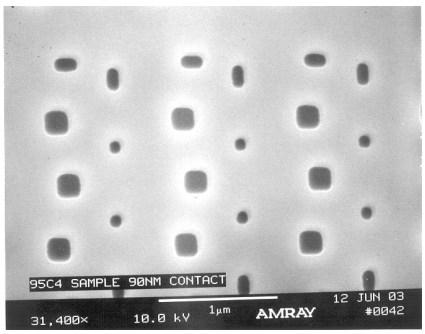
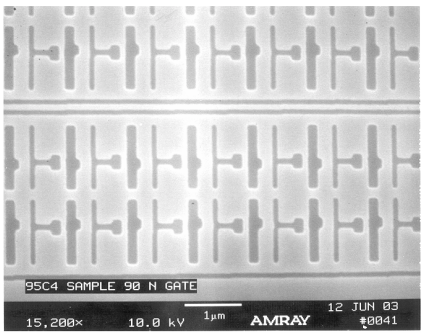
Mask Requirements

- Nominal feature 130-100nm, statistical sample.
  - Image size
  - Line end shortening
  - Corner rounding
  - Edge roughness
- Linearity, Statistical sample nested & isolated.
  - Minimum resolution to 200nm
- Placement, Systematic errors
  - Across membrane sample
  - Across data sample
  - Tool specific contribution sample
  - Sub field metrology for shape beam writers
- SEM images of nominal & best can do resolution
  - Edge roughness
- SEM images of defects.
- Transmission
- Centrality







	Contact Level	Gate Level
130nm		
90nm		

Sample Form

X-Ray Mask Request Form

Order Date 9/ 4 /2003 **Quantity**_2_ **Requested delivery Date** _ / /2003
2003 Slots 7 & 8
Mask Name __CNTech2003B **Instance** _#1&2 **Level(s)** ___Prime___
Customer Name___ JMAR_____ **E-mail** ___bgrenon@together.net_____
Customer Contact__ Brian J. Grenon_____ **Telephone #**__802-862-4551
For complete design and build requirements, refer to Mask design guide and associated drawings.

Mask Product Specifics

- Image Size Specification for mask quality definition.
  (Nominal _100nm, mean from nominal __10nm, uniformity __25nm-3s)
- Nested to Isolated maximum delta (Optimize 100nm contact quality)
- Image size X-Y (__15nm-3s)
- Customer specified bias (None)
- Image Placement Specification (50nm-3 s)
- Centrality, Chip to NIST ring (500 um)
- Membrane dimensions Chip area (X-35mm, Y- 35mm)
- Membrane center placement, Chip area (X-0mm, Y- 0mm)
- Membrane placement accuracy Chip area (+/-_500um)
- Membrane dimensions Outlying areas (none)
- Membrane center placement, Outlying area (none)
- Membrane placement accuracy outlying area (none)
- Defect Specification (no gross defects or raised defects over 2um)
- Image Placement Magnification Corrections (none)
- Systematic Tolerance. SF__2.0ppm ; Ortho__2.0ppm
- Mask Contrast (Dark field)
- Chip Size (X: 28mm Y: 28mm)
- Stepping Periodicity, Number of Die (na)
- V-notch orientation: down when mask name is readable backside.__
- Data mirror (data will be ready for E-beam, no flips required PRIME cell)
- Edge Roughness (_None_)
- Corner rounding – feature size / radius (best can do)
- Line end shortening, IS – Shortening, (na)
- Linearity, IS range – max variance (na)
- Transmission through alignment areas (>=50%) Clear all targets.

Input Data Format

- GDS-II
  Prime Cell _PRIME ___
- Reticle Layout map (attached .jpg)
- JMAR Supplied data

Mask Deliveries

BAE SYSTEMS

Slot	Mask Mask Orders	Order Date	GDS Data Ready	Commit Date	Ship Date	Status
1	Throughput Mask	5/31/02	6/11/02	7/1202	6/12/02	Delivered
2	Throughput Mask	6/27/02	6/11/02	8/8/02	7/12/02	Delivered
3 3A	Throughput Mask	9/6/02	6/11/02	10/18/02	9/26/02 10/16/02	
4	Throughput Mask	9/6/02	6/11/02	10/4/02	10/4/02	
5	Ironman	9/19/02	9/13/02	10/31/02	10/31/02	
6	DMS 173 MMIC	10/10/02	10/10/02	11/21/02	11/14/02	
7	ROBOMASC	11/14/02	11/14/02	12/26/03	1/2/03	
8	ROBOMASC	12/19/02	11/14/02	1/30/03	1/17/03	
9	Ironman	1/29/03	9/13/02	1/29/03	1/29/03	
10	F22 M72	2/10/03	2/28/03	3/28/03	3/28/03	
11	F22 M75	2/10/03	2/28/03	3/28/03	3/27/03	
12	F22 M71	2/10/03	2/28/03	4/4/03	4/3/03	
13	F22 M33	2/10/03	2/28/03	4/4/03	4/3/03	
14	Ironman	1/31/03	2/21/03	5/2//03	5/23/03	
15	Ironman	1/31//03	2/21/03	5/2/03	5/28/03	
16	Sampler1	2/10/03	2/17/03	5/9/03→ 6/18/03	6/16/03	
17	Sampler1	2/10/03	2/20/03	5/9/03	7/24/03	
18	Grid130	5/22/02	4/18/03	7/3/03	8/12/03	
19	Grid130	5/22/03	4/18/03	7/3/03	8/19/03	
20	Ironman	5/16/03	2/14/02	6/27/03	6/19/03	

J·MAR TECHNOLOGIES, INC.

BAE SYSTEMS

Mask Orders - Year 2

Slot	Mask	Order Date	GDS Data Ready	Commit Date	Ship Date	Status
1	ZONEMASK	5/27/03	5/20/03	7/14/03	6/6/03	Mask 93A2 shipped
2	ZONEMASK	5/27/03	5/20/03	7/14/03	6/12/03	Mask 97B6 shipped
3	GRID100	8/22/03	8/22/03	10/03/03	10/10/03	Mask 99C04 @repair
4	GRID100	8/22/03	8/22/03	10/03/03	10/10/03	Mask 102C4 @ repair
5	IronMaiden	9/10/03	8/26/03	10/22/02	11/03/03	Mask 97B4
6	IronMaiden	9/10/03	8/26/03	10/22/03		Mask 97B6
7	CNT2003	9/04/03				Data under review
8	CNT2003	9/04/03				Data under review
9	DMS 227	10/27/03	10/6/03	12/8/03	11/03/03	In mask build
10	DMS 256	10/27/03	10/29/03	12/10/03		In mask build
11	DMS256	10/27/03	10/29/03	12/10/03		In mask build
12	IronMaiden V2	10/27/03	10/27/03			In mask build; ALX70 coordinates needed
13						
14						
15						
16						
17						
18						
19						
20						

J·MAR TECHNOLOGIES, INC.

Mask Data -Year 1

Slot	Mask	Lot	Image Size	Uniformity (15nm)	Image Placement (50nm)	Defects (None)	Trans.	Notes
1	Throughput Mask	94C5	112nm	8nm	58nm,42nm*	N/A++	50.0-51.1%	IBM test pattern AM's; relaxed spec
2	Throughput Mask	95B5	134nm	8nm	49nm,45nm	N/A++	51.0-52.2%	IBM test pattern AM's; relaxed spec
3	Throughput Mask	98A6	138nm	8nm	68nm,45nm*	N/A++	52.0-52.4% 53.7-54.0%	IBM test pattern AM's; relaxed spec
3A 4	Throughput Mask	98B4	132nm	7nm	54nm,50nm*	N/A++ N/A++		IBM test pattern AM's; relaxed spec
5	Ironman	97A1	126nm	12nm	38nm,39nm	N/A+	52.4-53.1%	JSAL Design
6	DMS 173 MMIC	98C2	138nm	6nm	31nm,27nm		50.1-50.8%	BAE Gate mask
7	ROBOMASC	98B3	N/A Read/Rec	N/A	N/A	N/A++	51.9-52.5%	Resolution mask
8	ROBOMASC	97B1	N/A Read/Rec	N/A	N/A	N/A++	53.0-53.0%	Resolution Mask
9	Ironman	97B5	126nm	13nm	29nm,45nm	N/A++	TBD	JSAL Design

*PSE sendaheads to assure 50nm image placement were waived by JSAL to assure faster TAT

+Mask returned to IBM ++No KLA inspection required; gross defect spec only

Mask Data -Year 1

Slot	Mask	Lot	Image Size (130nm)	Uniformity (15nm)	Image Placement (50nm)	Defects (None)	Trans.	Notes
10	F22 M72	99A06	218nm*	14nm	50nm,44nm	None***	52.2-52.4%	BAE Gate Mask
11	F22 M75	99B03	221nm*	12nm	45nm,45nm	None***	52.7-53.0%	BAE Gate Mask
12	F22 M71	99B05	224nm*	9nm	34nm,23nm	None***	52.1-52.4%	BAE Gate Mask
13	F22 M33	97A3	433nm**	10nm	46nm,49nm	None***	50.9-51.6%	BAE Gate Mask
14	Ironman IBBI	94B3	136nm	16nm	48nm,50nm	N/A++	49.8-51.0%	Optimize Contacts; CD mean off-spec
15	Ironman IBBI	97A4	140nm	13nm	32nm,34nm	N/A++	50.7-50.9%	Round Contacts
16	Sample1	95C4	138nm	18nm	31nm,49nm	No defects in contacts	50.5-50.9%	Optimize contacts
17	Sample1	99B03	121nm	14nm	69nm,38nm	1 defect	53.1-53.5%	Optimize Contacts IP off-spec
18	GRID130	102C6	102nm	12nm	70nm,51nm	2 defects	51.9-52.1%	Characterization Mask IP off-spec
19	GRID130	102C6						Same as 18
20	Ironman	99B06	122nm	12nm	32nm,44nm	N/A++	52.3-52.6%	IBBI Design Rev 4

*CD Mean Target 220nm**CD Mean Target 450nm

***No brakes in gates; Nothing larger than 5um ++No KLA inspection required; gross defect spec only

Mask Data – Year 2

Slot	Mask	Lot	Image Size (100nm)	Uniformity (15nm)	Image Placement (50nm)	Defects (None)	Trans.	Notes
1	Zonemask	93A2	N/A	N/A	N/A	N/A	52.1-52.6%	IBBI Alignment marks Characterized
2	Zonemask	97B6	N/A	N/A	N/A	N/A	51.6-52.0%	IBBI Alignment marks Characterized
3	GRID2							100 nm Grid pattern
4	GRID2							100 nm Grid pattern
5	Iron Maiden							
6	Iron Maiden							
7								
8								
9								
10								

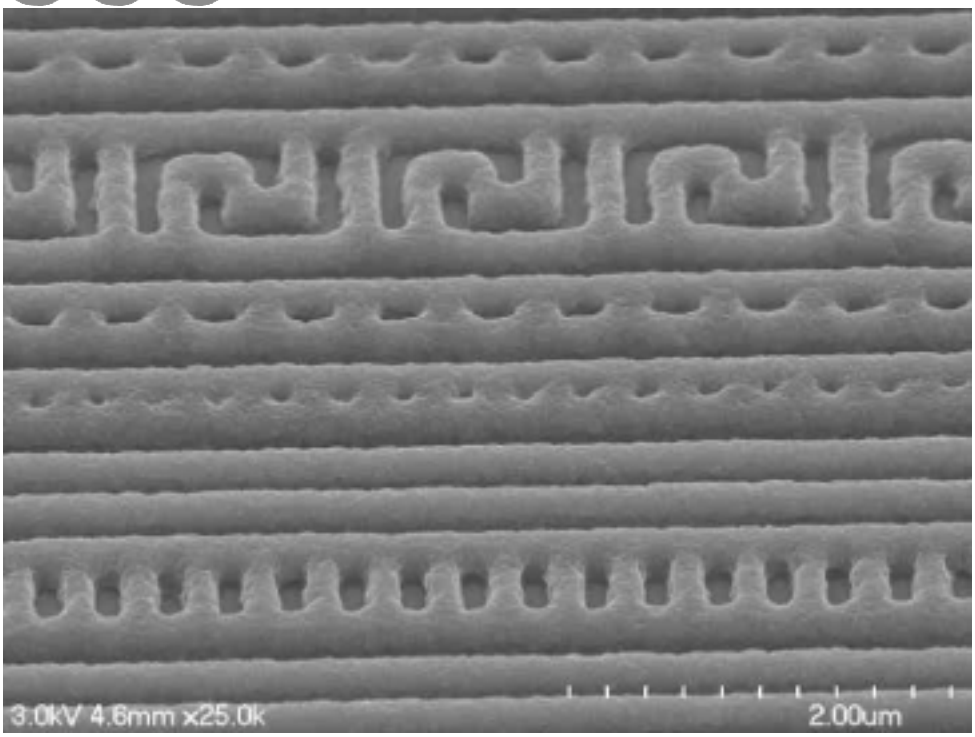
Mask Market Opportunities

- **CPL/ XRL Masks**
  - JMAR demos, testing, customers
  - BAES demos, product devices
  - Jefferson Lab (future?)
  - Canadian Customers - CLS
  - “Contacts” customers - <100 nm contacts
  - Overseas - process development customers
- **LEEPL**
- **EPL**

Jefferson Lab

BAE SYSTEMS

CAP112 IRONMAN

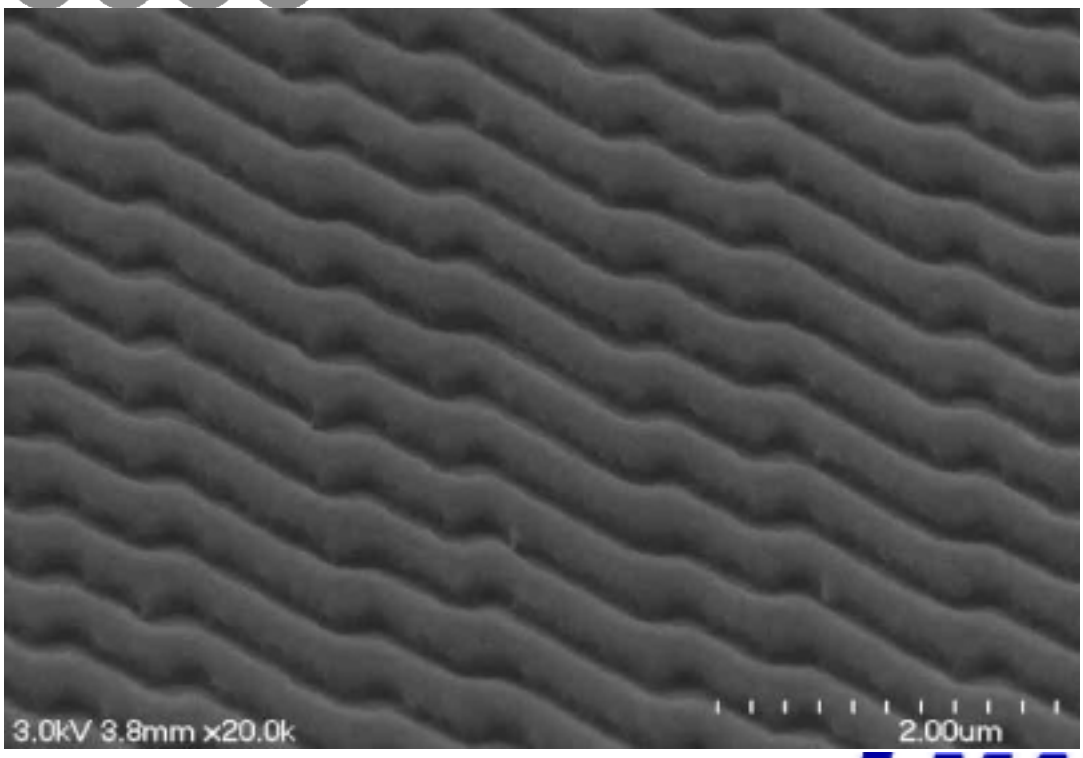


Serpentine pattern composed of 200,100, and 80nm features in a 3000A initial thickness of CAP112.

J·MAR TECHNOLOGIES, INC

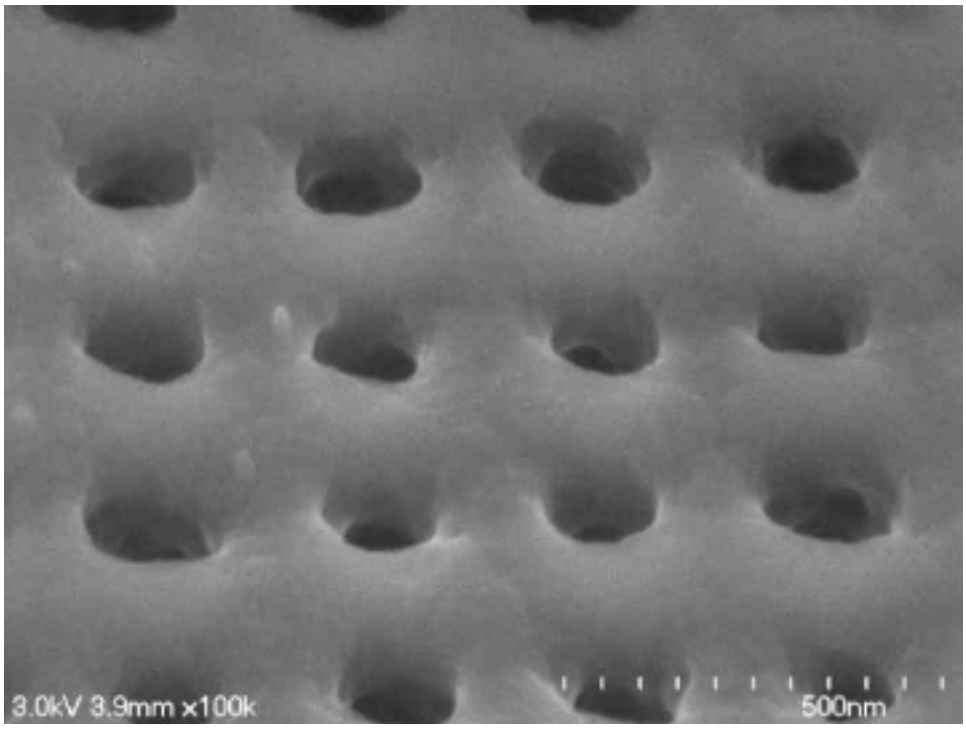
Jefferson Lab

BAE SYSTEMS



90nm LINE/SPACE PAIRS ZIG ZAG ON 45 DEGREE ANGLE in 3000A initial thickness OF CAP112

J·MAR TECHNOLOGIES, INC



90nm CONTACTS IN 3000A INITIAL THICKNESS OF CAP112

Summary

- CPL/ XRL Mask activities will continue to be funded.
- JMAR will continue to market CPL/ XRL systems and technology.
- Masks will be required by other customers.
- Future CPL mask requirements extend to 80nm in 2004, 70 nm 2005, 50nm in 2006, 45nm in 2007.

BAE SYSTEMS

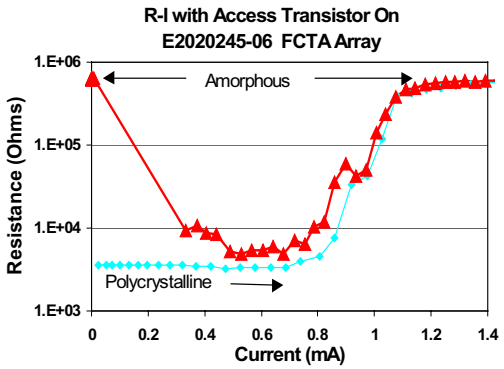
Chalcogenide Random Access Memory Technology (C-RAM) and the Need for Micro-Lithography

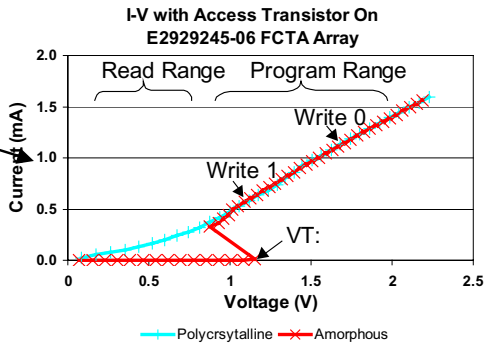
5 November, 2003

J. Rodgers
BAE SYSTEMS

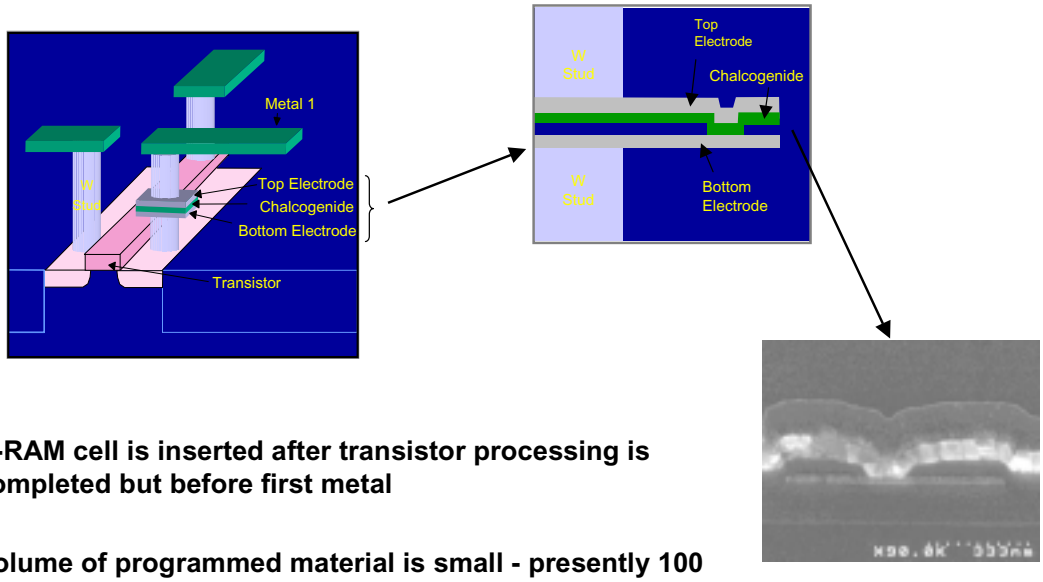
Chalcogenide Phase Change Memory Technology

- Mature thin film technology, compatible with CMOS processing
- Memory state stored as material phase change, not local charge storage
- Radiation hard - reflects response of base technology
- Large dynamic range
- Compact cell (1T1R)
- Excellent retention (10 years 120°C)
- No special packaging considerations
- Low programming current ~1mA / bit
- Low voltage operation: 3.3V, no high voltage supply, no charge pump
- Fast read / write (40 ns read / 400 ns write)
- Endurance (>10^9 cycles demonstrated)



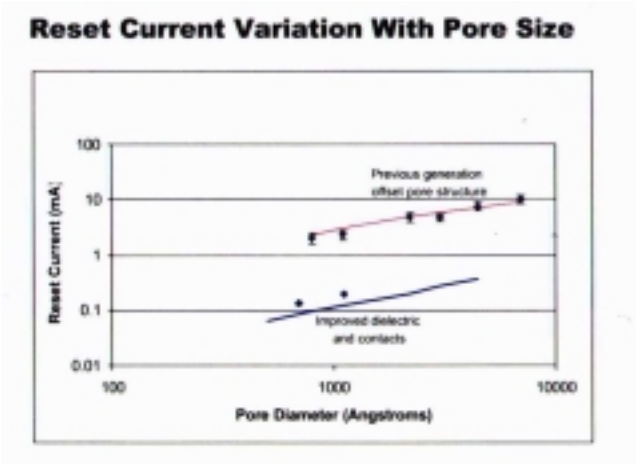


C-RAM Integration with CMOS



- C-RAM cell is inserted after transistor processing is completed but before first metal
- Volume of programmed material is small - presently 100 nm diameter circle, 50 nm thick

C-RAM Programming Current



From Ovonyx website, www.ovonyx.com

- Current required to program the device is a function of material volume
- Scaling in thickness has limits and also affects other parameters
- Present method prints 350 nm hole which is reduced to 100 nm in etch
- Next generation scaling should go to 60 nm with direct printing
- Ultimate goal of 25 nm if printing uniformity OK

Reducing C-RAM Cell Size

- 1.2 mA programming current drives overall cell size and therefore die size
- 4 Meg die in .25 µm RH-CMOS technology with 100 nm diameter pores will be approximately 10 mm x 10 mm
- Next generation projection is 16 Meg die in .15 um RH-CMOS
  - If 50 nm printing available and across die uniformity good then we can maintain 10 mm x 10 mm die size, assuming 75% reduction in current
  - 64 Meg die would be 17.4 mm x 17.4 mm under same assumptions
- Concern is uniformity across field of view because this drives programming current variation
  - Variation in present lithography process creates spread in required current and lowers yield

Reducing C-RAM Cell Size

- Fail bit-maps of large area memory array would be used as an indicator of image size uniformity and field of view fidelity
  - Mapping individual cell yield as a function of applied current indicates achieved image size (assuming uniform etch)
- Programming current also has effect on endurance
  - Smaller programmed volume requires less input power to heat to 600ºC
  - Lower power means less temperature rise in surrounding materials
  - 1E9 temperature cycles in materials with mis-matched expansion coefficients leads to device failure
  - Smaller devices with lower power should last longer
  - Intel has reported 1E12 demonstrated cycle life

Conclusion

- **Direct printing of 50 nm holes in a large area C-RAM memory array would be an excellent demonstration of capability while increasing yield and cycle endurance in .25 µm, 4 Meg or .15 µm, 16 Meg C-RAM**

- **Present art dose not support 64 Meg C-RAM in .15 µm RH-CMOS technology so this demonstration may open a path to a new product, a plus to RadHard space community**

- **Fail bit-maps would be the metric to evaluate uniformity and fidelity over the large number of holes and large field of view of a C-RAM memory array**

BAE SYSTEMS

Application of X-ray Lithography to MMIC Fabrication for Military Applications

Maureen Roche

November 5, 2003

Need for X-Ray Lithography

BAE SYSTEMS

- MMIC chips are backbone of radar, EW, missile seeker and communication systems
- Highest performance MMIC chips require sub 100 nm feature sizes.
  - Ka, V and W band applications ultimately need sub 100 nm MMICs for highest possible power added efficiency and lowest possible noise figure
  - Availability of sub 100nm gate MMICs enable phased array applications at 140 and 220 GHz
  - Provide performance margin for high yield manufacturing
- Currently, fabrication of 100 nm MMICs accomplished through direct write electron beam lithography; sub 100 nm chips cannot be fabricated with available e-beam systems at high throughput
- Alternate approach uses X-Ray Lithography System

MMIC Performance Drivers

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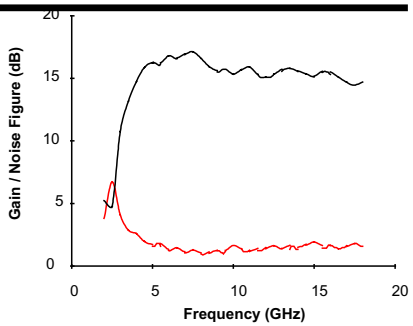
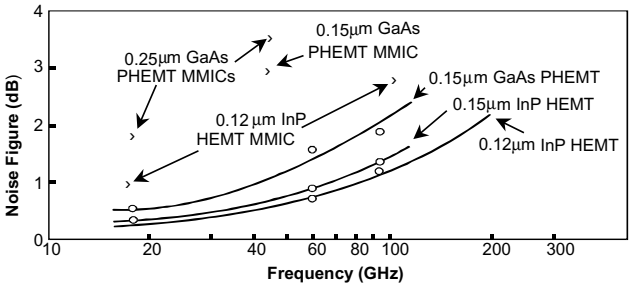
- Required performance improvements
  - Higher power per millimeter of periphery
  - Higher efficiency
  - Lower noise figure
  - Lower receive power dissipation
  - Smaller Size
  - Higher gain
  - Improved linearity
- Required device improvement
  - Reduced gate length
  - Advanced materials structures
    - PHEMT
    - InP HEMT
    - Metamorphic HEMT



Gain and Noise Figure Performance of Wideband LNA for Military Application



Transition to Advanced Materials and Smaller Gate Length Improves MMIC Noise Figure

Military Applications for 50 nm MMICs

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Application	Freq, (GHz)	Comments
Active Seeker	94/140	140GHz allows smaller beam, better signal/clutter ratios
Concealed Weapons Detection, (CWD), and Through the Wall Surveillance, (TWS)	94/140	Passive and active video rate imaging; lower noise at 94GHz allows lower cost sparser array; higher resolution at 140GHz for hand held units
Autonomous Landing System, (ASL), and Independent Landing Monitor, (ILM)	94/140	All weather aircraft operation using video rate passive imaging; low noise and high resolution advantages at 94/140 respectively
Passive Seeker	94/140/220	All weather, high resolution, difficult countermeasures, LPI, straight down, video rate, end game applications
Airborne Surveillance	94/140	All weather, adverse environment, passive video rate imaging, battlefield surveillance and detection of relocatable targets
Hazard Avoidance Radar	220	Helicopter hazard avoidance; high cross section of suspended cables at 220 GHz makes it ideal
Meteorological Satellite, (METSAT)	183	Ground state of water vapor molecules at 183GHz; ideal for profiling atmospheric water vapor; key to METSAT forecasts
Earth Observation Satellites, (EOS)	100 to 500	Many molecular transitions of key atmospheric species; ideal for atmospheric sounding and other remote sensing applications
Vehicle Radar	150	Autonomous collision avoidance applications; vehicle stylists want smaller sensors provided by 150GHz operation

Best Reported MMIC LNAs

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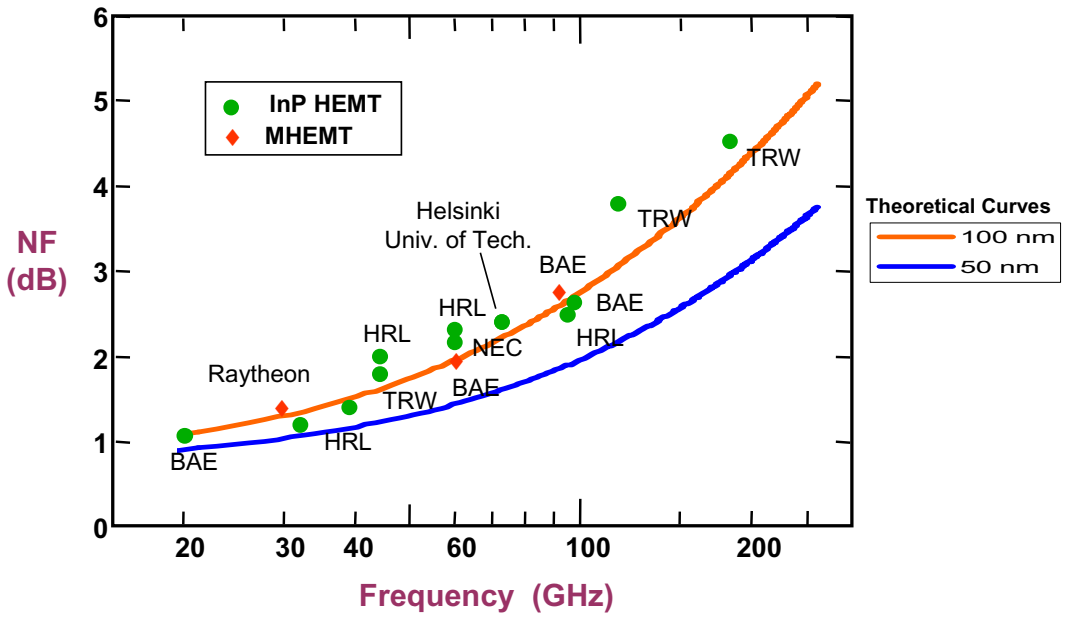

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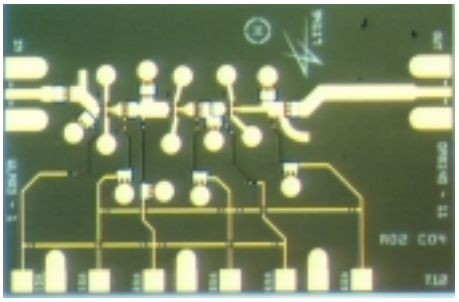
Missile Seeker Radar

- Current radar based Missile Seekers use single T/R Module and twist plate beam steering
- High G force missiles for ABM application need strapped down seekers
- Low cost 140GHz MMICs will enable phased array missile seekers with greatly improved target differentiation capability

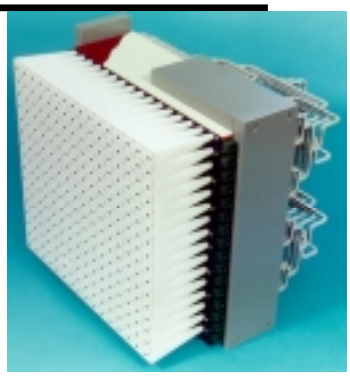


W band LNA MMIC

X-Ray Lithography Impact for Phased Arrays

BAE SYSTEMS

- Military applications of phased array antennas have significant MMIC content
- Large arrays required for spaced based imaging or communications
  - 25,000 elements
  - 300,000 MMICs
- Very low power dissipation LNAs are required reduce array power dissipation
- Low cost sub-100nm gate MMICs will provide the low power dissipation solution for large space based arrays



Prototype Millimeter wave Phased Array

Roadblocks

BAE SYSTEMS

- MMIC industry cannot afford synchrotron installation, need stand alone system
  - Existing point source systems are immature; more work needed to improve throughput, reliability
- Mask availability
  - IBM X-ray mask shop closing
  - 1X masks impede sub-100nm development
  - Phase shift reduction printing attractive but no commercial source for X-ray phase shift masks

Conclusions

BAE SYSTEMS

- Military requirement exists for affordable high performance millimeter wave MMICs for missile seekers
- 50 nm Gate Lengths are required for 160 to 220 GHz operation
- X-ray lithography has potential for producing such MMICs
- More investment is needed to assure availability of masks and to mature existing point source systems

X-Ray Lithography
Helios as the Source

GWYN P. WILLIAMS
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XRL Comparative Costs – 2 years of running

Brookhaven - assume use of VUV ring for $4m/yr
Wisconsin
$10m for 2 steppers
$0.5m for beamlines
$0.5m for management
$2m for cleanroom
Total cost for 2 years $22m

Helios-1 - recommissioning and ops 2 years $14.5m
$10m for 2 steppers
$2m for cleanroom
$0.5m for management
Total cost for 2 years $27m

XRL – Throughput

Synchrotron source ~ one 300 mm wafer / minute
Point source ~ one 300 mm wafer / day

Plus synchrotron reliability is > 95%

Basis for above

Brightness

Assume that we have a 10 watt source.

Z-pinch or laser plasma is into 4π sr

Synchrotron is into 10^{-6} sr

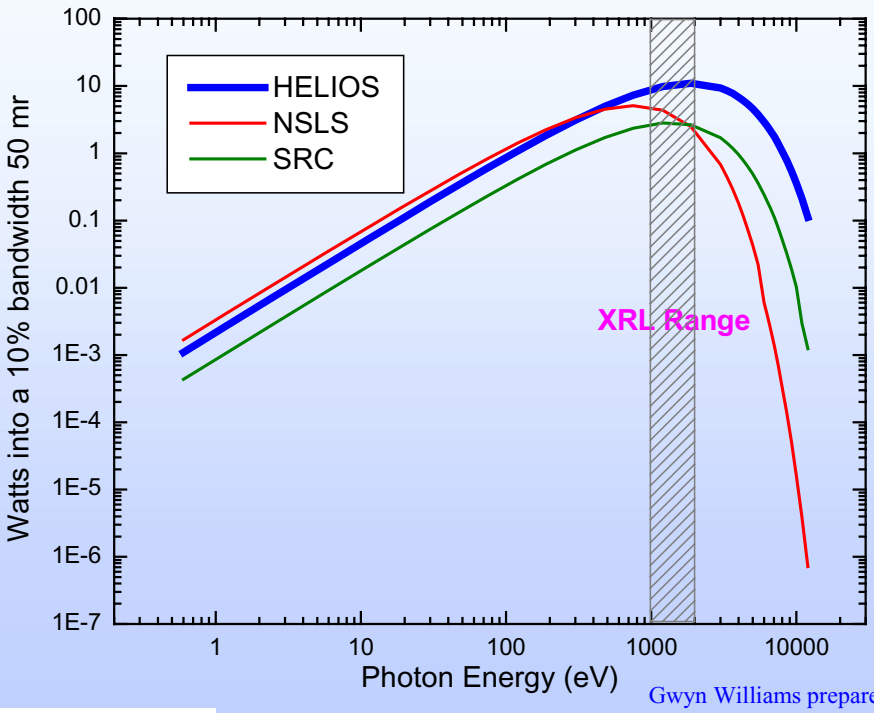
Ratio of $\frac{4\pi}{10^{-6}} \approx 10^7$

7 joules per wafer* means that synchrotron exposes in ~ 4 secs
while point source exposes in ~ 2 days

* assume 300mm wafer, = 707 cm^2 @ 10mJ/cm^2 = 7 joules/wafer

Gwyn Williams prepared for discussion Nov. 4, 2003

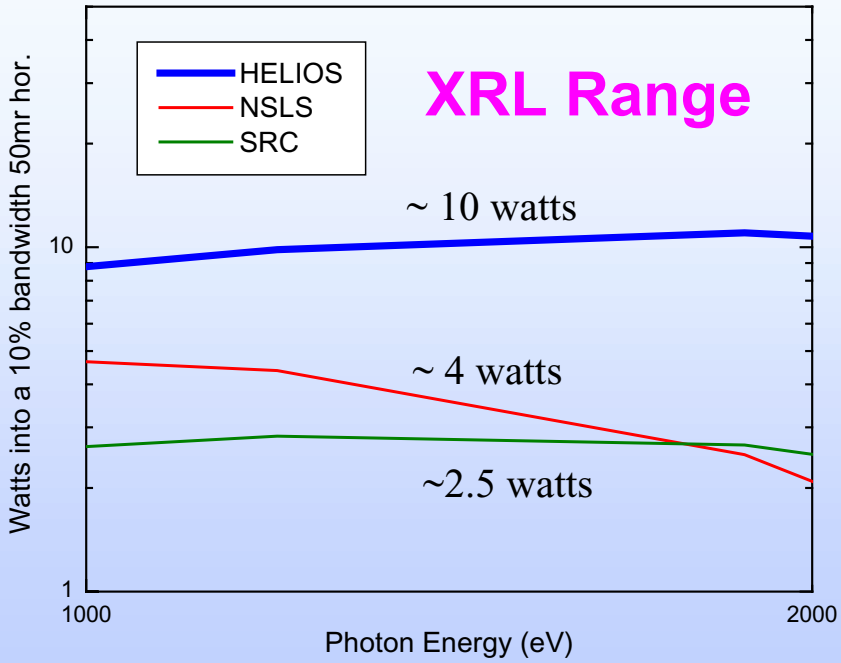
XRL – Synchrotron Power



30 cm wafer
= 707 cm^2
@ 10mJ/cm^2
Exposure time
per wafer = 0.7s
for 10 watts

Gwyn Williams prepared for discussion Nov. 4, 2003

XRL – Synchrotron Power



Gwyn Williams prepared for discussion Nov. 4, 2003

Helios – Recommissioning $$

All loaded numbers, not direct costs.
Re-commissioning: Includes bldg. modification for linac plus 100x100 foot 2 story addition, shielding.

	$K
Modify FEL bldg for injector and power supplies	500
Building addition including utilities	4000
Magnet power supplies and controls	1000
RF power supplies and controls	600
Labor – installation (basis 10 people/10 weeks, rigging)	450
Liquid helium line	200
Re-commissioning (basis 3 people/1 year)	750
Beamlines	500
Project management	500
Contingency	1000
TOTAL	**9,500**

Gwyn Williams prepared for discussion Nov. 4, 2003

Thomas Jefferson National Accelerator Facility
Operated by the Southeastern Universities Research Association for the U.S. Department of Energy
Office of Science U.S. DEPARTMENT OF ENERGY

Helios – Annual Operations $$

All loaded numbers, not direct costs.

	$K
Maintenance and supplies	700
1 Operator 24 x 7 (6 FTE's)	750
Liquid helium	200
Project management	250
Utilities (including low-conductivity water)	100
Contingency	500
TOTAL	**2500**

Gwyn Williams prepared for discussion Nov. 4, 2003