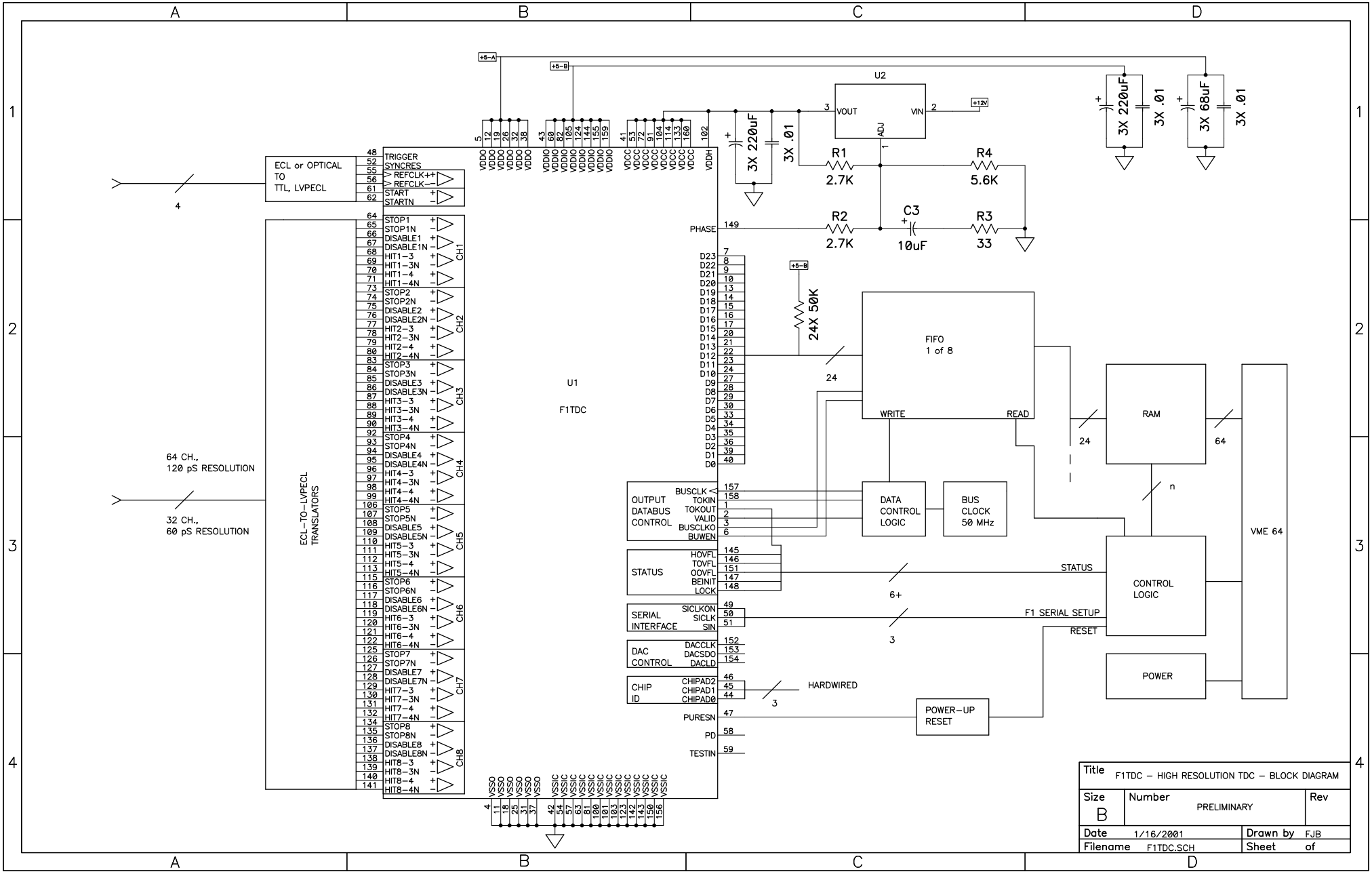
ECL or OPTICAL TO TTL, LVPECL
4
64 CH., 120 pS RESOLUTION
32 CH., 60 pS RESOLUTION
ECL-TO-LVPECL TRANSLATORS
TRIGGER
SYNCRES
REFCLK+
REFCLK-
START
STARTN
STOP1 STOP1N DISABLE1 DISABLE1N HIT1-3 HIT1-3N HIT1-4 HIT1-4N
STOP2 STOP2N DISABLE2 DISABLE2N HIT2-3 HIT2-3N HIT2-4 HIT2-4N
STOP3 STOP3N DISABLE3 DISABLE3N HIT3-3 HIT3-3N HIT3-4 HIT3-4N
STOP4 STOP4N DISABLE4 DISABLE4N HIT4-3 HIT4-3N HIT4-4 HIT4-4N
STOP5 STOP5N DISABLE5 DISABLE5N HIT5-3 HIT5-3N HIT5-4 HIT5-4N
STOP6 STOP6N DISABLE6 DISABLE6N HIT6-3 HIT6-3N HIT6-4 HIT6-4N
STOP7 STOP7N DISABLE7 DISABLE7N HIT7-3 HIT7-3N HIT7-4 HIT7-4N
STOP8 STOP8N DISABLE8 DISABLE8N HIT8-3 HIT8-3N HIT8-4 HIT8-4N
CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8
U1
F1TDC
VDDO VDDIO VDCC VDDH
VSSO VSSIC
+5-A
+5-B
+12V
U2
VOUT VIN ADJ
3X 220uF
3X .01
3X 68uF
R1 2.7K
R2 2.7K
R3 33
R4 5.6K
C3 10uF
PHASE
24X 50K
D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
FIFO 1 of 8
WRITE
READ
24
RAM
64
n
VME 64
OUTPUT DATABUS CONTROL
BUSCLK TOKIN TOKOUT VALID BUSCLKO BUWEN
DATA CONTROL LOGIC
BUS CLOCK 50 MHz
STATUS
HOVFL TOVFL OOVFL BEINIT LOCK
6+
CONTROL LOGIC
SERIAL INTERFACE
SICLKON SICLK SIN
F1 SERIAL SETUP
RESET
3
DAC CONTROL
DACCLK DACSDO DACLD
CHIP ID
CHIPAD2 CHIPAD1 CHIPAD0
HARDWIRED
POWER
PURESN
PD
TESTIN
POWER-UP RESET
Title F1TDC – HIGH RESOLUTION TDC – BLOCK DIAGRAM
Size B
Number PRELIMINARY
Rev
Date 1/16/2001
Drawn by FJB
Filename F1TDC.SCH
Sheet of