New TDC Development at Jefferson Lab
Physics Division
Data Acquisition Group
Fast Electronics Group
June 7, 2001
Motivation:

- LeCroy Fastbus product line discontinued
- Repair and maintenance costs are increasing significantly for Fastbus instrumentation
- Presently no multi-hit high resolution solution

Will need high resolution multi-hit TDC to support the new detectors outlined in the 12 GeV Upgrade Plan

Examples:

- Hall A -- Medium Acceptance Detector
  Drift Chambers
  Hodoscopes
  Calorimeter
- Hall B -- CLAS upgrade
  Central Detector -- Calorimeter, Drift Chamber
  Forward Tracker
  Wire chambers
- Hall C -- SHMS
  Hodoscope Upgrade
  Wire Chambers
  Shower counters
- Hall D (8000 high resolution TDC channels)
  Vertex Chamber/Start counters
  Forward Tracking Chambers
The *F1* TDC Integrated Circuit

- 8 Channel Time to Digital Converter developed for the Compass experiment at CERN
- Versatile design. Can be configured for 4 high resolution channels or 8 low resolution channels per chip
- *F1* developed at CERN to fulfill the time resolution, multi-hit, and event rate requirements for the Compass experiment at CERN. *F1* IC developed with industry partner Acam-messelelectronic gmbh in Germany. Acam produces the *F1* chip as a commercial product.

**F1 chip highlights**

1. Resolution -- Two modes
   - 4 channels--High-resolution 60ps least count.
   - 8 channels--Low-resolution 120ps lease count.
2. Dynamic range -- 16 bits or ~4uS [ High resolution mode ]
3. Double pulse resolution -- 11nS
4. On board Hit buffer size -- 32 hits in high resolution mode
5. On board readout buffer, interface FIFO and trigger count buffer
6. +5.0 V power
7. Hit Inputs can be Low Voltage Differential Standard [LVDS], PECL, TTL
8. 160 pin plastic quad flatpack surface mount device
9. Commercially available from Acam

More *F1* information on the web at:  http://www.acam.de/Content/F1_e.htm
The Jefferson Lab F1 TDC Module

Jefferson Lab -- Physics Division --
Design Team
   Fernando J. Barbosa -- Fast Electronics Group
   Ed A. Jastrzembski -- Data Acquisition Group

Module Overview

64 input channels

   4 front panel connectors. Module will be configured for High-resolution mode (32 channels) or Low-resolution mode (64 channels)
   Inputs will accept standard ECL inputs to be compatible with existing systems at JLAB

Additional buffering of each F1 chip → 32K x 24 bit FIFO

Module memory is 8Mbytes of fast RAM operated as FIFO [ Single VME address ] with 1M x 64-bit organization to exploit the 64-bit transfer mode of VME.

Module will be capable of dual-edge data transfer (2eVME) as defined in the VME64x standard [ Highest data transfer rate ~100Mb/sec ]

Module will support "chain-block" transfer for reading multiple TDC modules within one crate.
Can be used in a Non-VME64x powered card enclosure (crate) with provisions on board to produce required 3.3V power.
# TDC Module Comparison

<table>
<thead>
<tr>
<th></th>
<th>1872/1875</th>
<th>C.A.E.N. V767</th>
<th>JLAB F1 TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module Format</td>
<td>FastBus</td>
<td>VME; VME (CERN 430)</td>
<td>VME; VME64x</td>
</tr>
<tr>
<td>Resolution [LSB]</td>
<td>25ps/50ps/100ps</td>
<td>800ps</td>
<td>60ps/120ps</td>
</tr>
<tr>
<td>Channels/module</td>
<td>64</td>
<td>128</td>
<td>32 Hres/64 Lres</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>12 or 15 bit mode</td>
<td>20 bit</td>
<td>16 bit</td>
</tr>
<tr>
<td>Double pulse resolution</td>
<td>N/A [Single Hit]</td>
<td>10ns</td>
<td>11ns</td>
</tr>
<tr>
<td>Integral non-linearity</td>
<td>&lt; 3 counts</td>
<td>Not specified</td>
<td>&lt;1 count</td>
</tr>
<tr>
<td>Commercially available?</td>
<td>Not anymore</td>
<td>Yes</td>
<td>Soon</td>
</tr>
<tr>
<td>Multihit?</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Local memory?</td>
<td>No. 8 event buffer</td>
<td>Yes; 32K</td>
<td>Yes: 8M (1M x 64bit)</td>
</tr>
</tbody>
</table>
Prototype Schedule

- Draft Specification completed April 2001
- Twenty (20) F1 chips have been purchased and received.
- Front end design in progress
  - Channel assignments
  - ECL input configuration
  - Clock stabilization circuits
- VME interface, memory control, CSR interface, and FIFO logic design in progress
- Schematic capture
- Printed Circuit Board layout optimization
- PCB manufacturing
- Assembly
  - Prototype will be assembled in the Fast Electronics Lab with SMD manufacturing equipment
- **Prototype delivery goal by late Fall 2001**
- Testing will present interesting challenges

Preliminary Cost Estimate [ Prototype quantity of 2 ]

<table>
<thead>
<tr>
<th>Description</th>
<th>Price per Board</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1 TDC Chips (20 chips)</td>
<td>~$100/chip</td>
</tr>
<tr>
<td>Memory, Programmable Logic, FIFOs</td>
<td>$500</td>
</tr>
<tr>
<td>Multilayer Circuit Board Manufacturing</td>
<td>$500</td>
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<tr>
<td>Connectors, passives, front panel, hardware</td>
<td>$300</td>
</tr>
<tr>
<td>Assembly Labor [JLAB]</td>
<td>$1000</td>
</tr>
<tr>
<td>Total</td>
<td>$3100</td>
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</table>