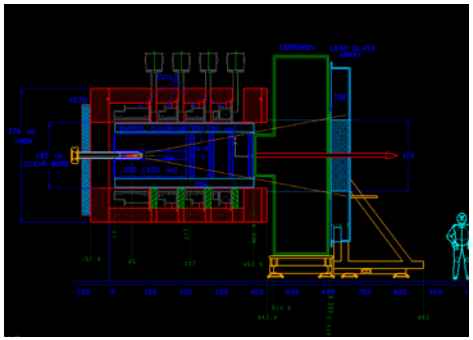
Hall B 12GeV Upgrade Workshop

Jefferson Lab

2-3 February 2007



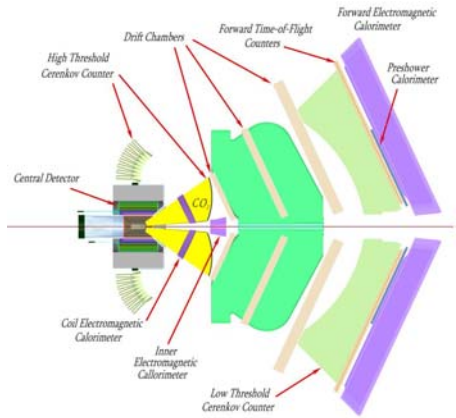
ELECTRONICS for the Upgrade

R. Chris Cuevas

Jefferson Lab

Physics Division

Group Leader -- *Fast* Electronics



Topics:

- Requirements
- Projects and Progress
  - 250Msps Flash ADC
  - Energy Sum Module
- The Bigger Picture
  - DAQ/Electronics Work Plans
  - All Halls using JLAB Electronics
  - Concerns & Issues

DAQ & Trigger Motivation

- New Electronics are a result of new requirements
- These requirements are extracted from Technical Design Reviews and of course direct discussions with Hall Staff.

- To achieve upgrade requirements for increased Trigger rates and DAQ data rates:.
    - Replace FastBus 1881 modules -- Slow conversion [1.2uS]
    - Design ‘pipeline’ front end readout modules that will eliminate delay cable for each channel, and incorporate signal processing features, trigger processing, and event buffering [Flash ADC]
    - Design ADC ‘summing’ system to be used in Level 1 Trigger

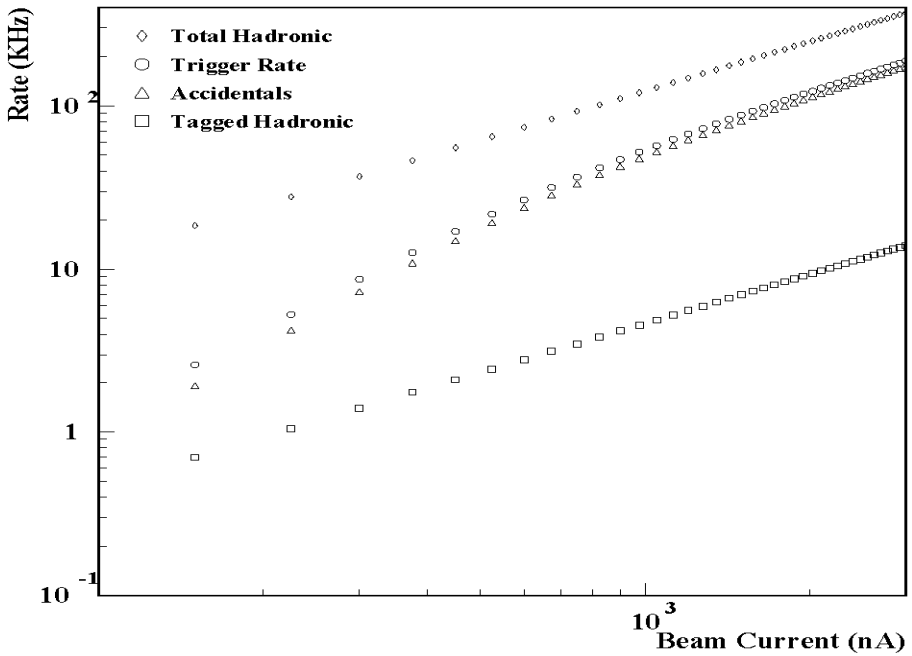


Figure 7.2: Estimated rates as a function of electron beam current. Plotted is the total hadronic rate and the estimated trigger rate, which is the sum of accidental coincidences and the tagged hadronic signal.

CLAS-NOTE
2000-004
Elton Smith

High rate test

Hall D Trigger Rate
>180Khz

Requirements

DAQ & Trigger Motivation

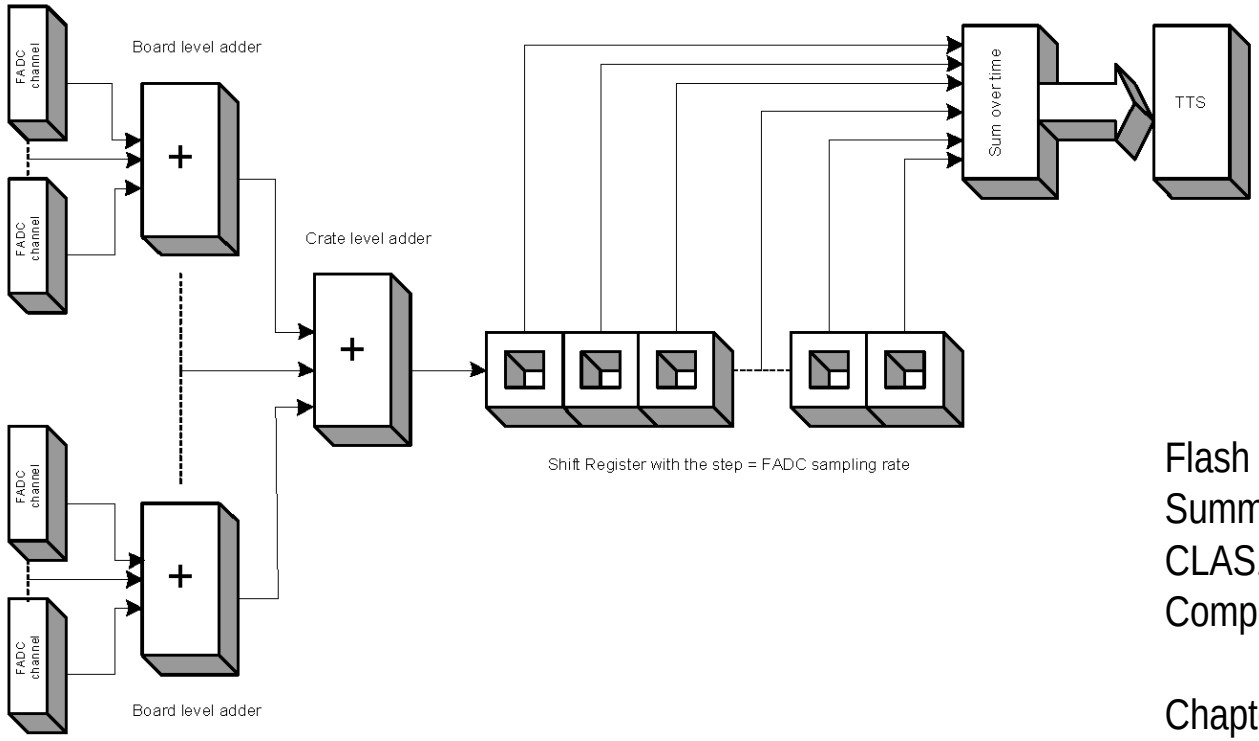


Figure 6.2: Level1 triggering system based on flash ADCs.

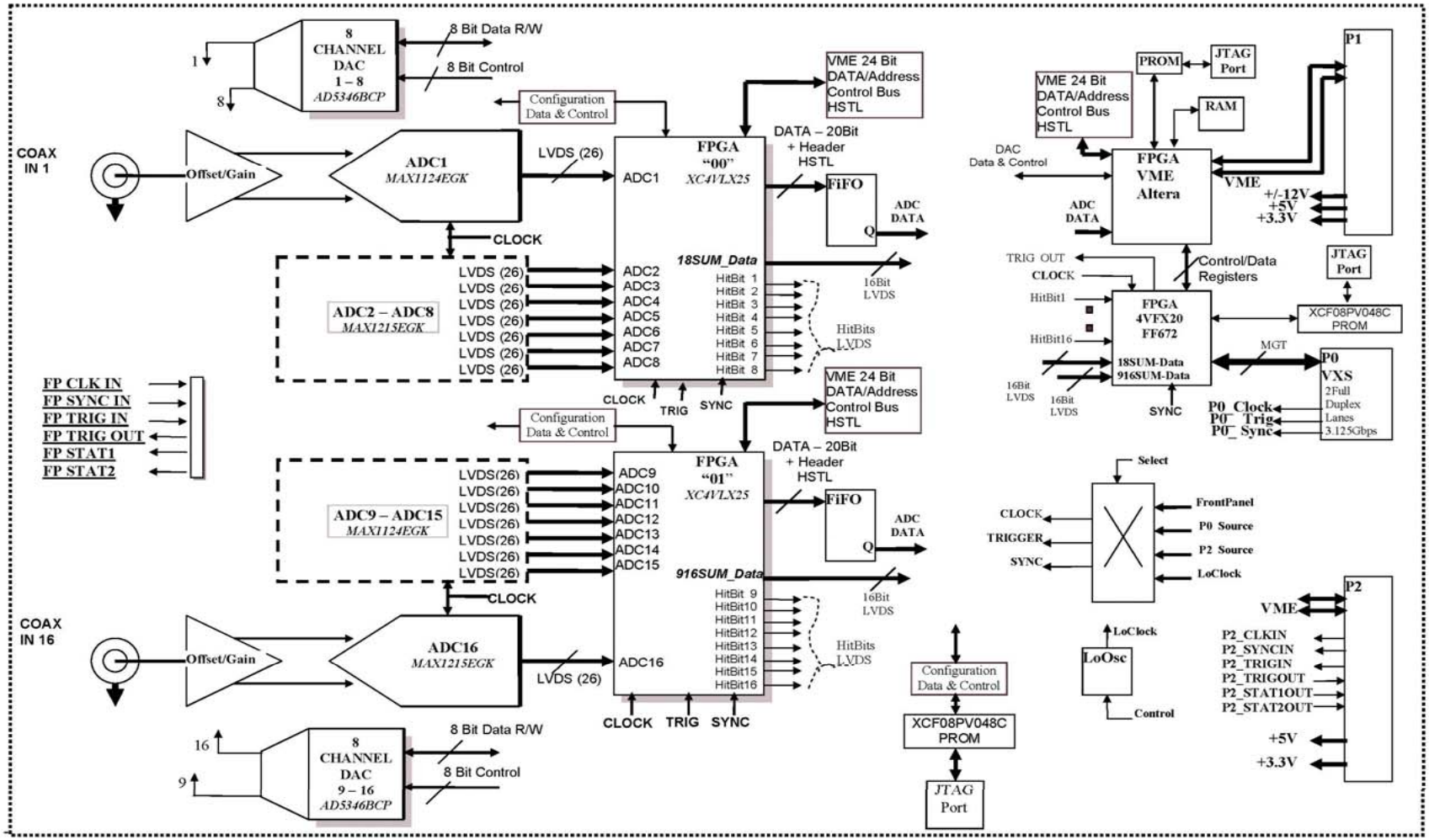
Flash ADC
Summing
CLAS12
Computing Upgrade

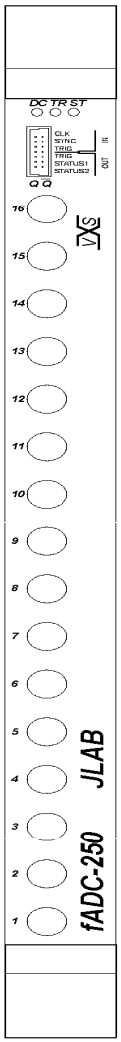
Chapter 6

Requirements

Flash ADC Status - Prototype

- Block Diagram
  This diagram is not intended for extreme details, and has not been updated recently. The diagram shows the important decisions for FPGA selection and other hardware features.
- Schematic
  The Schematic is a tremendous amount of effort and is 47 pages!! Clearly the work of several engineers and designers.
- Printed Circuit Board
  The latest layout is shown on a slide that follows. Power regulators and other power components will be finalized soon and full time work for routing will begin soon.
- Components
  XC4VFX20 parts ordered and received. These parts have all 8 MGT units operational at 3.125Gbps. 10 bit Maxim ADC parts ordered and received. XCLX25 parts have been received. All other parts are stock items and we will purchase enough for two prototype units.


8 CHANNEL DAC 1 – 8 AD5346BCP
8 Bit Data R/W
8 Bit Control
Configuration Data & Control
VME 24 Bit DATA/Address Control Bus HSTL
COAX IN 1
Offset/Gain
ADC1 MAX1124EGK
LVDS (26)
FPGA "00" XC4VLX25
DATA – 20Bit + Header HSTL
FiFO
ADC DATA
CLOCK
ADC2 – ADC8 MAX1215EGK
18SUM_Data
16Bit LVDS
HitBits LVDS
FP CLK IN
FP SYNC IN
FP TRIG IN
FP TRIG OUT
FP STAT1
FP STAT2
TRIG
SYNC
ADC9 – ADC15 MAX1124EGK
FPGA "01" XC4VLX25
916SUM_Data
COAX IN 16
ADC16 MAX1215EGK
8 CHANNEL DAC 9 – 16 AD5346BCP
XCF08PV048C PROM
JTAG Port
PROM
RAM
DAC Data & Control
FPGA VME Altera
VME
+/-12V
+5V
+3.3V
P1
TRIG OUT
Control/Data Registers
HitBit1
HitBit16
FPGA 4VFX20 FF672
18SUM-Data
916SUM-Data
MGT
P0 VXS
2Full Duplex Lanes 3.125Gbps
P0_Clock
P0_Trig
P0_Sync
Select
FrontPanel
P0 Source
P2 Source
LoClock
TRIGGER
LoOsc
Control
P2
P2_CLKIN
P2_SYNCIN
P2_TRIGIN
P2_TRIGOUT
P2_STAT1OUT
P2_STAT2OUT



fADC250

VME64x Flash ADC Module Specifications

Signal Inputs	Number	16 S Version (50 Ohm, LEMO)*
	Range	-0.5V, -1V & -2V. User Selectable
	Offset	±10% FS per channel via DACs
Clock	Sampling	250 MSPS, Differential
	Jitter	1 pS (10-bit ADC), 350 fS (12-bit ADC)
	Source	Internal and External
Control Inputs/Outputs	Clock	IN – Diff., LVPECL (Front Panel & Backplane)
	Trigger	IN, OUT - Differential (Front Panel & Backplane)
	Status 1	OUT – Differential (Front Panel & Backplane)
	Status 2	OUT – Differential (Front Panel & Backplane)
	Sync	OUT – Differential (Front Panel & Backplane)
	Trigger SW	Software Strobe (Internal)
Conversion Characteristics	Resolution	10-bit (8 and 12-bit by chip replacement)
	INL	± 0.8 LSB
	DNL	± 0.5 LSB
	SNR	56.8 dB @ 100 MHz Input
	Data Latency	32 nS
Trigger Latency	8 µS	
Data Memory	8 µS	
Data Processing	Sparcification Windowing Charge, Pedestal, Peak Time (Over Threshold, Relative to trigger) Output (Backplane, VXS)	
Interface	VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320 MB/sec) with VXS-P0	
Packaging	6U VME64x	
Power	+3.3V, +5V, +12V, -12V	

FJE JLAB FADC_SPEC.DOC

ADC FPGA Functional Description

The ADC FPGA receives streaming 12 bits data at 250 MHz from 8 ADC. It performs **Channel Data Processing** for each ADC, computes **Energy Sum** of all ADC, and generates **Acceptance Pulse** for each ADC. The data selected in Channel Data Processing and results of Energy Sum are passed to VME FPGA and Hit Sum FPGA respectively for further processing.

1. Channel Data Processing:

ADC Data

Trigger Input

Time Line

|←Programmable Trigger Window→|
-------- 100nS to 2uS ----------

|←----------Programmable Latency (100nS to 8uS ----------→ |

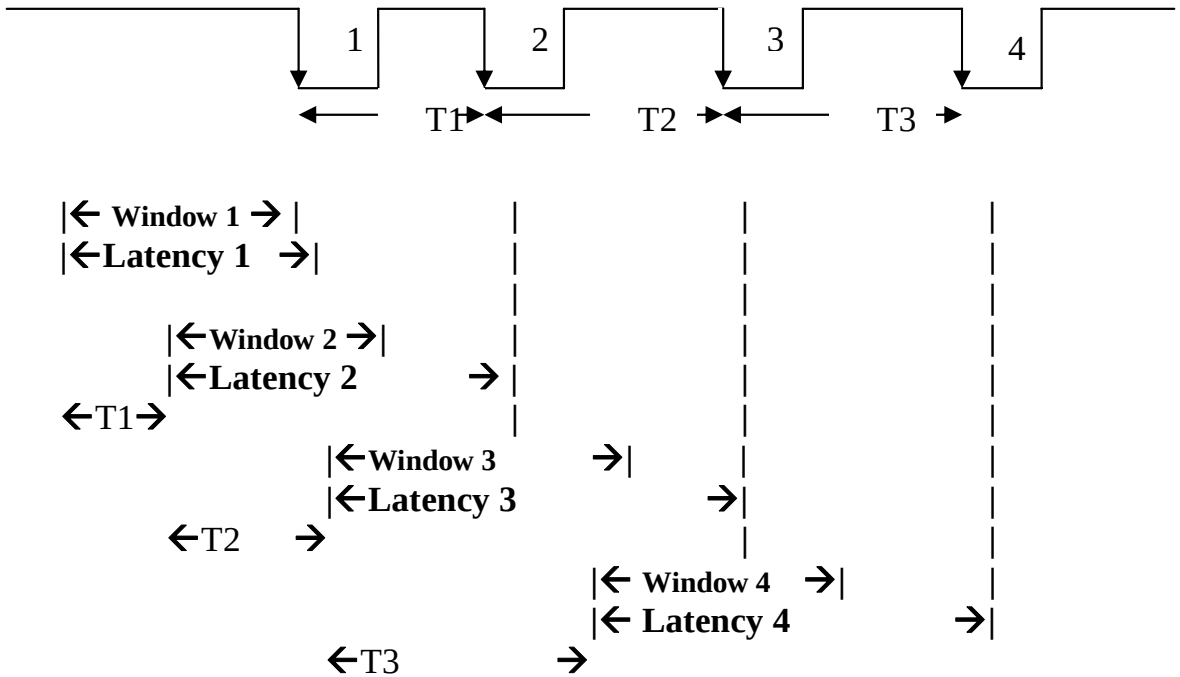
Data from ADC are stored continuously in circular buffer until Trigger input becomes active (low). The data that was stored from the time that the Trigger occurs back to the time specified by Programmable Latency within the Programmable Trigger Window are processed. There are three options to which these data are processed. The options are selectable by the user. **While data are being processed, ADC FPGA will continue storing incoming ADC data with no loss of data.**

4 Data Readout 'Options' Available

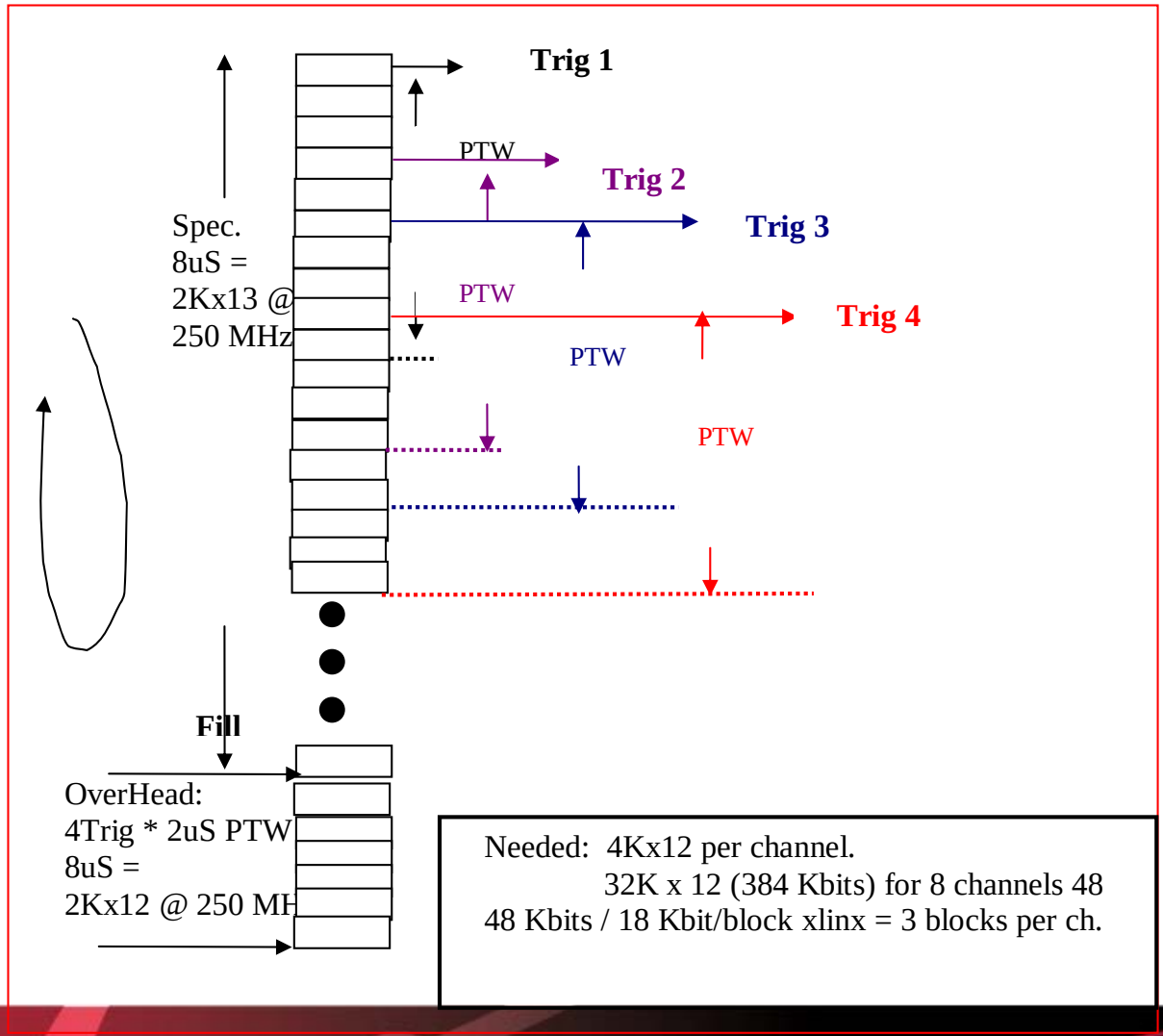
Trigger Input Buffer:

In the event that the Trigger Input rate is faster than the data processing time, the processing algorithm has to be able to process 4 (or more. TBD due to memory limitation) consecutives triggers with no loss in time lines. If a trigger cannot be processed due to an overflow condition, the VME FPGA will be notified: “no data for trigger”. The format is TBD.
Minimum T1 is 50 nS (less will be loss).

Successive Trigger Input Illustration:



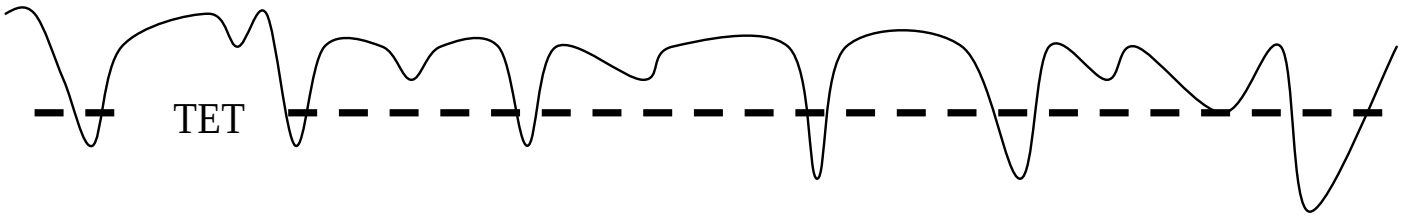
Memory Model for Successive Trigger Input Illustration:



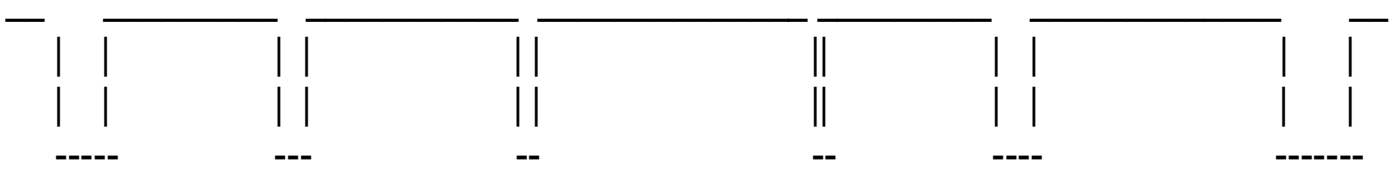
Needed: 4Kx12 per channel.
32K x 12 (384 Kbits) for 8 channels 48
48 Kbits / 18 Kbit/block xlinx = 3 blocks per ch.

Acceptance Pulse Illustration:

ADC data



Hit Bit



Additional feature is the energy sum for all 16 input channels

The energy sum value is continuously updated ever 4ns

Jefferson Lab

Thomas Jefferson National Accelerator Facility

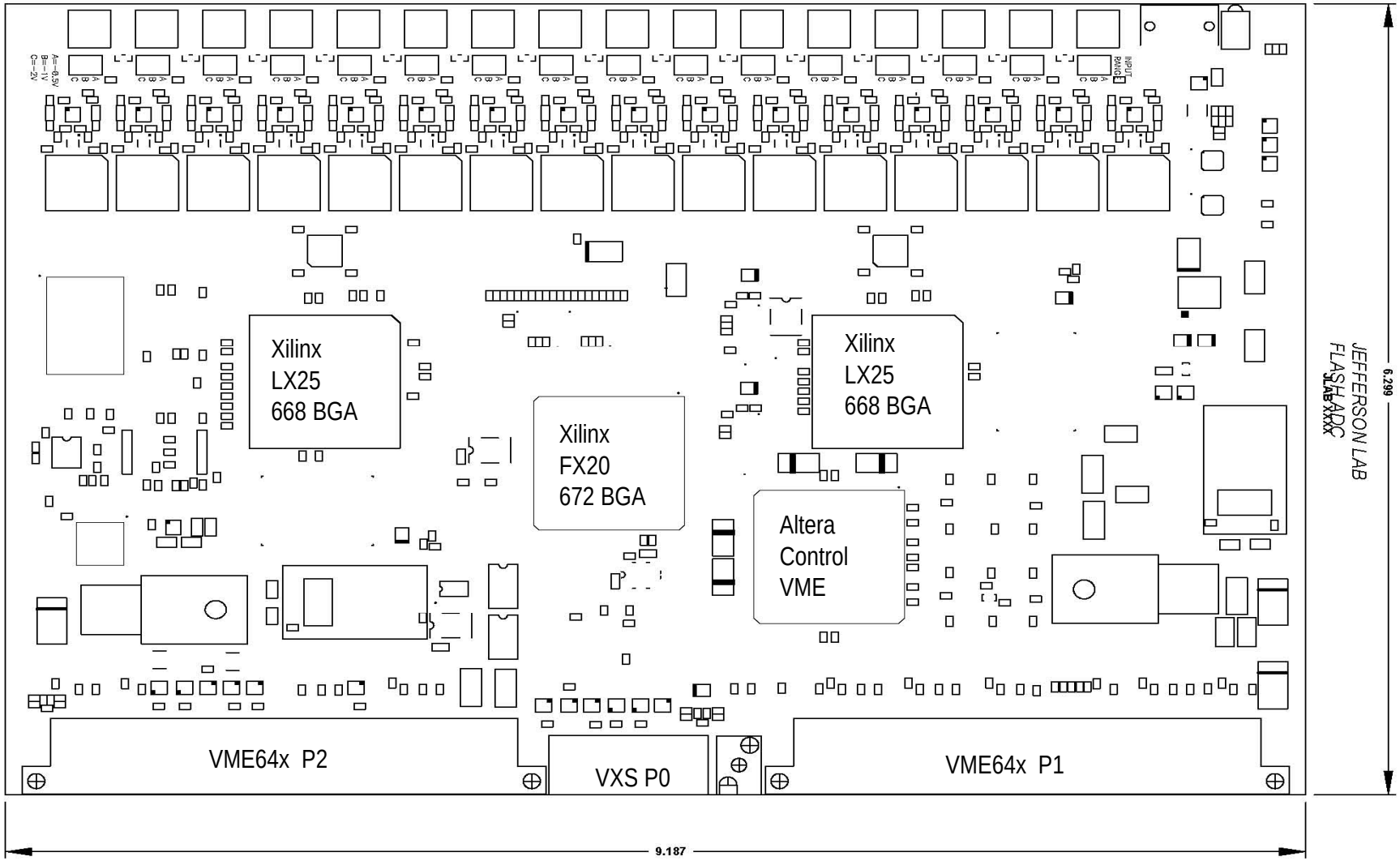
NEWPORT NEWS, VIRGINIA

UNITED STATES DEPARTMENT OF ENERGY

FLASH ADC

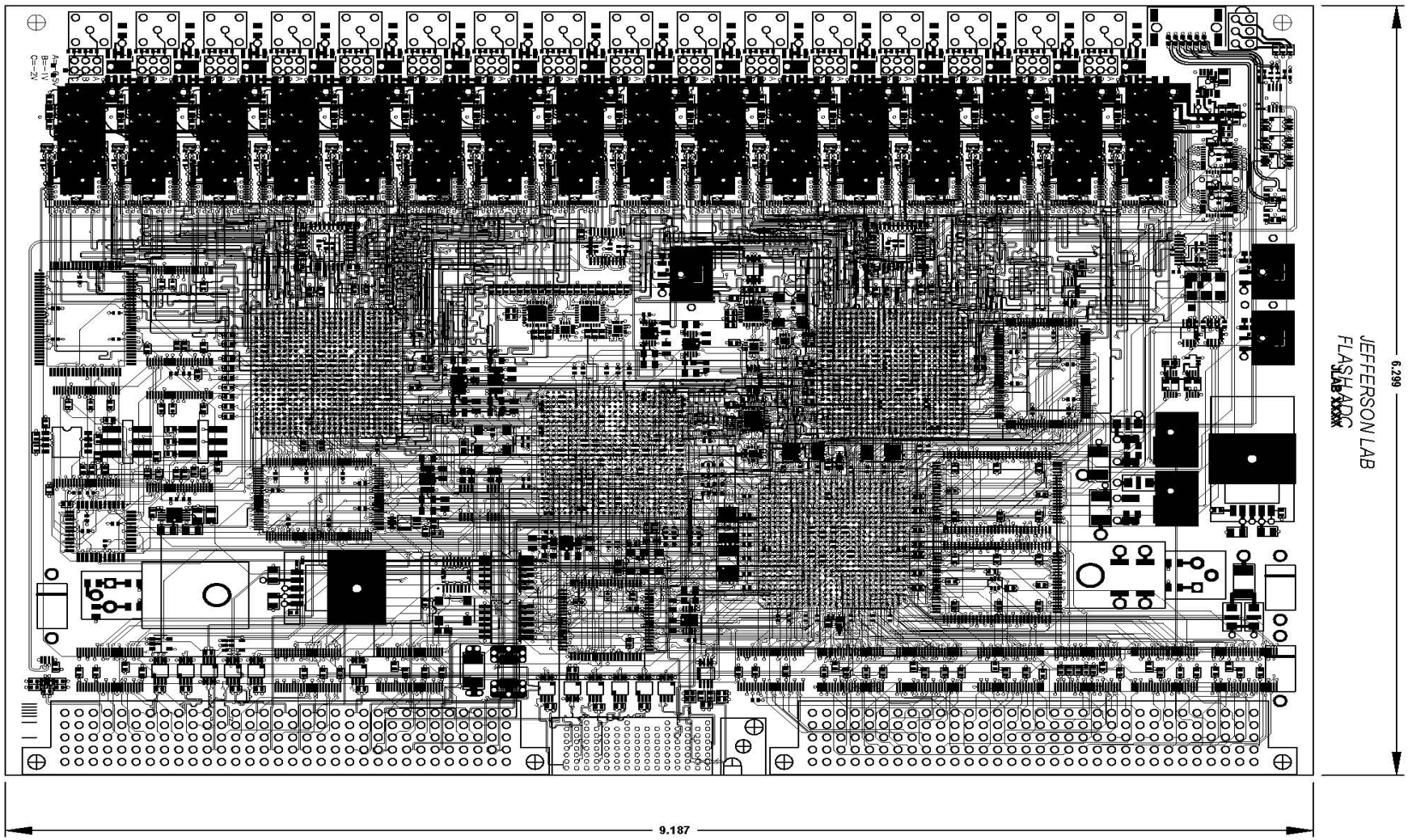
FJB,EJ,HD,JW 6/23/06

MADE IN THE U.S.A.



14 Layer circuit board
Power/GND layers not shown
ENORMOUS AMOUNT OF WORK!

Jefferson Lab
Thomas Jefferson National Accelerator Facility
NEWPORT NEWS, VIRGINIA
UNITED STATES DEPARTMENT OF ENERGY
FLASH ADC
FJB,EJ,HD,JW 6/23/06
MADE IN THE U.S.A.



Flash ADC Development Milestones

- This module is a very challenging design and the progress is remarkable, given that the design team members are committed to other projects also.

➢ October 2006 -- Design Complete [Schematic reviewed]

➢November ‘06 - February 2007 – Final layout/Routing/Review/Order

➢March 2007 – June 2007 INTENSE TESTING! This will include software development work for Coda ‘Drivers’ and Test Station.

➢Summer 2007 – Production modules,, “How many would you like to order?”

Energy SUM Module Development

- The prototype module is assembled and initial testing is complete. The design engineer left the lab in August, and the work focus has been on the Flash ADC, but FPGA code design for the sum module has recently been tested.

- The energy sum prototype module will allow us to continue the research necessary to gain expertise with the new VXS, { VME with serial extensions} technology.

- We have purchased the necessary test instruments for measuring the MultiGigabit Transceivers, and have evaluated several VXS crates from different manufacturers.

Quick VXS Review

Why VXS?

VXS provides an infrastructure for multi-GBps switched serial technologies to compete and grow on top of VME

Expected to extend the life of VME for decades

- Part of the VME Renaissance

Pro's

- Very high bandwidth
- Low latency
- Increased scalability (as compared to a bus architecture)
- Less contention (as compared to a bus architecture)
- Experiment with switched serial under the safety of the parallel bus
- Migrate from parallel bus to serial switched at one's own pace
- Provides a platform for high availability systems – hot swap

Flash ADC, Energy Sum & VXS

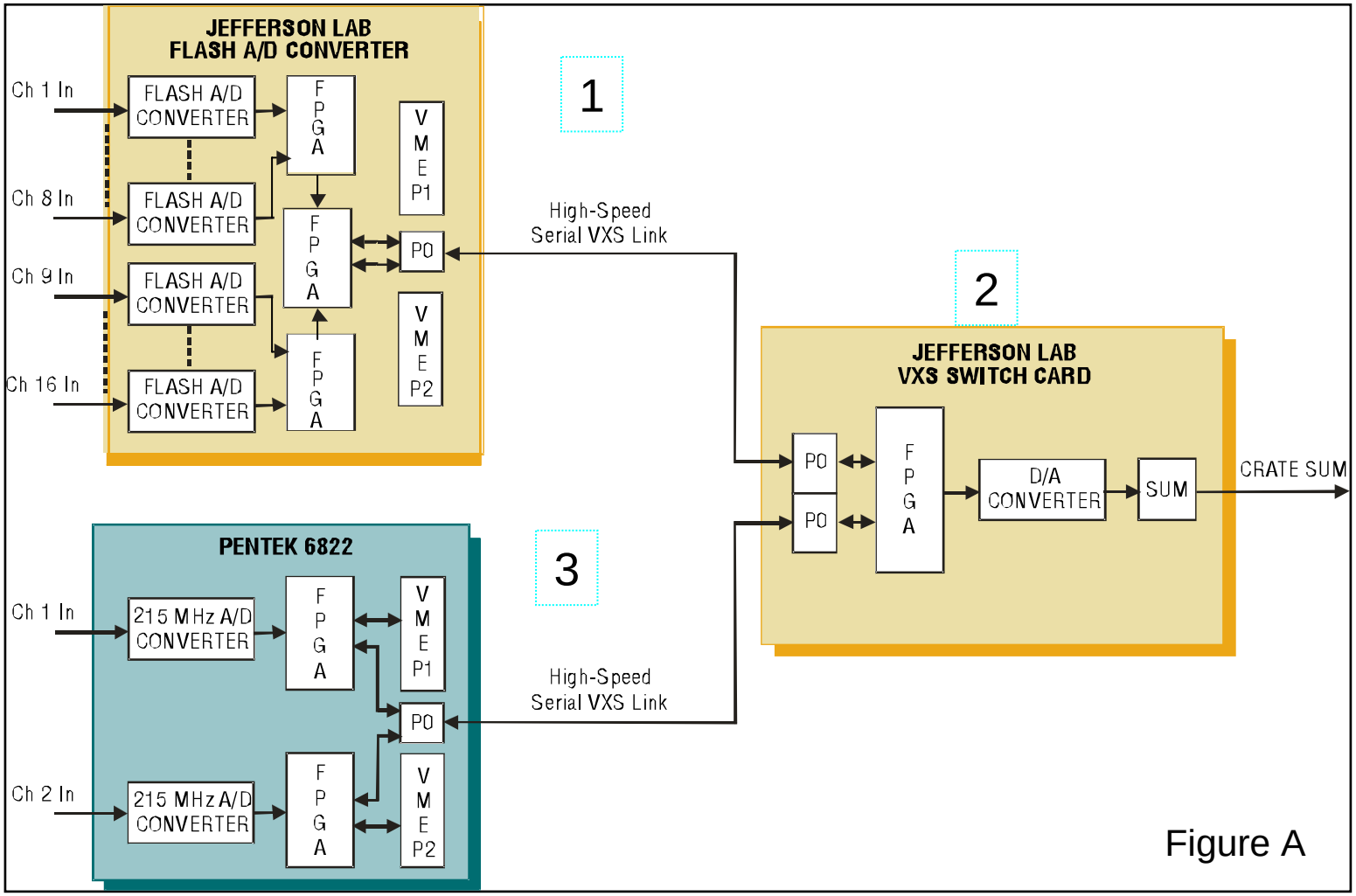
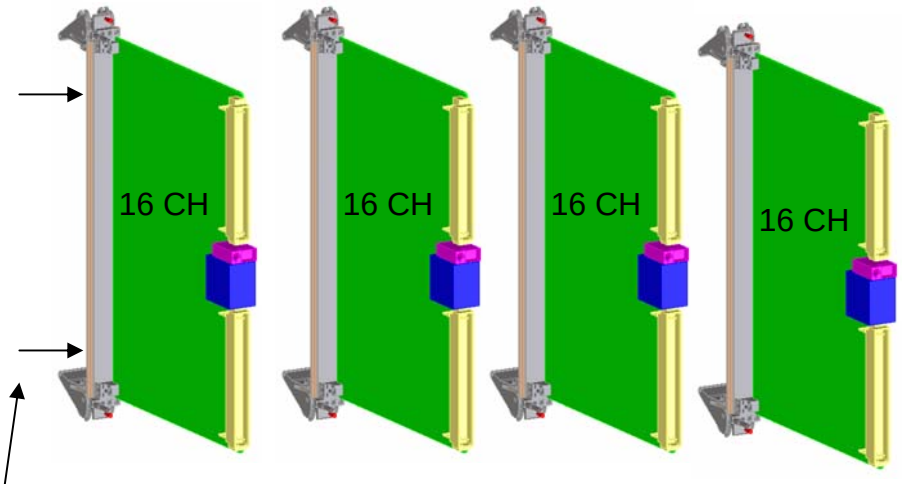


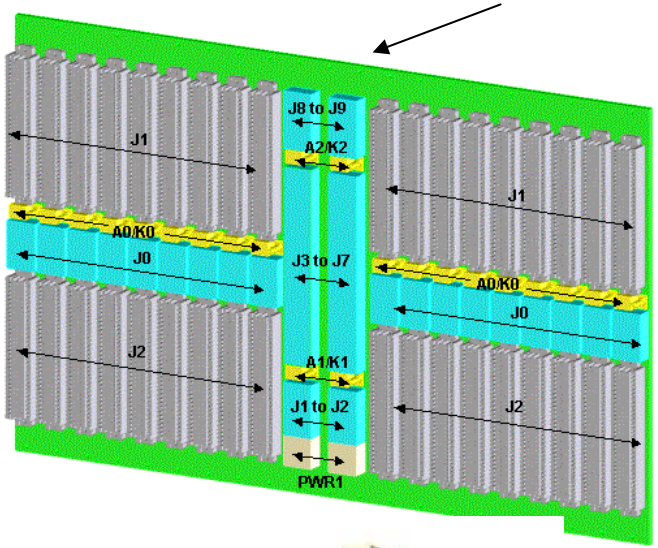
Figure A

Quick VXS Review

VXS “Payloads”
(Jlab fADC)



VXS Backplane

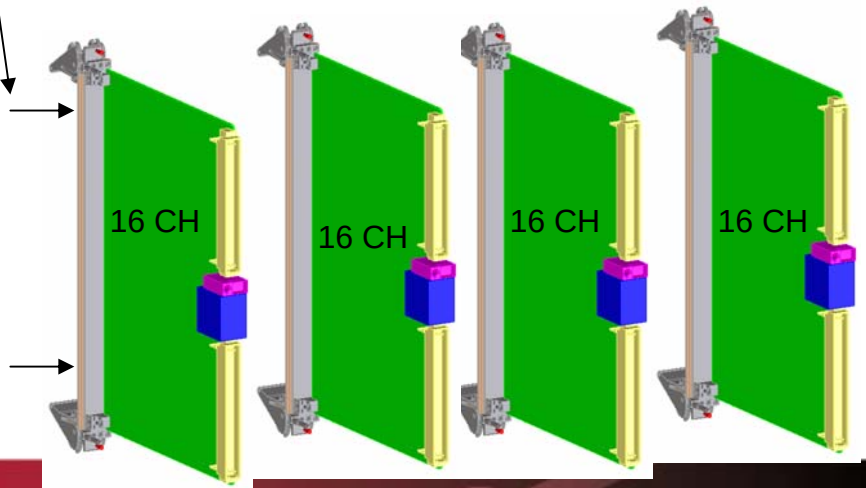


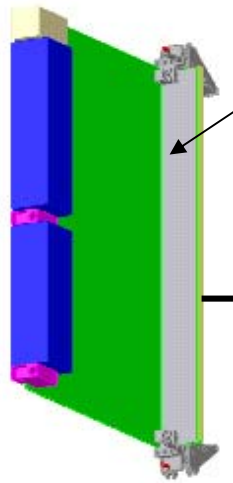
VME64

High Speed Serial

VME64

Detector Signals

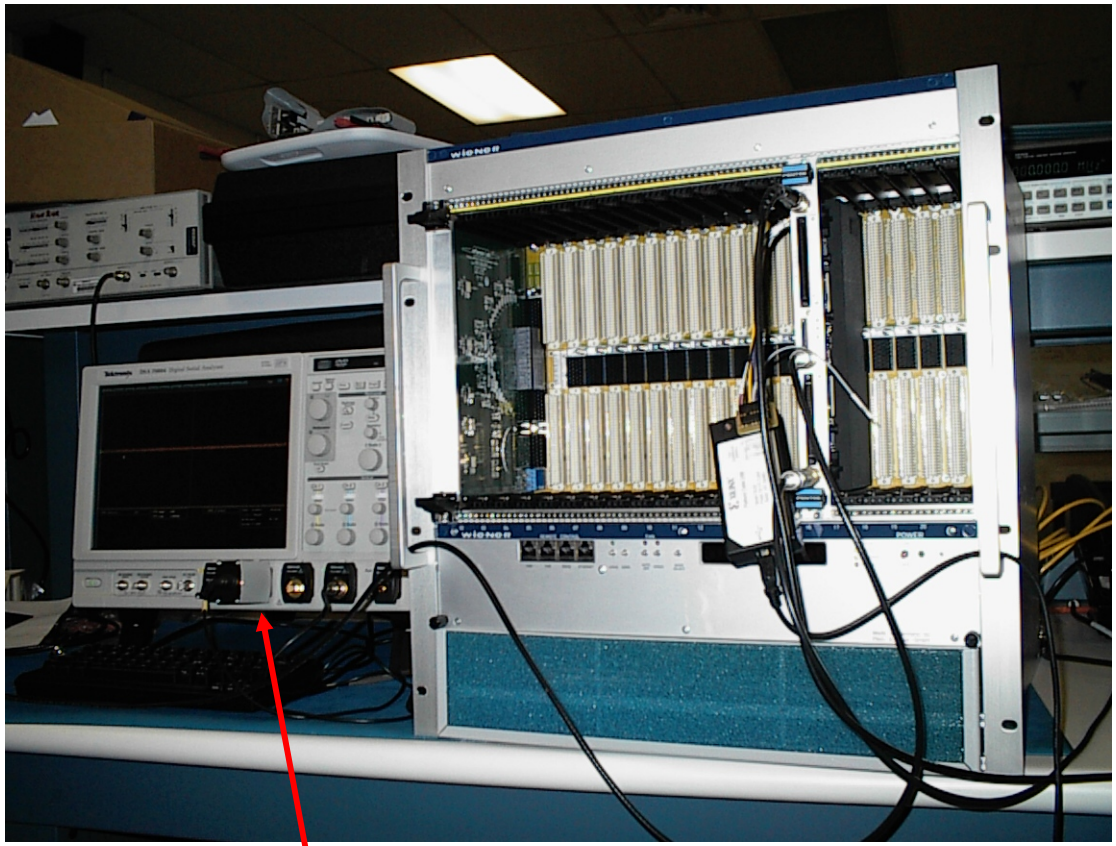




VXS “Switch” Card (Jlab Energy Sum)

Crate Sum to Trigger

More VXS Fun



21 Slot VXS crate
Manufactured by
Wiener Plein & Baus

The absolute latest
In high speed serial
Analysis with digital
Oscilloscope technology
Was delivered in Sept!

Tektronix DSA 70000 8Ghz BW Digital Serial Analyzer

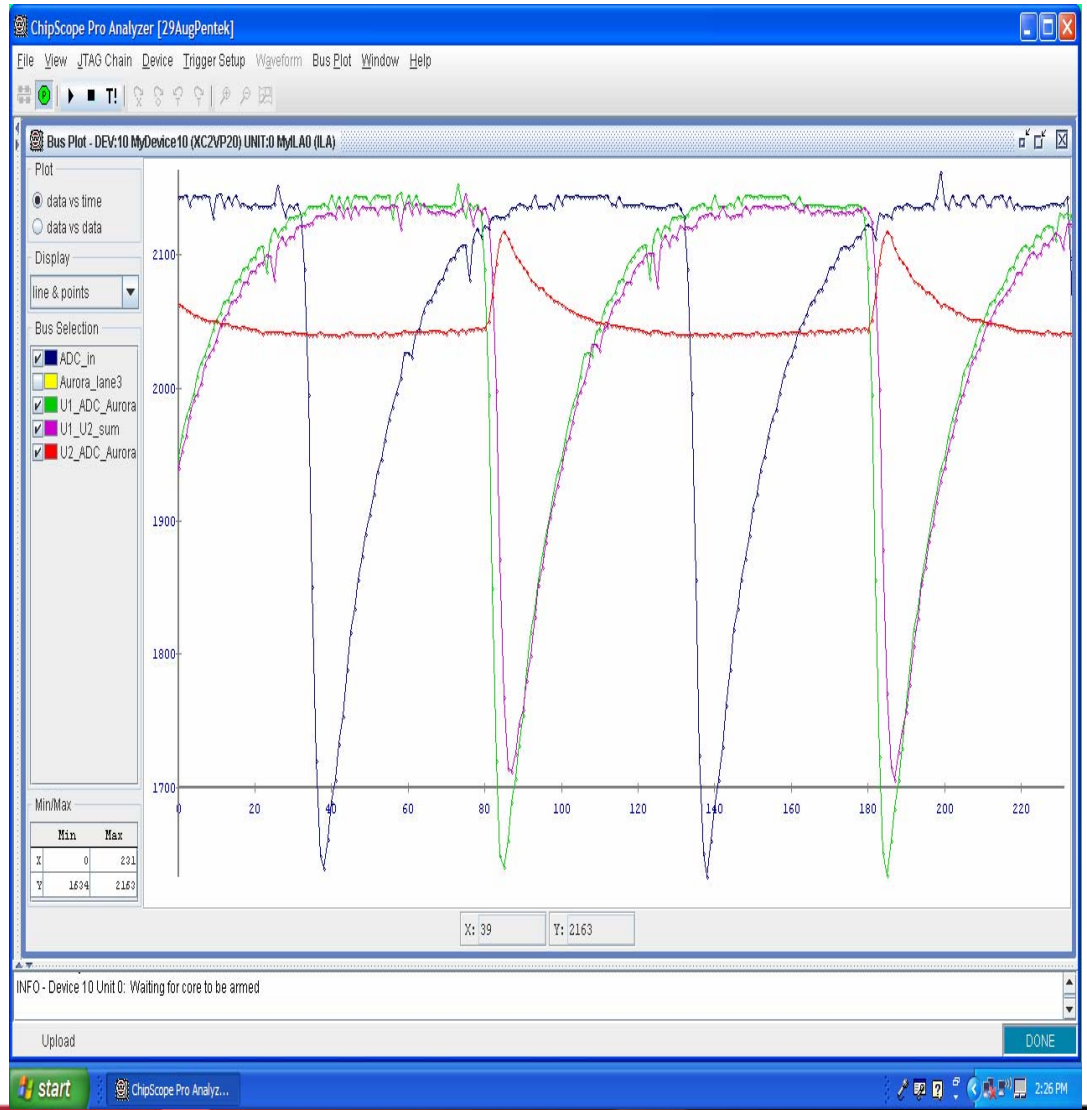


Figure 3: VXS Loopback Waveform results (Xilinx ChipScope Pro)

Test Conditions:

Input ADC1: BLUE → Negative exponential pulse

Input ADC2: RED → Negative exponential pulse; Inverted and attenuated (14db)

1Mhz Input Frequency for both inputs

Output ADC1_Aurora: GREEN → Data transmitted round trip for ADC1

Output ADC1_ADC2_SUM: MAGENTA → ADC1 + ADC2 result transmitted round trip

Conclusion:

The backplane functions correctly for the given payload assignment. Four high speed serial 'lanes' are used at 2Gbps for an aggregate transfer rate of 8Gbps. The Aurora protocol appears to have a latency of approximately 400ns roundtrip, but the proper summing function occurs without error and is extremely stable.

Further testing with the Pentek module is planned to achieve the maximum serial transfer rating of the Xilinx VirtexII Pro FPGA. The Jlab switch slot design will allow the testing of two Jlab flash ADC prototype modules and the Pentek module.

The Bigger Picture

- DAQ & Electronics Work Plans
- All Halls using JLAB Electronics
- Concerns & Issues

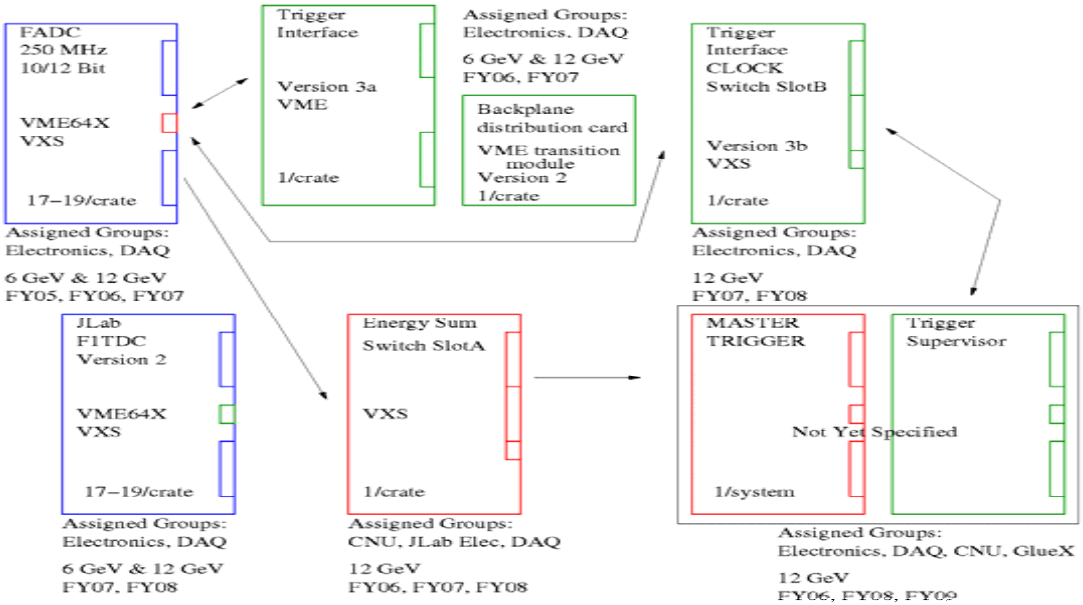


Figure 1: Schematic of the electronic boards that are required to support the plans for GlueX pipeline electronics and data acquisition. Indicated are the module classifications, responsible groups, expected use in the 6 or 12GeV program, and estimate of time frame for design and prototyping.

*Note: Two Xilinx development Modules received for CNU to Prototype and test crate summing Information to Master Trigger

~ Discussion ~

- Upgrade requirements demand increase in performance of existing DAQ/Front-End Electronics
- We are in a decent position to develop the required instrumentation modules to replace aging and obsolete modules. (F1TDC replaces 1872, FlashADC replaces 1881 and analog summing)
- Designs for new ‘pipeline’ trigger interface modules are in close collaboration with the DAQ/Coda group

- Concerns & Issues

- New technology, New test equipment, More firmware (Fpga), More power per module, Software design,,,
- The *elusive* final requirements document. Maybe a better idea is to form working groups for these custom designs,,
- Manpower
- Money