Update on DAQ for 12 GeV Hall C

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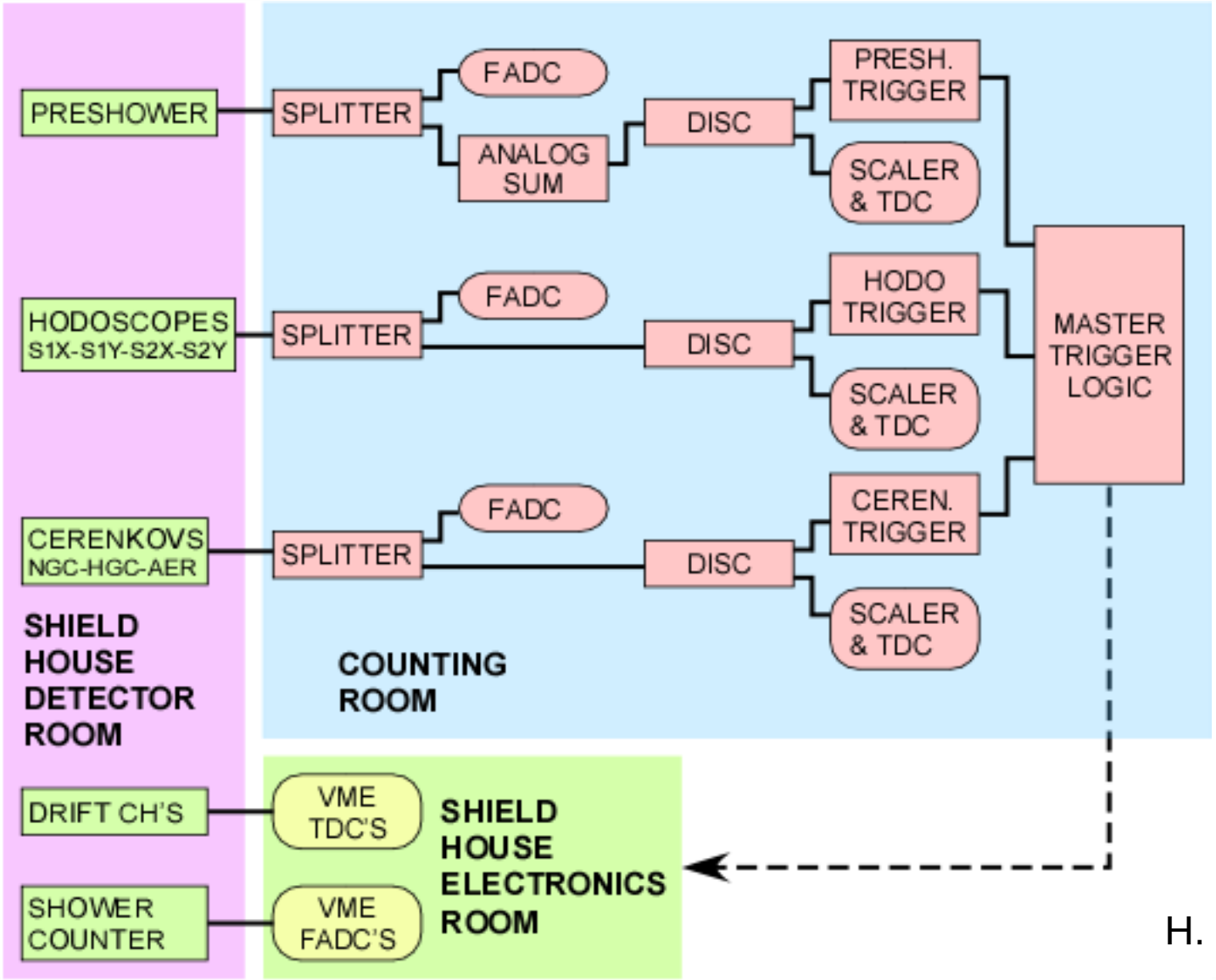
Hall C Winter User Group Meeting
Jan 22, 2018

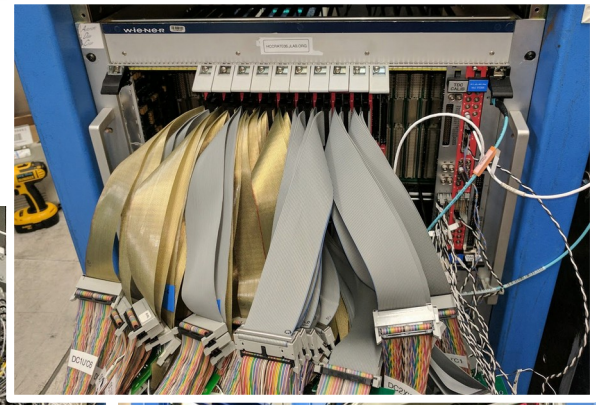
SHMS/HMS Trigger/Electronics

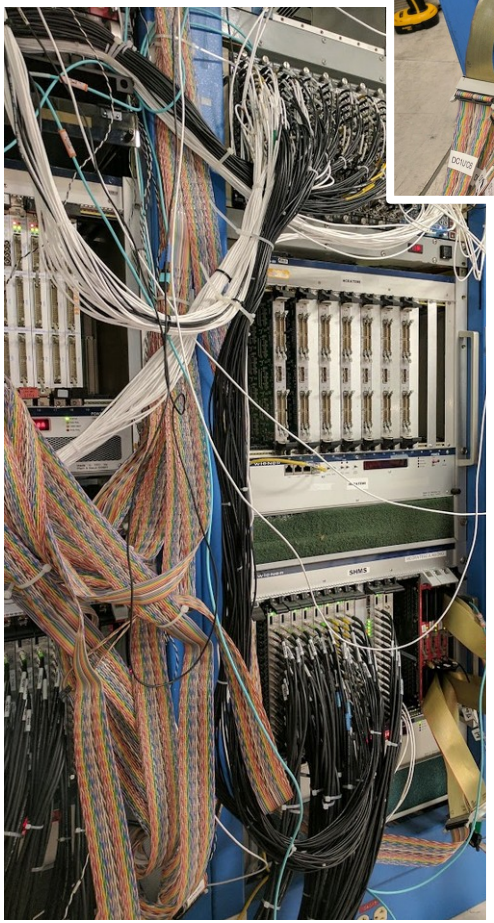


H. Fenker

SHMS & HMS DAQs Operational

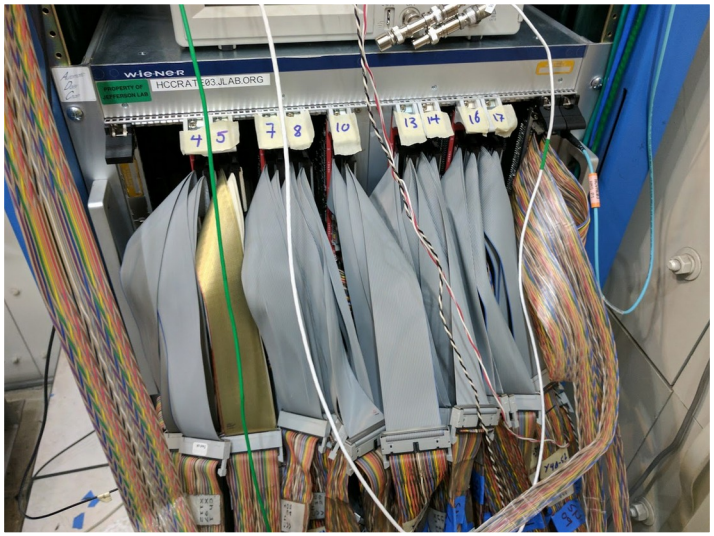
- **SHMS**
  - → ROC2: CH
    - » Hodoscopes
    - » Cerenkov Detectors
    - » Misc. Signals
  - → ROC4: SHMS hut
    - » Shower + Preshower
  - → ROC6: SHMS hut
    - » Drift chambers
  - → ROC8: CH
    - » Hardware scalers

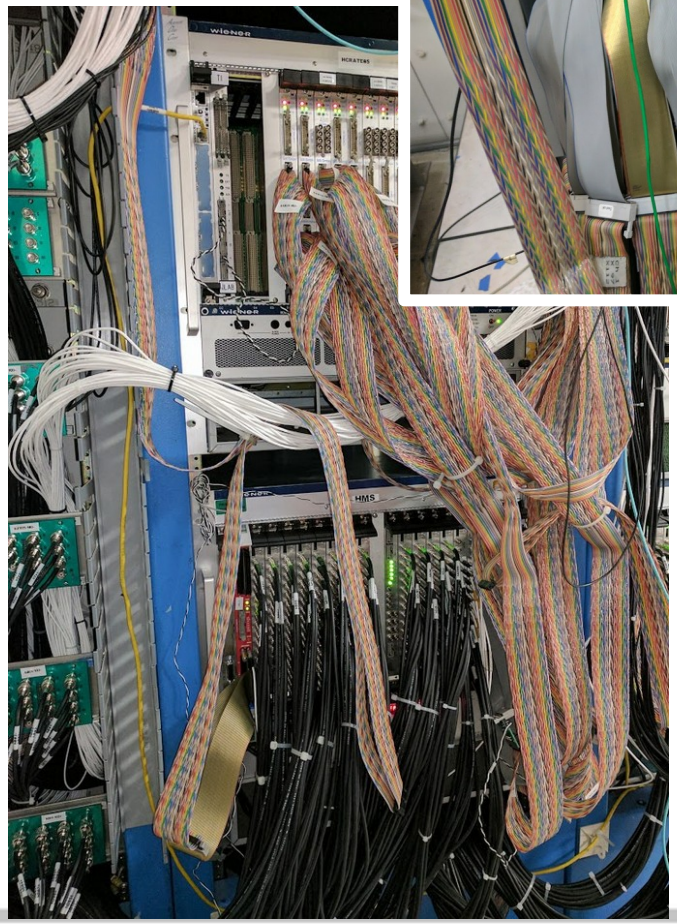




SHMS & HMS DAQs Operational

- **HMS**
  - → ROC1: CH
    - » Hodoscopes
    - » Calorimeter
    - » Cerenkov Detectors
    - » Misc. Signals
  - → ROC3: HMS hut
    - » Drift chambers
  - → ROC5: CH
    - » Hardware scalers





SHMS / HMS Triggers

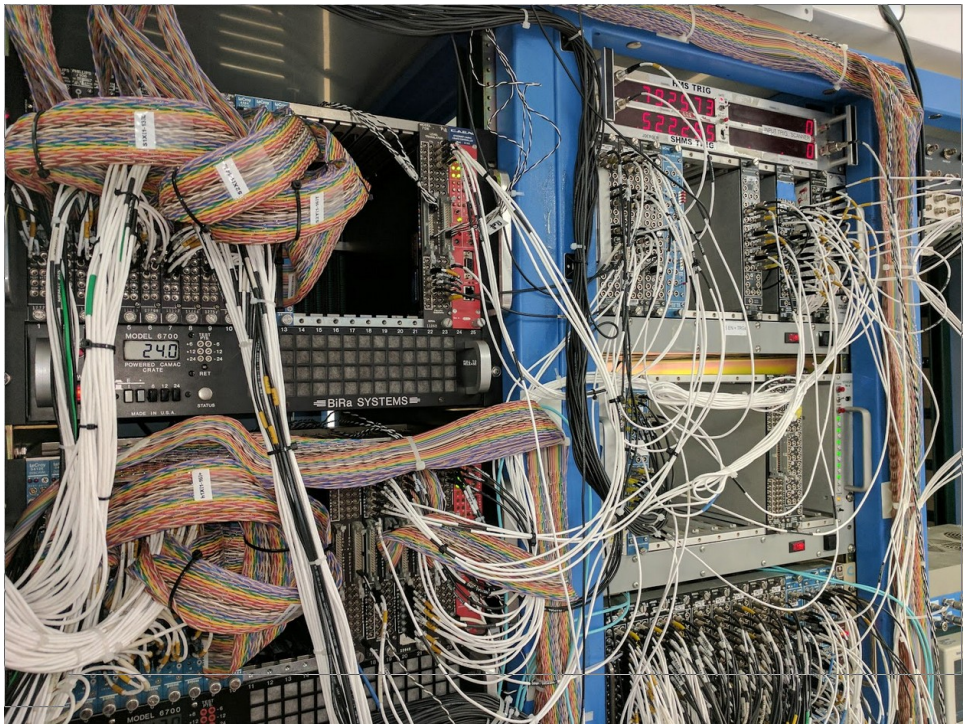
- S{1,2} = S_x .and. S_y
- CER = Cerenkov
- STOF = S1 .and. S2

- SCIN = 3/4 { S1x, S1y, S2x, S2y }

- EL-Hi = SCIN .and. PSh_Hi
- EL-Lo = 2/3{SCIN, STOF,PSH_Lo} .and. CER

- EL-Real = EL-Hi .or. EL-Lo
- EL-Clean = EL-Hi .and. EL-Lo

- Pulser/Random trigger
  - → EDTM injection for deadtime monitoring, synth. coin. trig

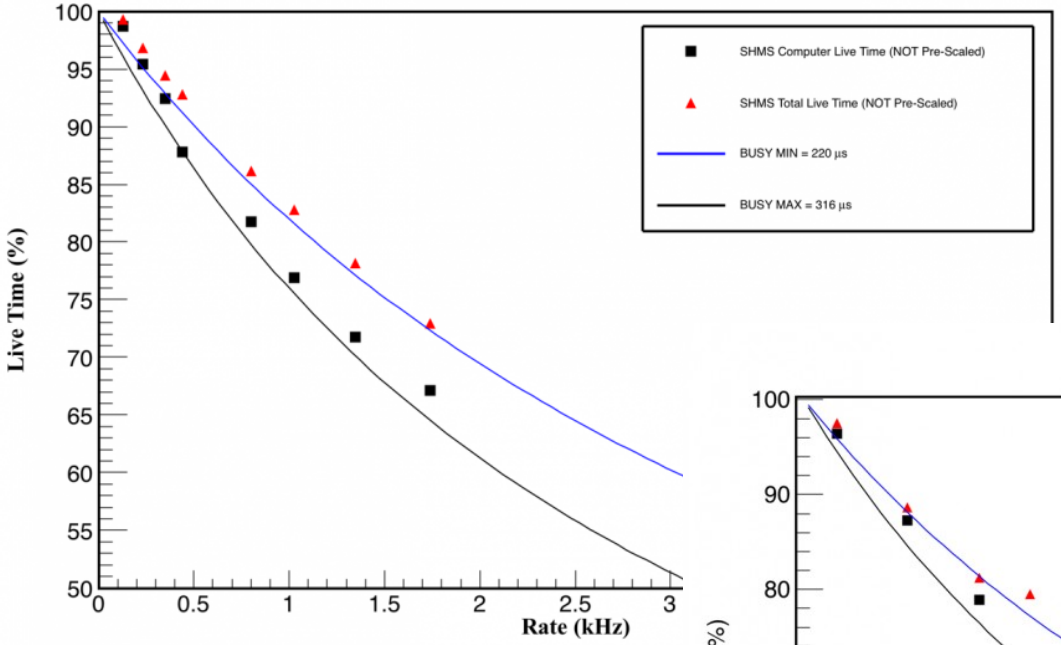


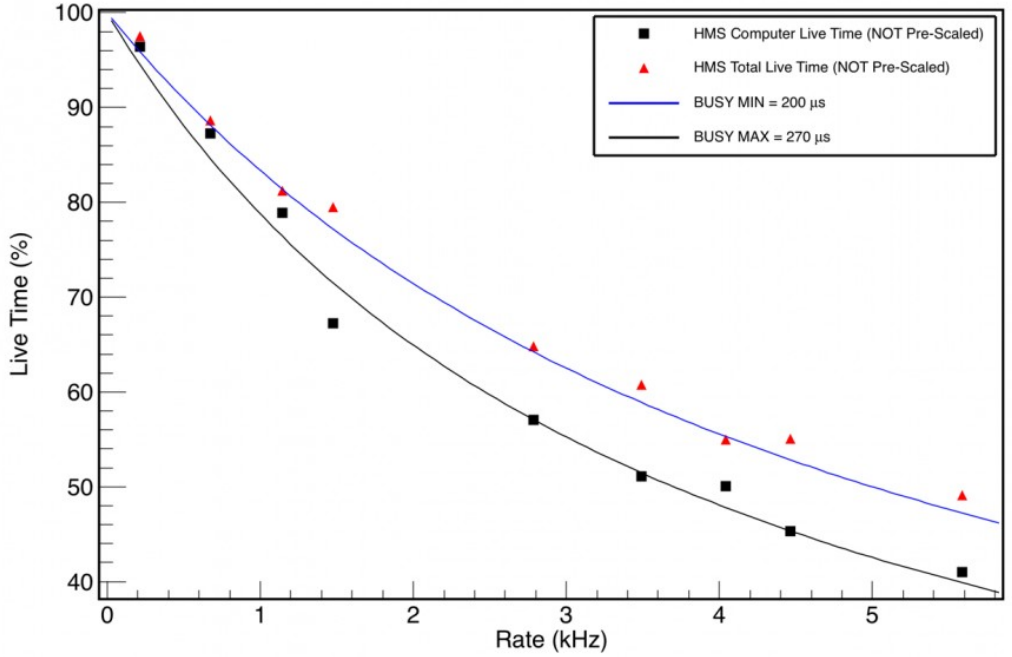
- Each arm has its own Trigger Master (behaves like a TS)
  - → Both coincidence and independent/parallel-arm operation available
- We use TM module for trigger prescaling
- NOTE: There is *no* Calorimeter Sum for SHMS trigger
  - → SHMS Pre-Sh sum *does* exist

Basic Performance Seems Good

- Trigger efficiencies
  - → All hodoscope planes working well
  - → Efficiency > 99% for electrons for all triggers
- PID studies
  - → Cerenkov and Pre-Shower/Shower cuts working well
  - → PID triggers seem clean
- DAQ Deadtimes
  - → As expected for ‘ROC-lock’ readout mode
  - → ~ 70% live at 2 kHz accept rate
    - » We can do better – will try optimizing this week
- DAQ stability has been good

Livetimes vs. Model





Slides from C. Yero

New terms for the 12 GeV DAQ

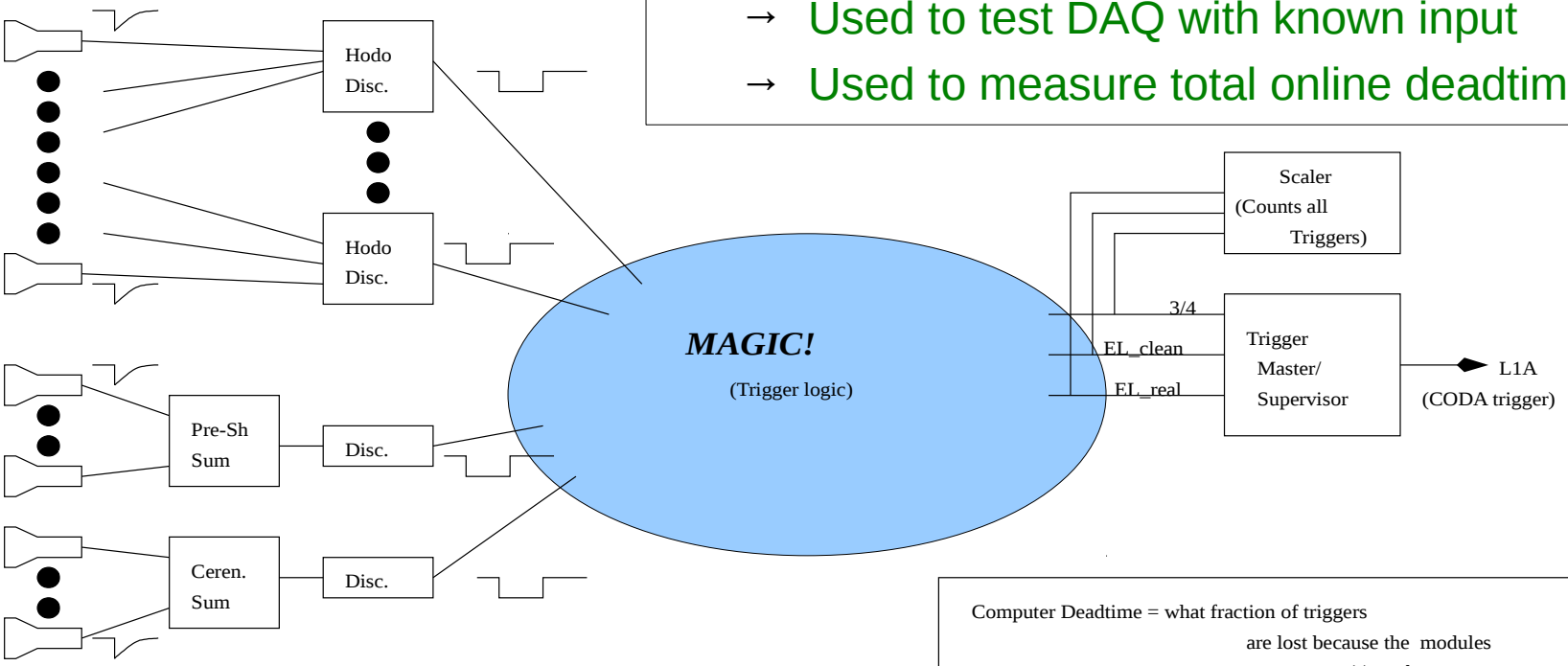
- "EDTM"
  - → Electronic DeadTime Monitoring/Measurement

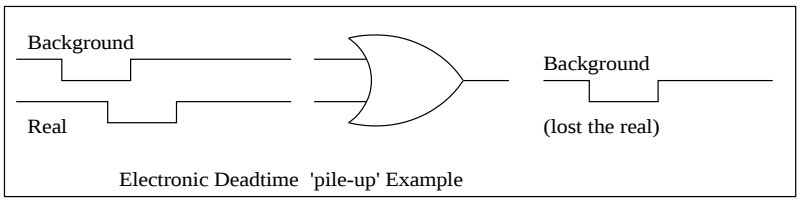
- "Reference Time"
  - → Associated with modern TDCs (CAEN 1190/1290) and Timing from JLab FADCs

EDTM System

Simple DAQ Sketch (no EDTM)

- EDTM = Electronic DeadTime Measurement/Monitor
  - → 'Synthetic' trigger under our control
  - → Used to test DAQ with known input
  - → Used to measure total online deadtime





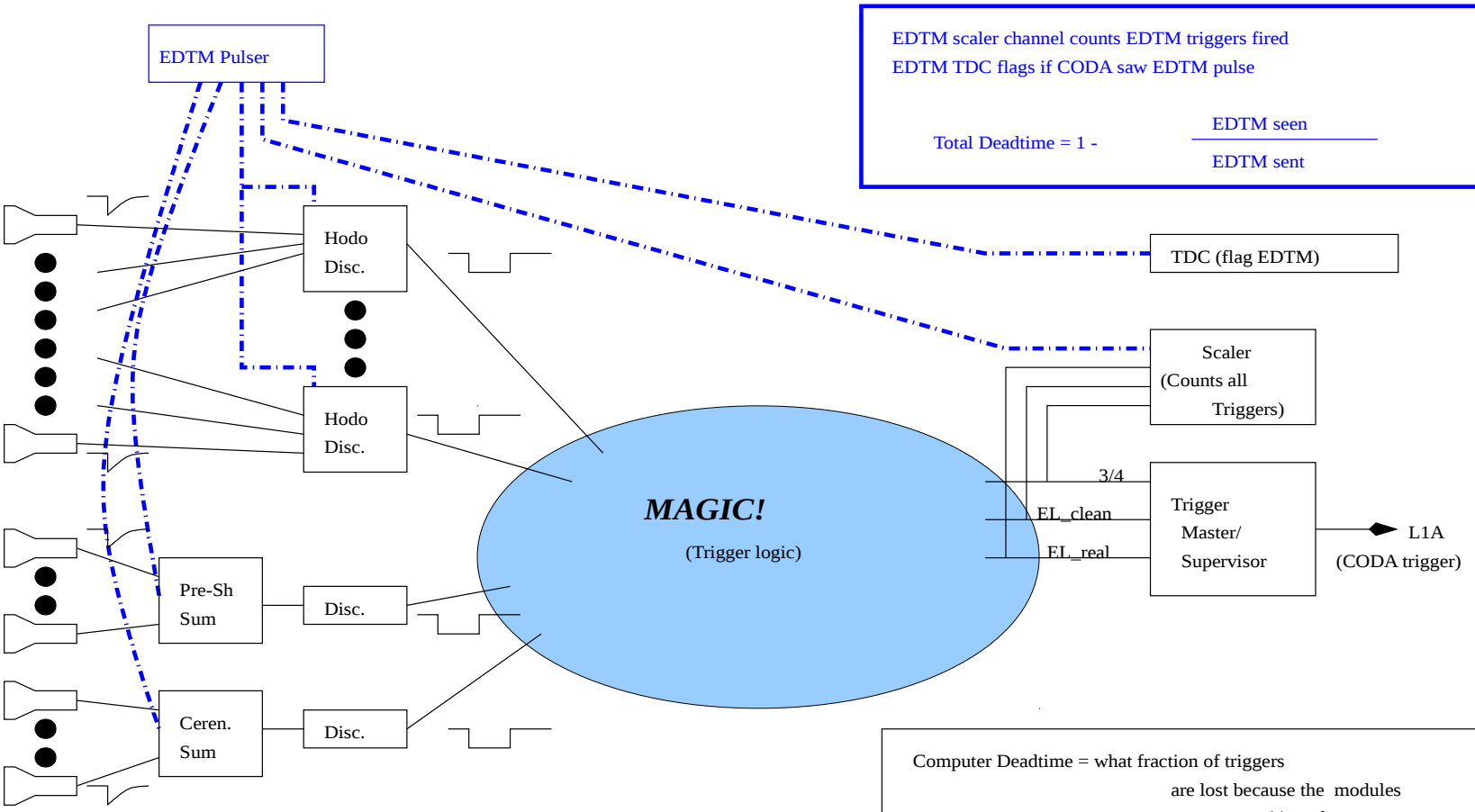
Electronic Deadtime 'pile-up' Example

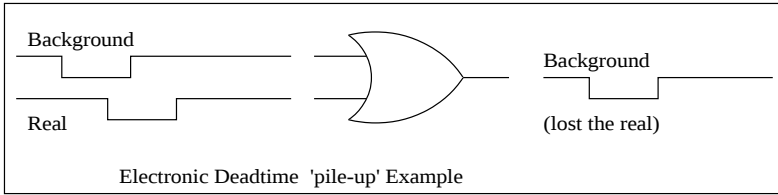
Computer Deadtime = what fraction of triggers are lost because the modules or computer(s) are busy.

Electronic Deadtime = what fraction of triggers are lost due to pile-up in trigger logic.

Total Deadtime is combination of these.

EDTM System





Computer Deadtime = what fraction of triggers are lost because the modules or computer(s) are busy.

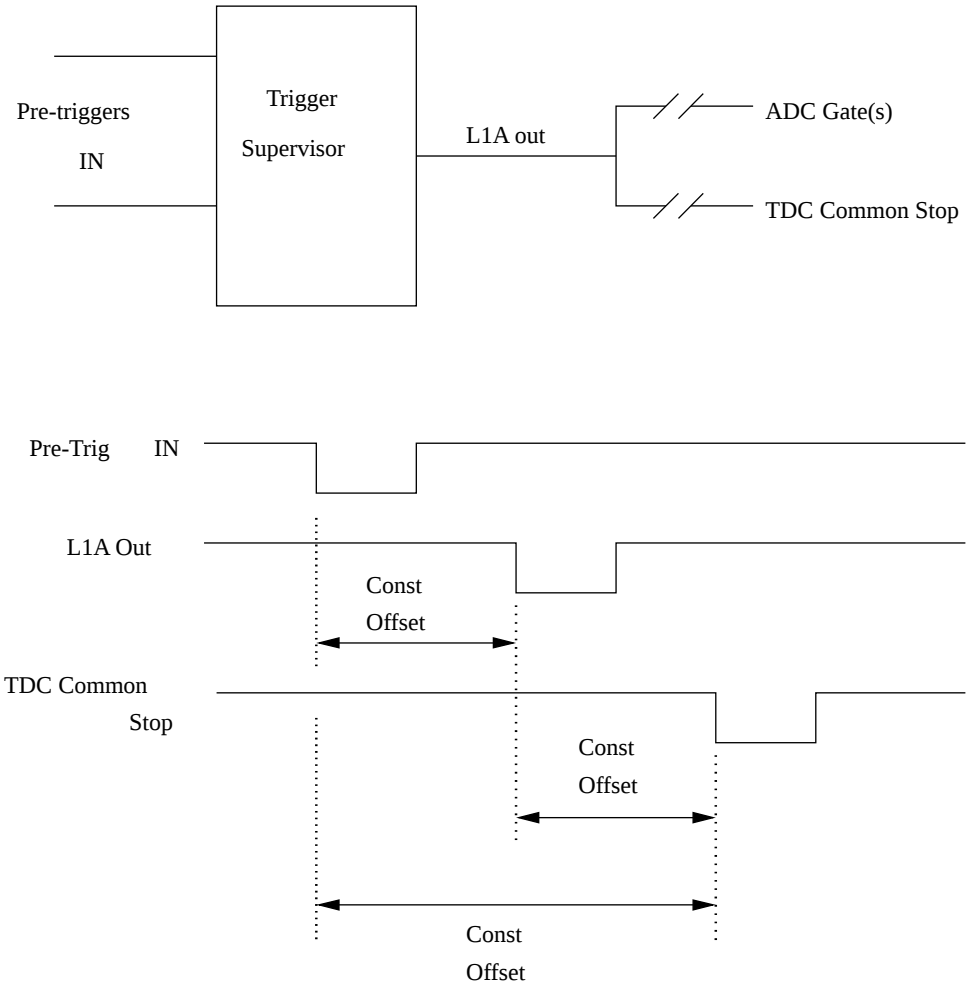
Electronic Deadtime = what fraction of triggers are lost due to pile-up in trigger logic.

Total Deadtime is combination of these.

“Reference Time” in Legacy System

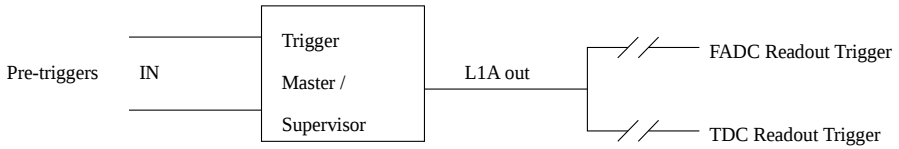
- TS output has fixed timing relative to L1A output

  → TDC common input is the built in “reference time” for all detector signals for that unit

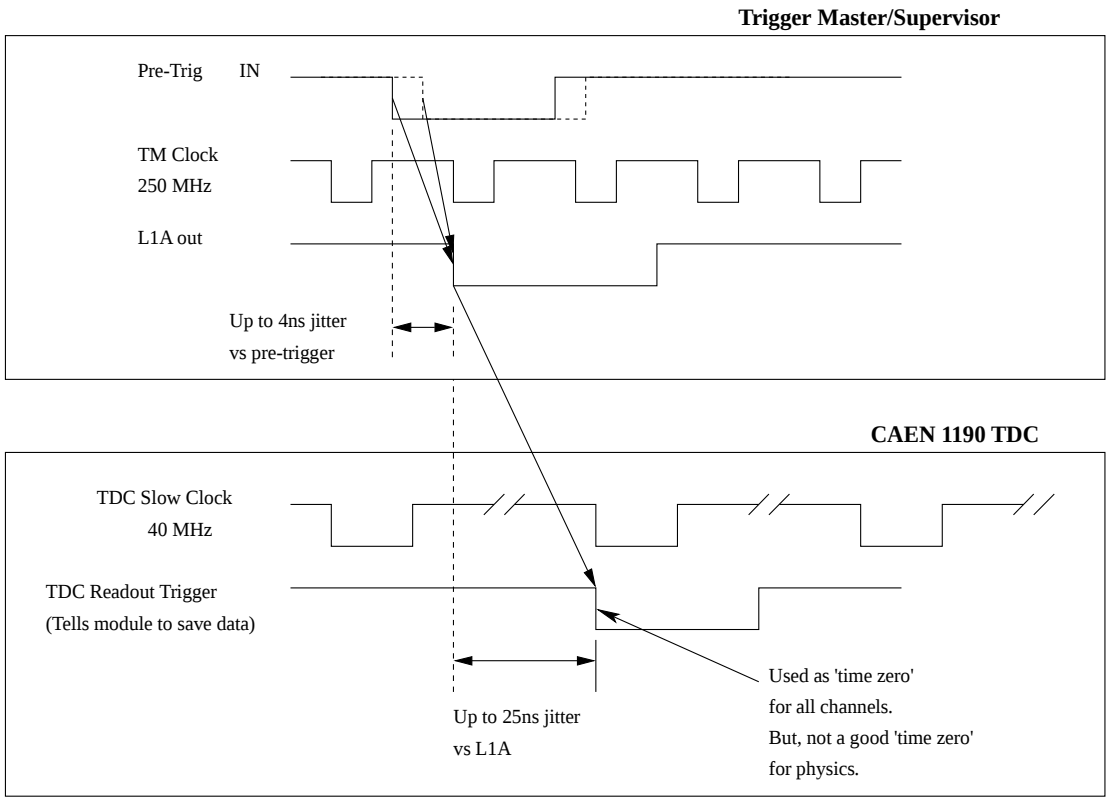


“Reference Time” in modern Systems

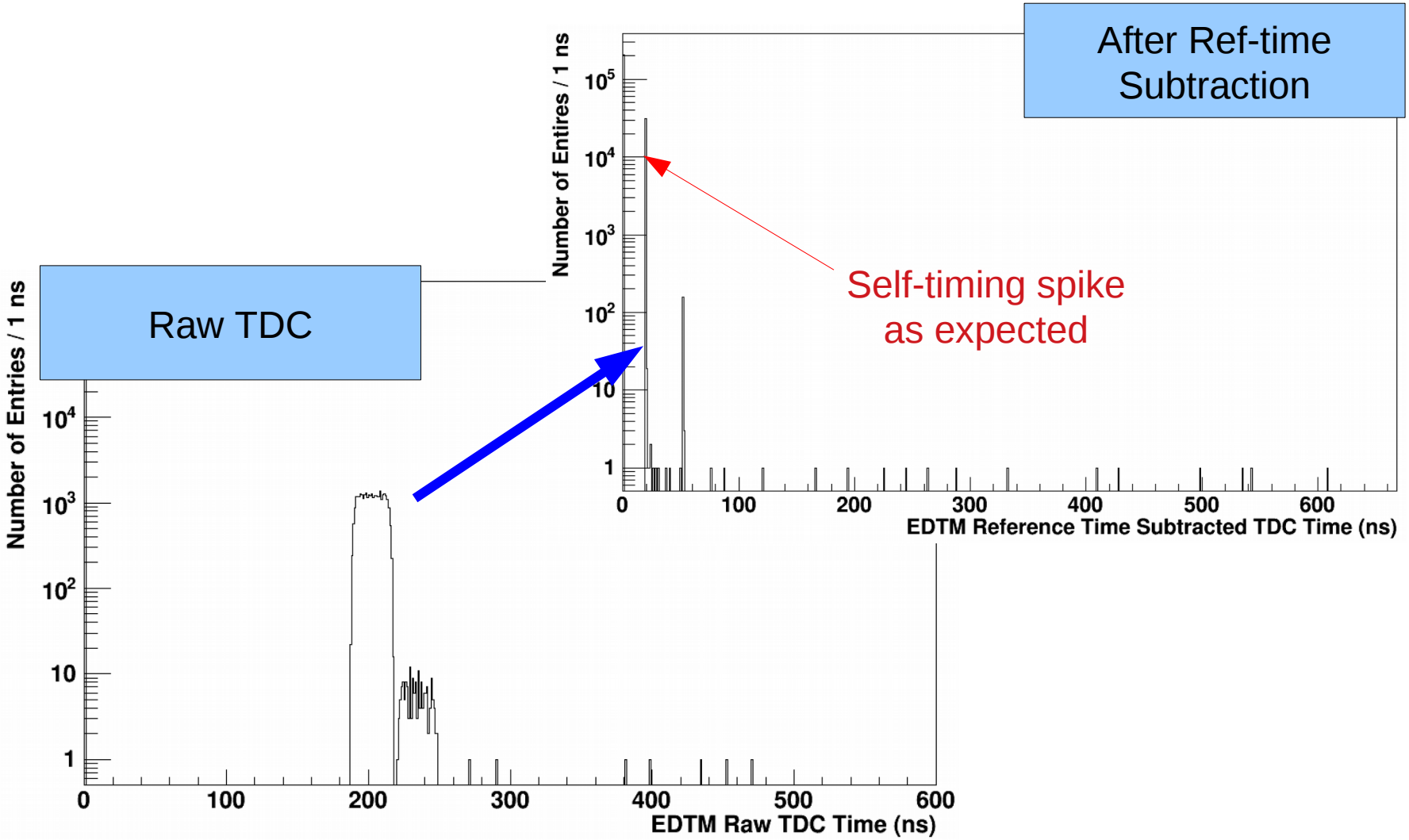
- New TS/TM output has jitter relative to inputs due to internal clock (ie. 250 MHz)



- TDC common trigger is synced also synced to slower internal clock (ie. 40 MHz)
  - → High res TDC clock only used for TDC channel inputs
  - → One of those high-res channels must explicitly be used as a 'reference' time for all the other channels
    - » We use a duplicate copy of the pretrigger



Before and After ref-time subtraction

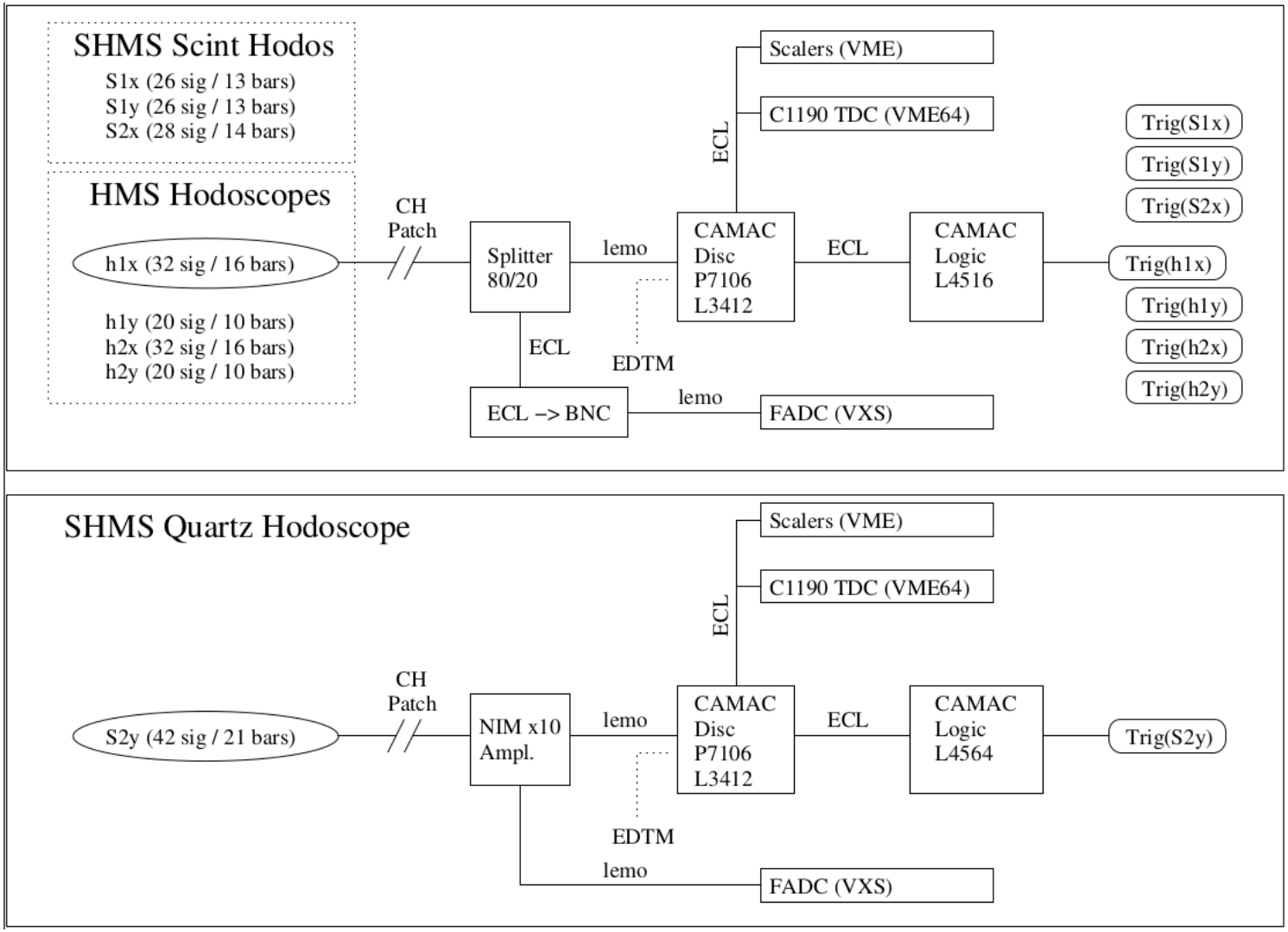


Status and To-do Lists

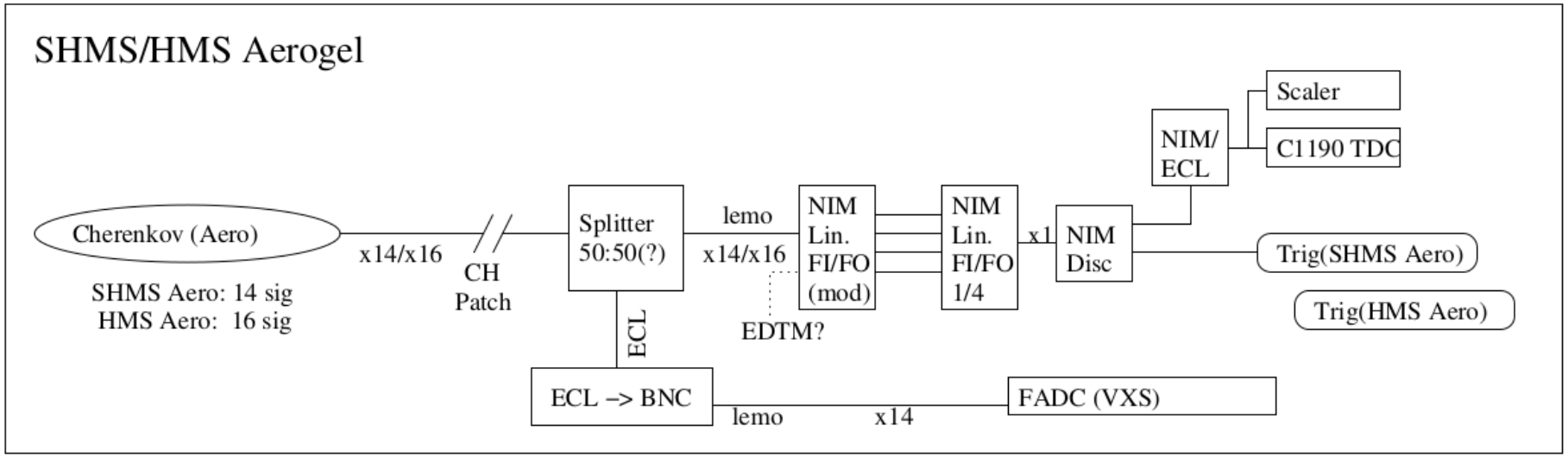
- **General Status**
  - → DAQs work in single-arm and coincident mode
  - → Triggers seem to be performing correctly
  - → Deadtime is 'OK' running in slow/conservative mode
    - » Plan to test 'simple' buffered mode operation shortly
- **Short term To Do list**
  - → Switch to buffered mode
  - → Understand discrepancies between 'simple' and 'EDTM' measures of computer deadtime
    - » EDTM is necessary for understanding electronic deadtimes upstream of the pre-trigs in the trigger circuit
  - → Polish scaler GUI operation
    - » ‘xscaler’ GUI disconnect from from the scaler server process and stops updating until restarted.
  - → Polish online monitoring GUIs
    - » Add scaler stripcharts pages
    - » Add sync-check histos (for running in buffered mode)

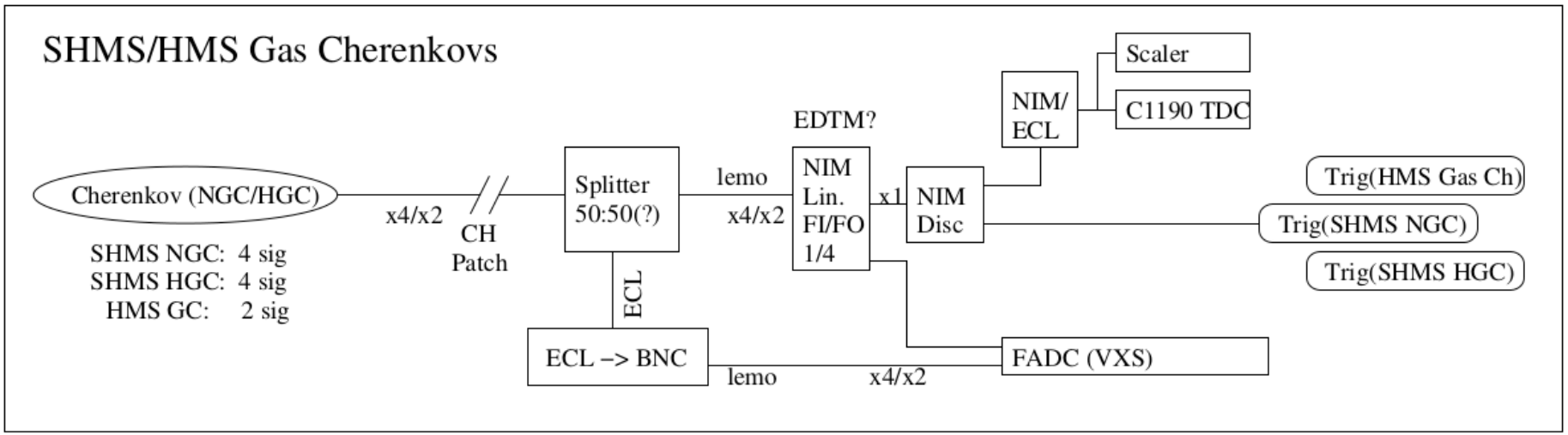
Misc/Backup Slides

Hodoscopes

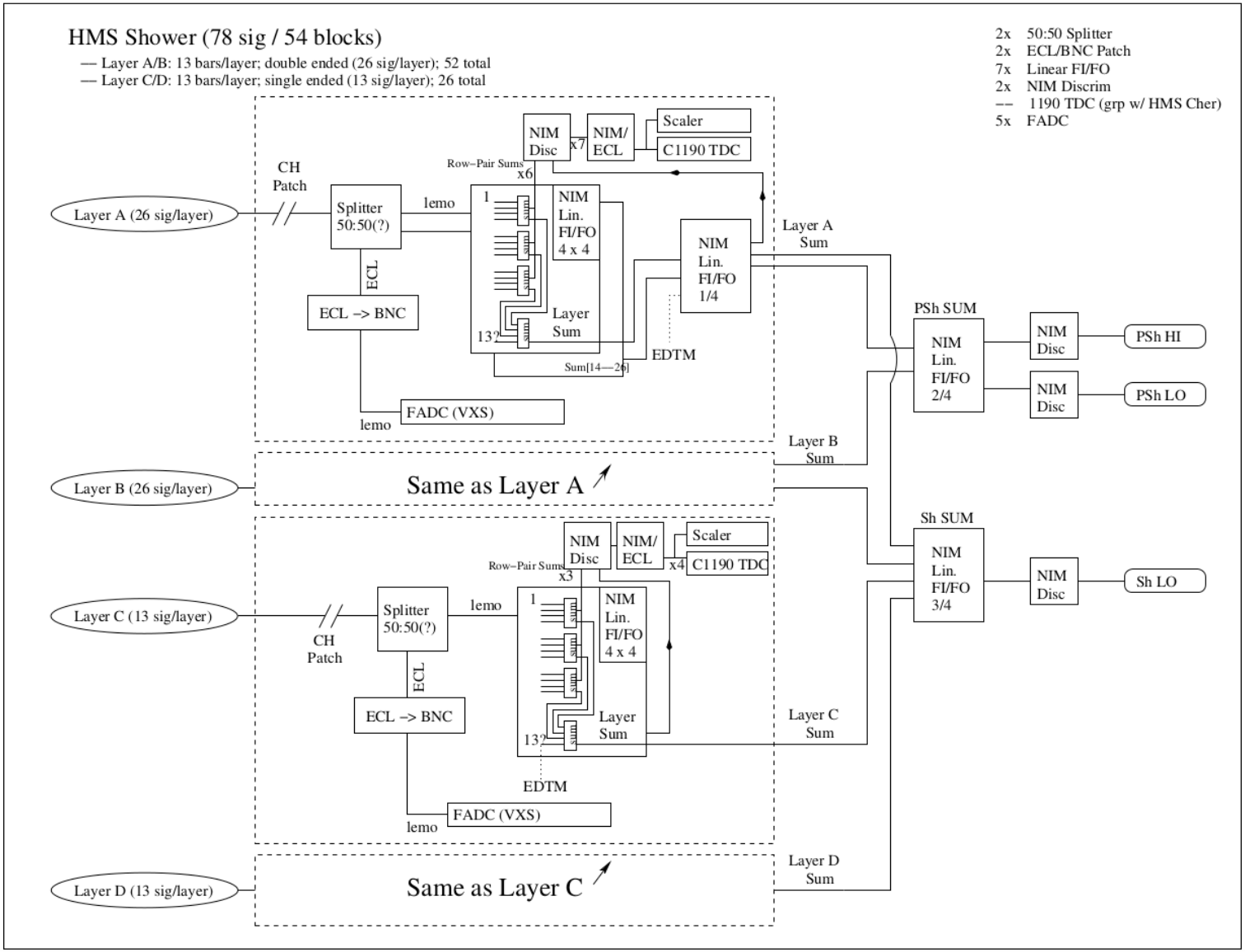

SHMS Scint Hodos
S1x (26 sig / 13 bars)
S1y (26 sig / 13 bars)
S2x (28 sig / 14 bars)
HMS Hodoscopes
h1x (32 sig / 16 bars)
h1y (20 sig / 10 bars)
h2x (32 sig / 16 bars)
h2y (20 sig / 10 bars)
CH Patch
Splitter 80/20
lemo
CAMAC Disc P7106 L3412
ECL
Scalers (VME)
C1190 TDC (VME64)
CAMAC Logic L4516
Trig(S1x)
Trig(S1y)
Trig(S2x)
Trig(h1x)
Trig(h1y)
Trig(h2x)
Trig(h2y)
ECL
EDTM
ECL –> BNC
lemo
FADC (VXS)
SHMS Quartz Hodoscope
S2y (42 sig / 21 bars)
CH Patch
NIM x10 Ampl.
lemo
CAMAC Disc P7106 L3412
ECL
Scalers (VME)
C1190 TDC (VME64)
CAMAC Logic L4564
Trig(S2y)
EDTM
lemo
FADC (VXS)

Cherekovs

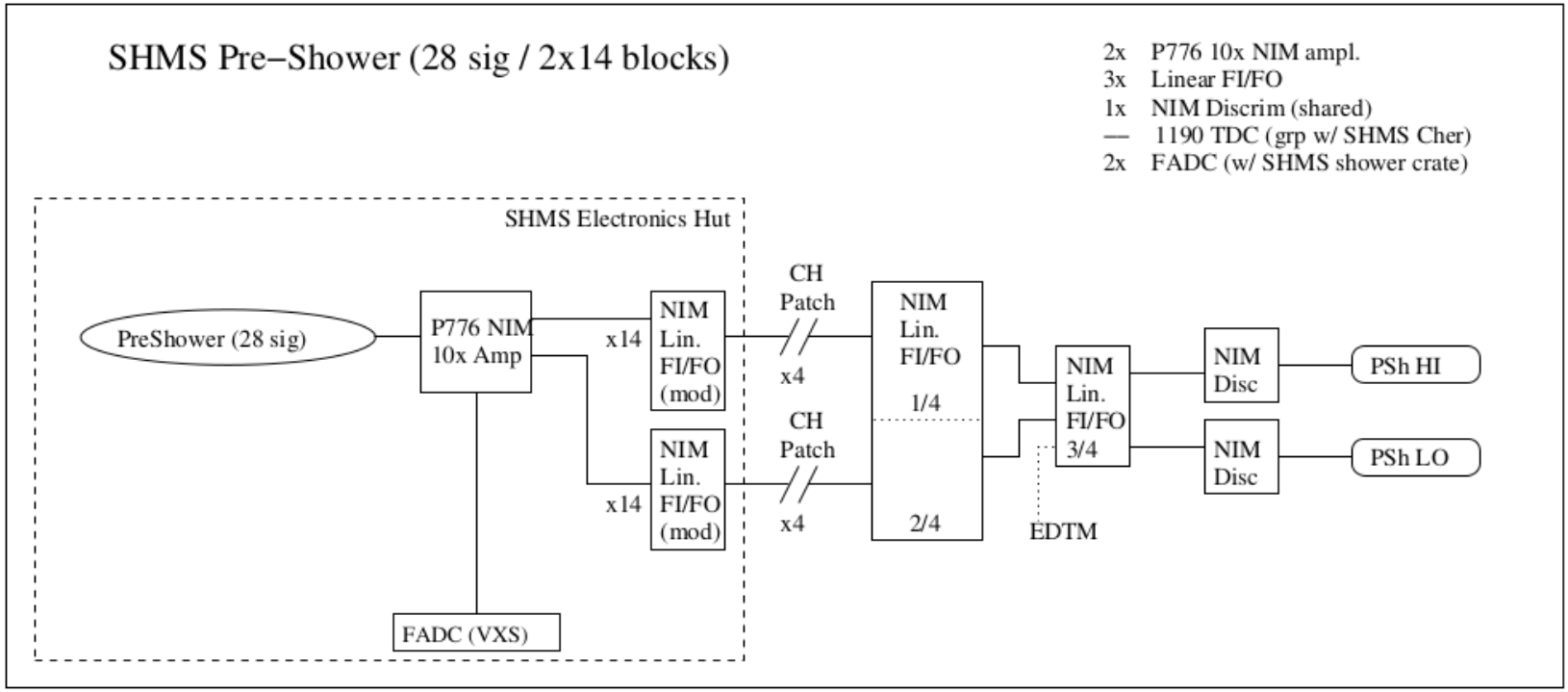

SHMS/HMS Aerogel
Cherenkov (Aero)
SHMS Aero: 14 sig
HMS Aero: 16 sig
x14/x16
CH
Patch
Splitter
50:50(?)
lemo
x14/x16
NIM
Lin.
FI/FO
(mod)
EDTM?
NIM
Lin.
FI/FO
1/4
x1
NIM
Disc
NIM/
ECL
Scaler
C1190 TDC
Trig(SHMS Aero)
Trig(HMS Aero)
ECL
ECL –> BNC
lemo
x14
FADC (VXS)


SHMS/HMS Gas Cherenkovs
Cherenkov (NGC/HGC)
SHMS NGC: 4 sig
SHMS HGC: 4 sig
HMS GC: 2 sig
x4/x2
CH
Patch
Splitter
50:50(?)
lemo
x4/x2
EDTM?
NIM
Lin.
FI/FO
1/4
x1
NIM
Disc
NIM/
ECL
Scaler
C1190 TDC
Trig(HMS Gas Ch)
Trig(SHMS NGC)
Trig(SHMS HGC)
ECL
ECL –> BNC
lemo
x4/x2
FADC (VXS)

HMS Shower


HMS Shower (78 sig / 54 blocks)
— Layer A/B: 13 bars/layer; double ended (26 sig/layer); 52 total
— Layer C/D: 13 bars/layer; single ended (13 sig/layer); 26 total
2x 50:50 Splitter
2x ECL/BNC Patch
7x Linear FI/FO
2x NIM Discrim
-- 1190 TDC (grp w/ HMS Cher)
5x FADC
Layer A (26 sig/layer)
CH Patch
Splitter 50:50(?)
lemo
ECL
ECL -> BNC
lemo
FADC (VXS)
Row-Pair Sums
x6
NIM Disc
x7
NIM/ ECL
Scaler
C1190 TDC
NIM Lin. FI/FO 4 x 4
Layer Sum
13?
Sum[14—26]
EDTM
NIM Lin. FI/FO 1/4
Layer A Sum
Layer B (26 sig/layer)
Same as Layer A
Layer B Sum
Layer C (13 sig/layer)
CH Patch
Splitter 50:50(?)
lemo
ECL
ECL -> BNC
lemo
FADC (VXS)
Row-Pair Sums
x3
NIM Disc
x4
NIM/ ECL
Scaler
C1190 TDC
NIM Lin. FI/FO 4 x 4
Layer Sum
13?
EDTM
Layer C Sum
Layer D (13 sig/layer)
Same as Layer C
Layer D Sum
PSh SUM
NIM Lin. FI/FO 2/4
NIM Disc
PSh HI
NIM Disc
PSh LO
Sh SUM
NIM Lin. FI/FO 3/4
NIM Disc
Sh LO

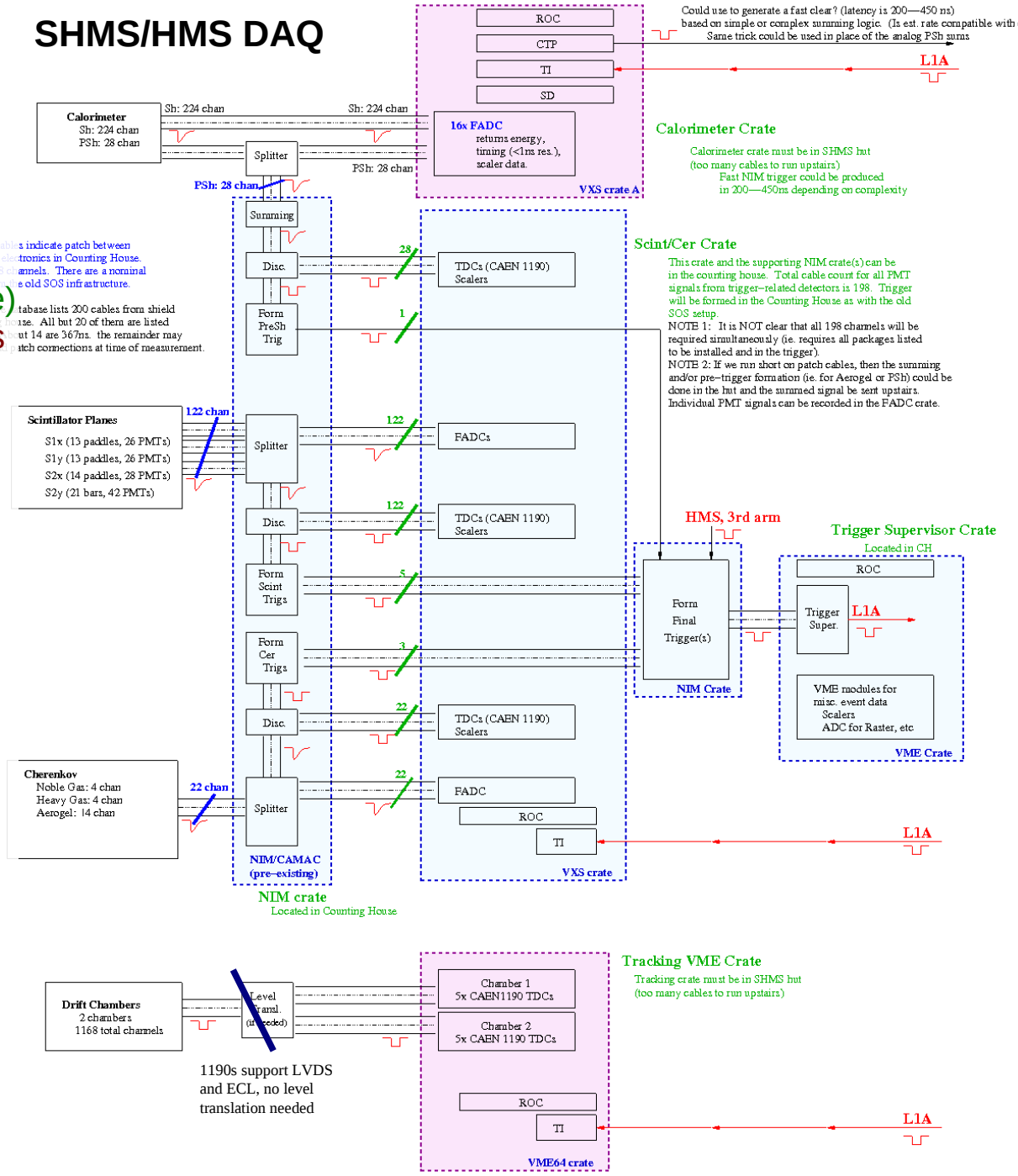
SHMS Pre-shower

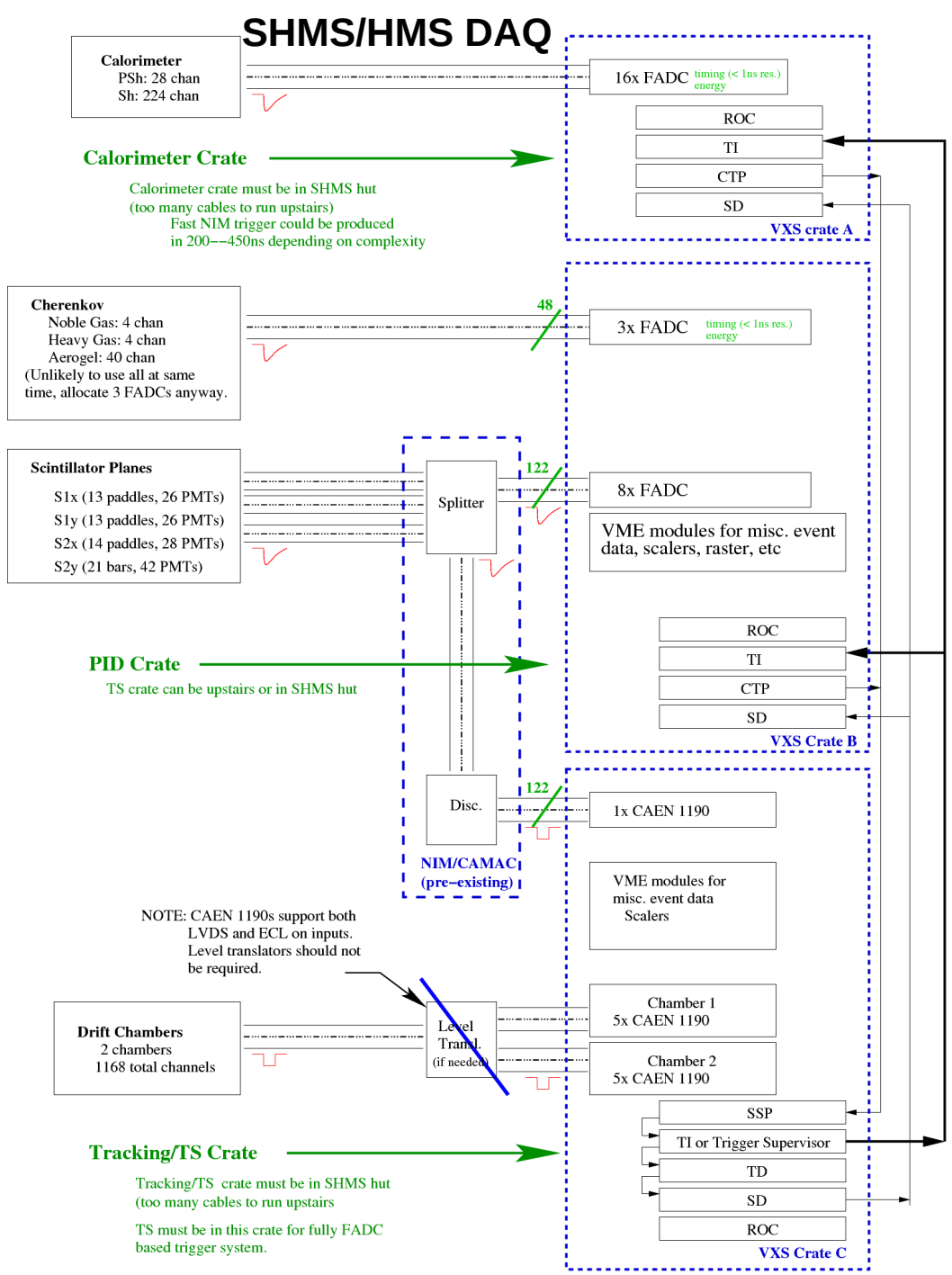


Hybrid/Legacy Trigger

- Will restore HMS trigger, SHMS has same logical design.
  - → FASTBUS electronics have been replaced with FADCs (running in integrating mode) and VME CAEN 1190 TDCs
  - → A “legacy” NIM trigger has been implemented.
  - → This is our 12 GeV starting point.
- FADCs provide ADC, TDC (~1 ns res.), and scaler data
- CAEN 1190 TDC: 100 ps res.
  - → All detectors except SHMS Calorimeter are in TDCs!
- If desired, Calo. FADCs could provide a simple sum, or more sophisticated cluster trigger with latency of ~200—400ns
  - somewhat slow for main trigger, but could be used as a fast clear

SHMS/HMS DAQ



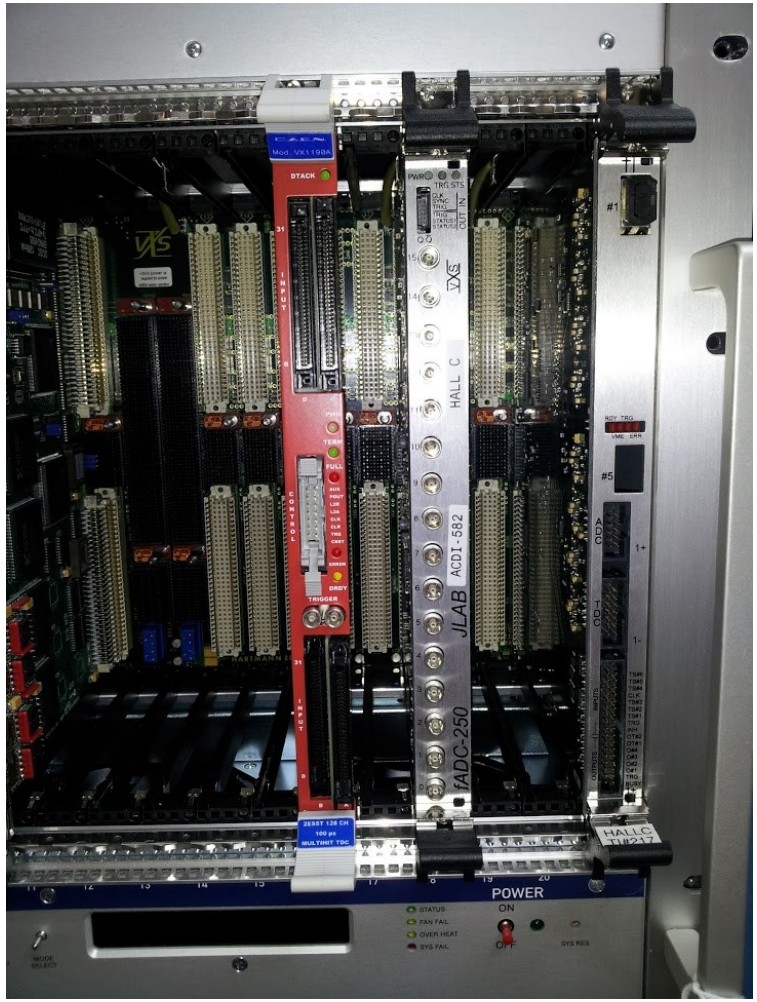


"Modern" Trigger/DAQ

- "Stage 2" evolution of system
  NOT planned for first set of experiments
  - fully pipelined capable
  - 'deadtimeless' operation at >10kHz possible
- Legacy/NIM logic will be left in place and can be used as either primary or auxiliary trigger.
  - (Will need legacy trigger to debug/cross-check any FADC logic anyway)
- DAQ can be configured for:
  - high-speed fully-pipelined mode
    - trigger can be generated in NIM logic, *or* in firmware
  - "Hybrid mode"
    - ie. in conjunction with non-pipelined 3rd arm, etc.

New Inventory

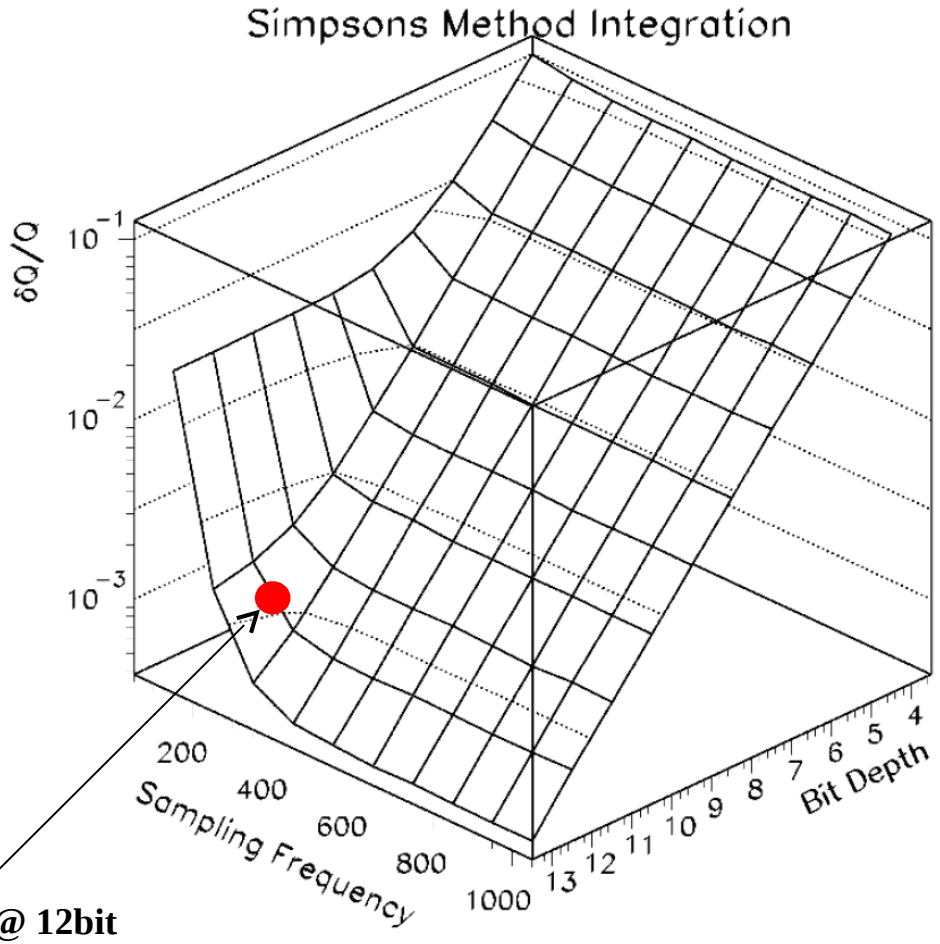
- 4 new VXS crates
  - → primarily used to support FADCs (special J0 backplane bus)
- 640 ch JLab FADC [40 mod]
  - → SHMS: 422 ch / HMS: 200 ch
- 2304 ch CAEN 1190 TDC [18 mod]
  - → SHMS: 1290 ch / HMS: 810 ch
- 2 New Trigger Supervisor (TS) boards
- 5 New Trigger Interrupt (TI) boards
- 2 Trigger Distribution (TD) boards
  - → fans triggers/clocks out to crates
- 2+2 Signal Distribution (SD) board
  - → fans triggers/clocks out to FADCs
- 3 Crate Trigger Processor (CTP) boards
- 1 Sub-System Processor (SSP) board
- 'Special' multi-fiber optical cable run SHMS <-> HMS <-> CH



3.4 FADC Sampling – Charge Accuracy

Hall D FCAL PMT: FEU 84-3

- **10,000 Random height pulses 10-90% full scale of ADC range simulated**
- **Sampling frequency makes little difference beyond 250MHz at 12bit, providing ~0.1% charge resolution**
- **PMT pulse shape dominates sample frequency and bit depth of ADC**



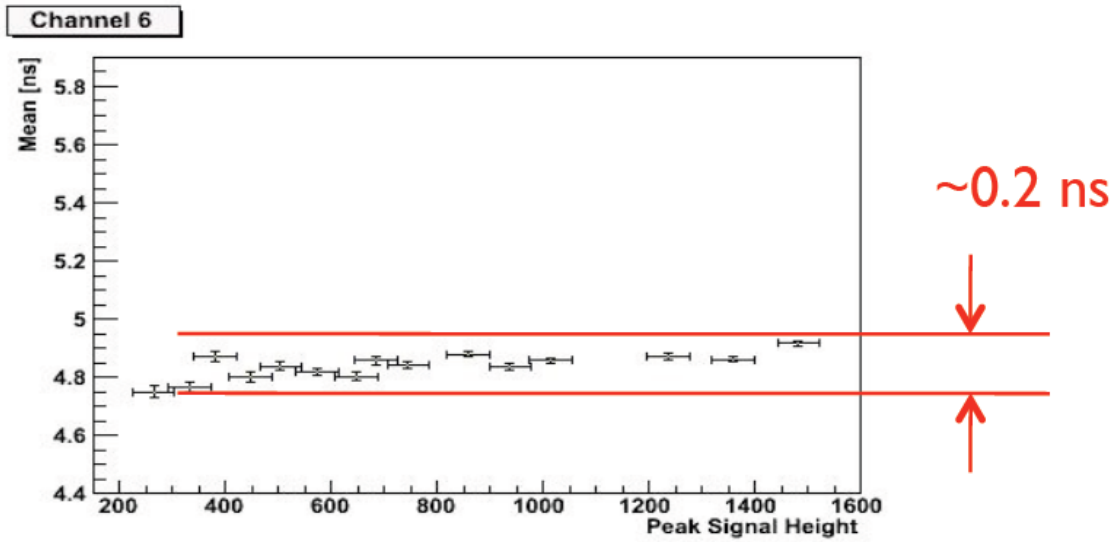
250MHz @ 12bit

FADC Sampling – Timing Accuracy

Hall D FCAL PMT: FEU 84-3

- **Timing algorithm developed & tested by Indiana University for the Hall D forward calorimeter.**
- **Implemented on the JLab FADC250 hardware achieving <300ps timing resolution on 50% pulse crossing time with varied signal heights.**

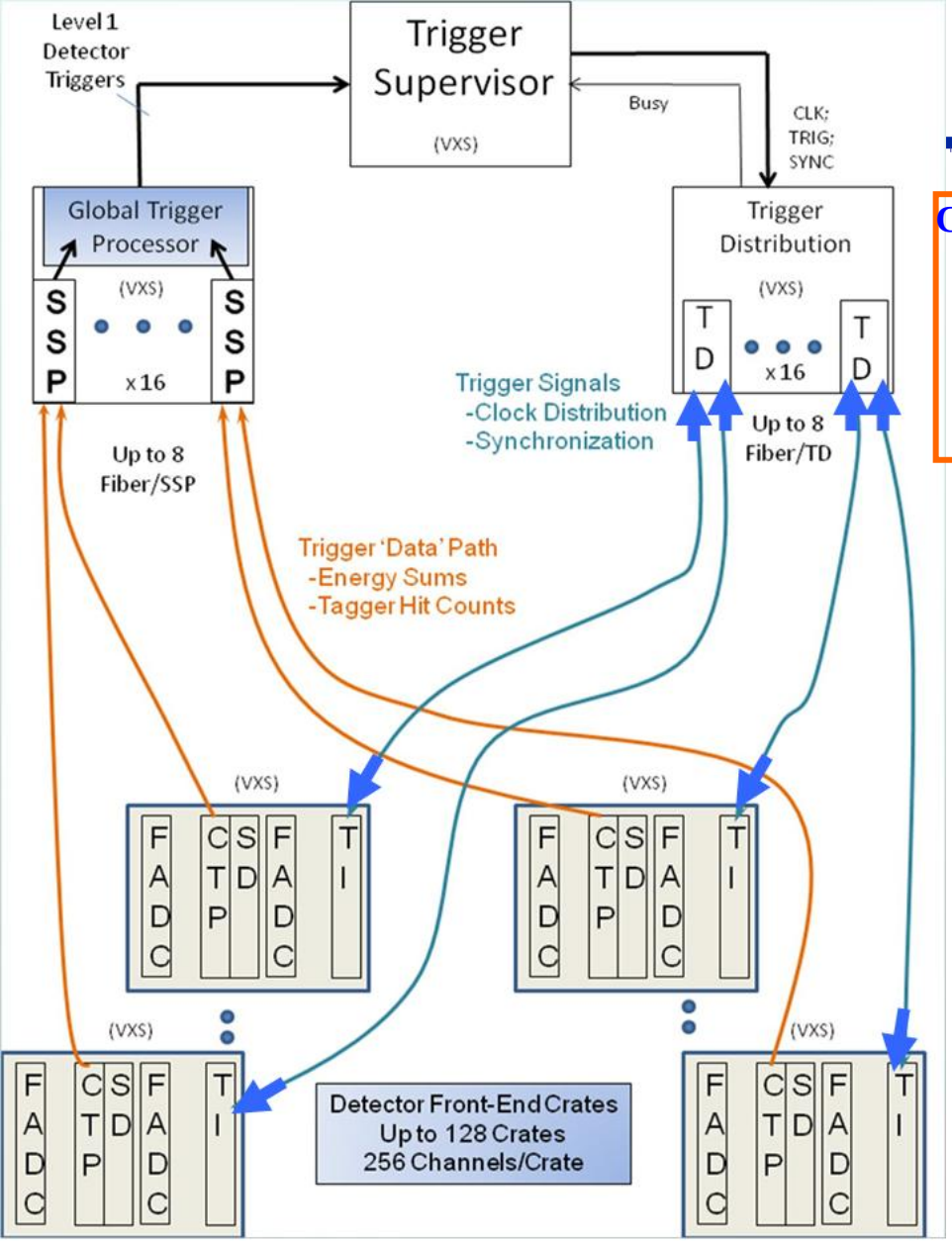
- Resolution allow reliable information to link calorimeter with tagged electron bunch.



Typical timing resolution achieved ~1/10 the sample rate. The PMT shape will drive the ADC sample rate & depth requirements.

From: GlueX Doc# 1258-v1

Trigger System Diagram



CTP -> SSP -> GTP
L1 Trig_Data
Uni_Directional

Energy Sums

TS -> TD -> TI
Link
1.25Gb/s
Bi-Directional

BUSY
Trigger Sync
Trig_Comnd

Trigger Supervisor (Distribution)

Global Trigger Processing
Sub-System Processing (Multi-Crate)

Crate Trigger Processing

Flash ADC Modules

Detector Signals

F250 Dynamic Noise Suppression

- Added 60 Hz background with increasing amplitude
  - → fan signal to QDC (v792) and FADC
  - → FADC signal gets 'pedestal subtracted' event-by-event by averaging samples before the pulse in digitization window.
- This was done offline, but would be easy to do in firmware.
- Work done by Charlie Dauchess (now undergrad at Va Tech)