SVT DAQ Status

HPS Collaboration meeting June 17th 2014

Ben Reese, Ryan Herbst, Per Hansson Adrian

Outline

Overview

Front end board

Vacuum penetration boards

High speed and magnetic field tests

DAQ platform and JLab integration progress

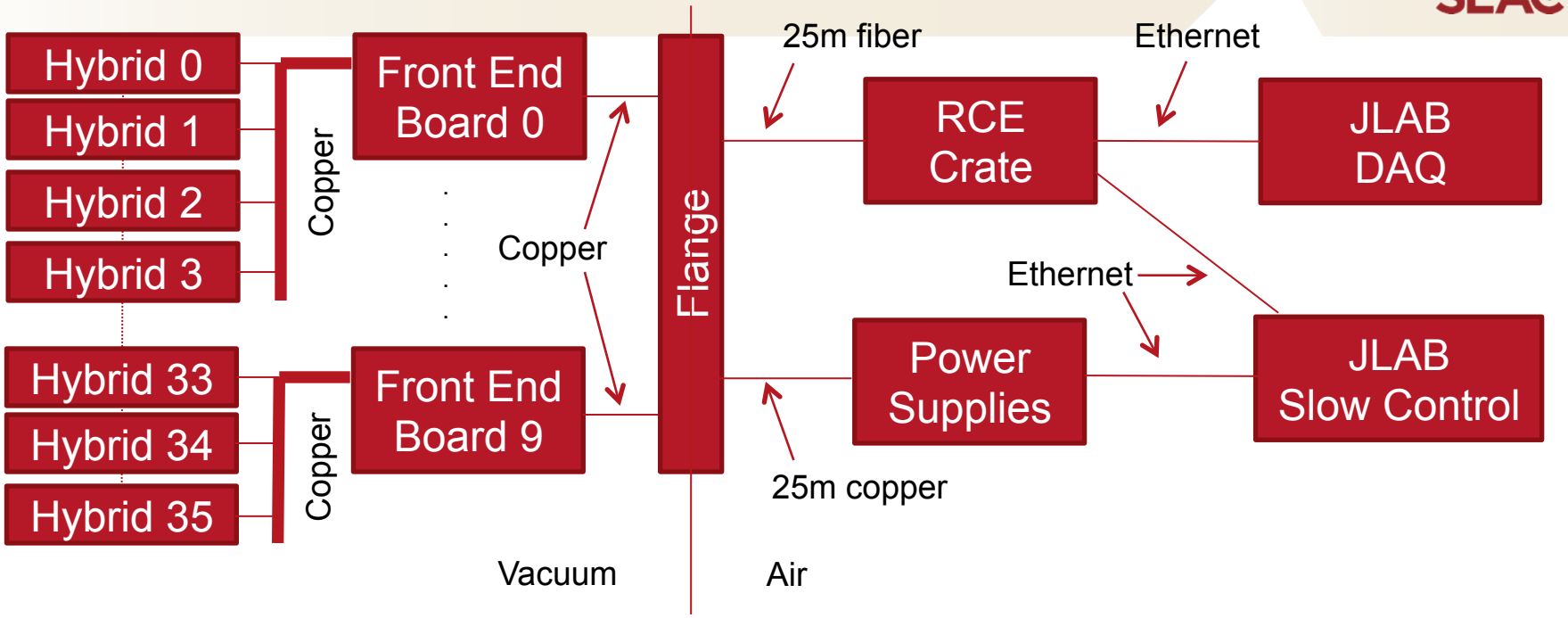
Project management

For internal cabling and hybrids, see talks from Omar, Sho and Tim

More detailed information:

- Ryan's talk tomorrow
- https://confluence.slac.stanford.edu/download/attachments/158045620/hps_svt_daq_collab_winter2014_ben.pptx?version=1&modificationDate=1390425987000&api=v2
- https://confluence.slac.stanford.edu/download/attachments/158045620/hps_svt_daq_herbst_20140122.pptx?version=1&modificationDate=1390419798000&api=v2

SVT Overview



- 36 hybrids
  - 12 in layers 0 – 3 (2 per module)
  - 24 in layers 4 – 6 (4 per module)
- 10 front end boards
  - 4 servicing layers 1 – 3 with 3 hybrids per board
  - 6 servicing layers 4 – 6 with 4 hybrids per board
- RCE crate: data reduction, event building and JLab DAQ interface

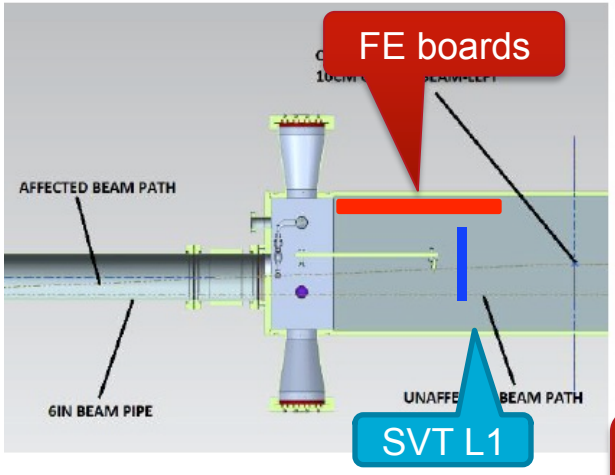
Raw ADC data rate (Gbps)	
Per hybrid	3.33
Per L1-3 Front end board	10
Per L4-6 Front end board	13

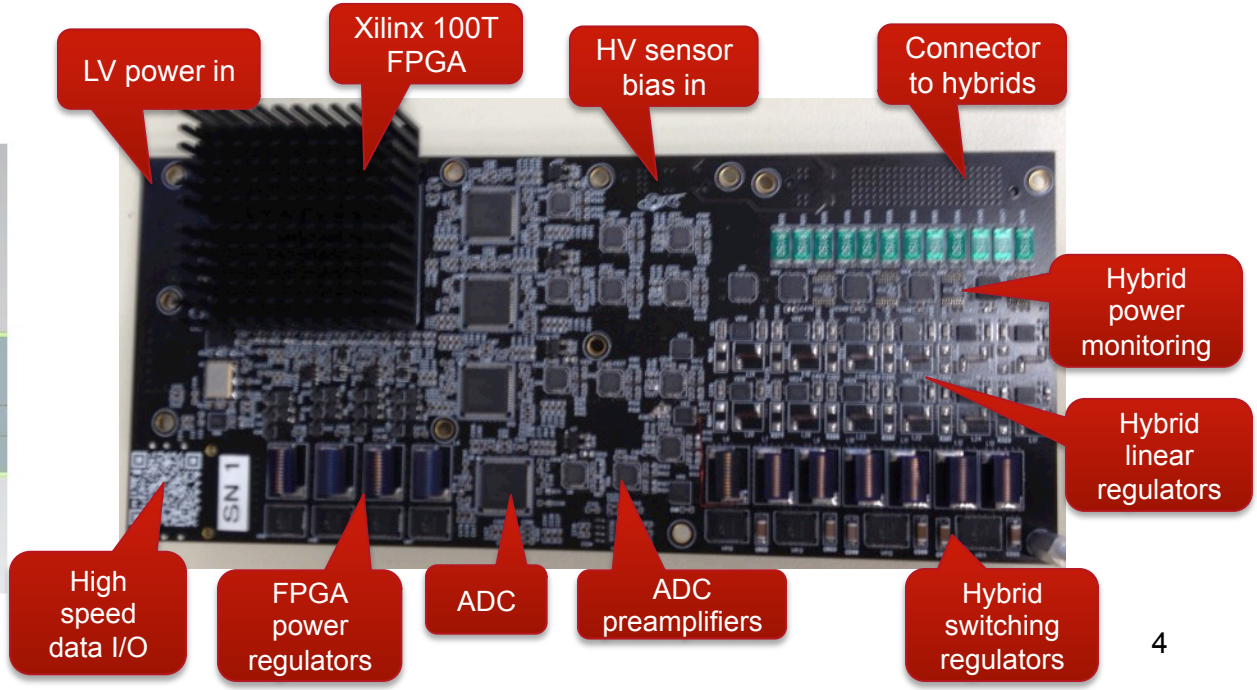
Front End Board

Purpose

- Digitize APV25 outputs
- Shorten distance between APV25 and ADC converter
- Local power conversion (simplify vacuum penetration), control and monitoring for hybrids
- Control configuration of APV25 and ADC chips (I^2C, SPI)
- Send (raw) ADC samples on high-speed PGP links to RCE crate (via flange board)

<=4 hybrids/FEB
10 FEB in total

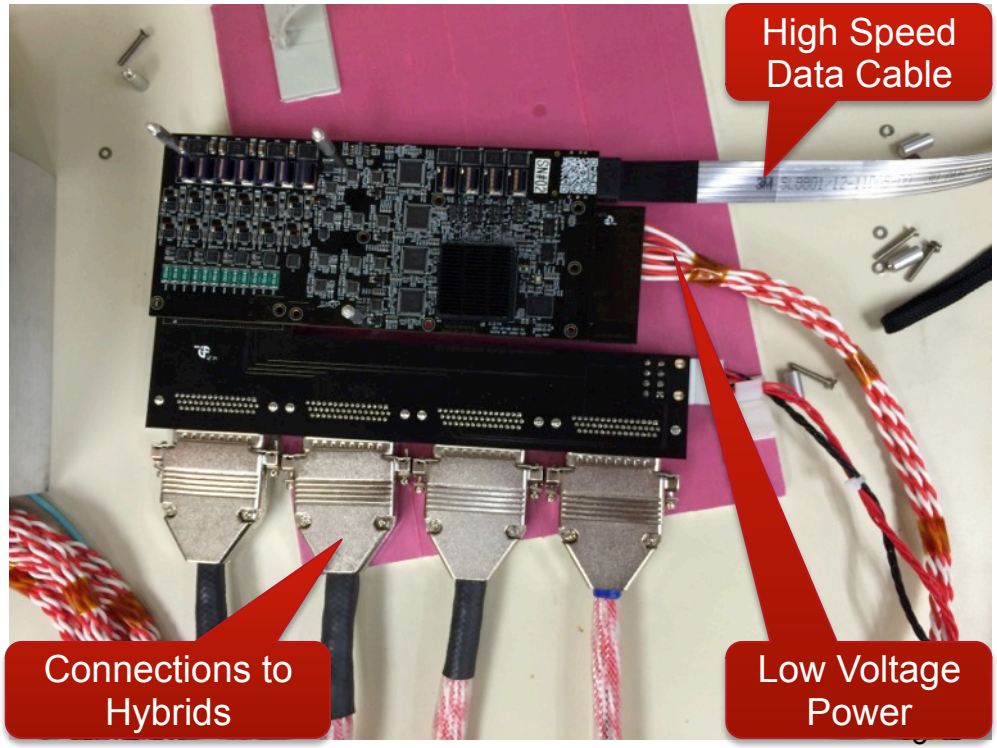




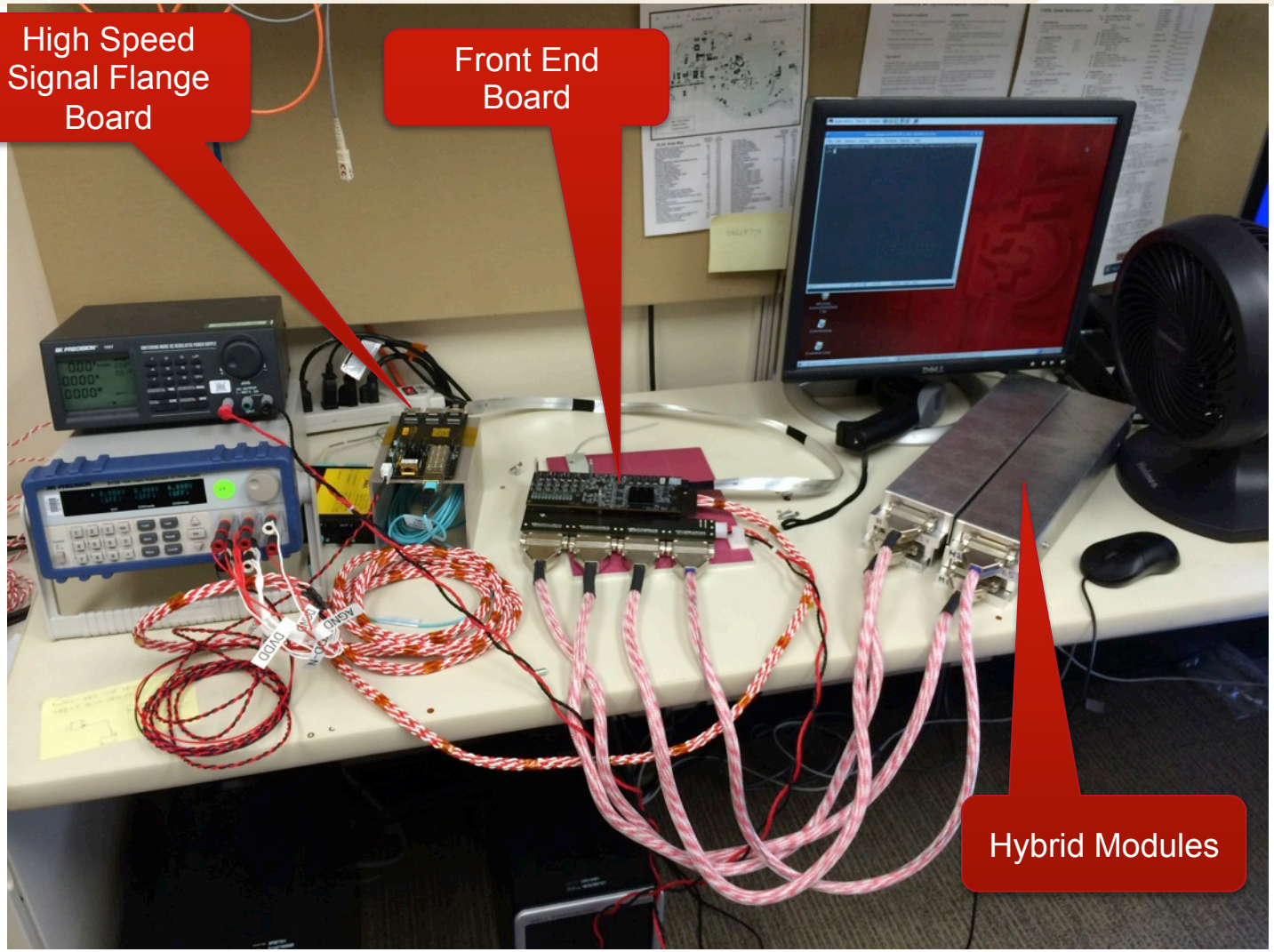
Front End Board - Status

- Successfully running with 4 attached Hybrids.
- High speed transceivers and signal cable verified.
- Voltage regulators verified (all 25 of them).
- All 20 ADC channels verified.
- Noise performance is good.

- Rework needed:
  - Wait for digital power stable before
    allowing analog regulators on
  - Move mounting holes
  - 1-2 dumb schematic mistakes
  - **All very minor changes**
- Respin to be ordered this month

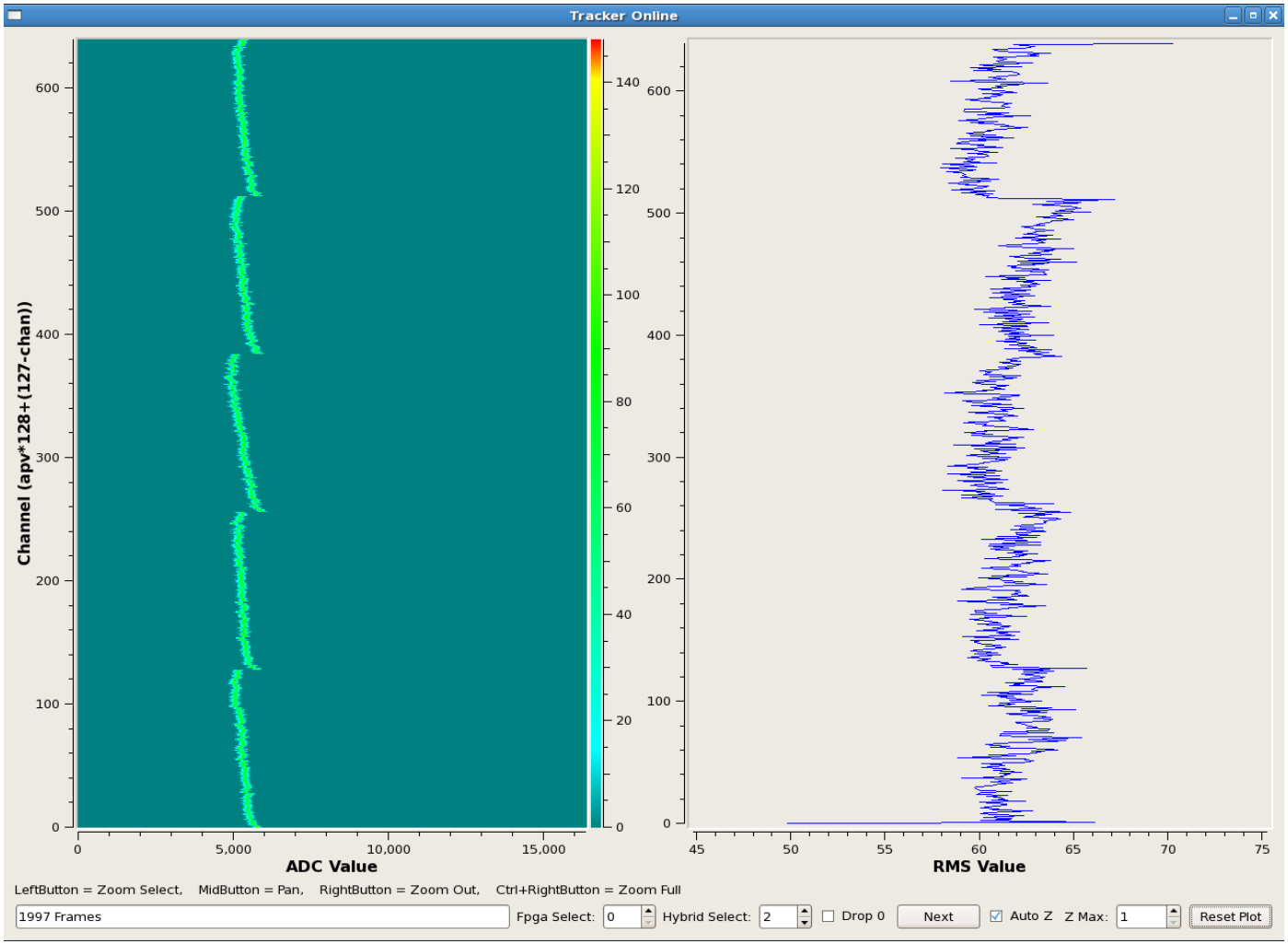


Front End Board – Test Setup

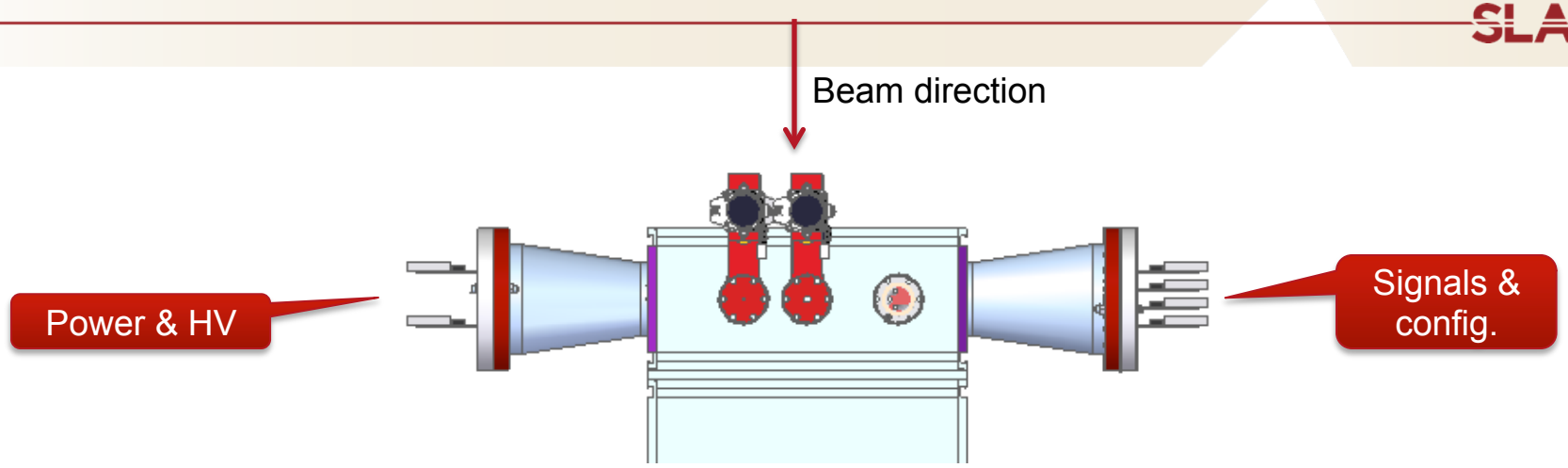


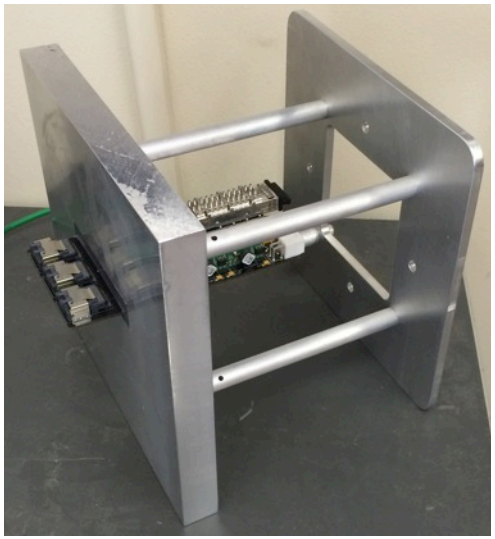
Front End Board - Noise Performance

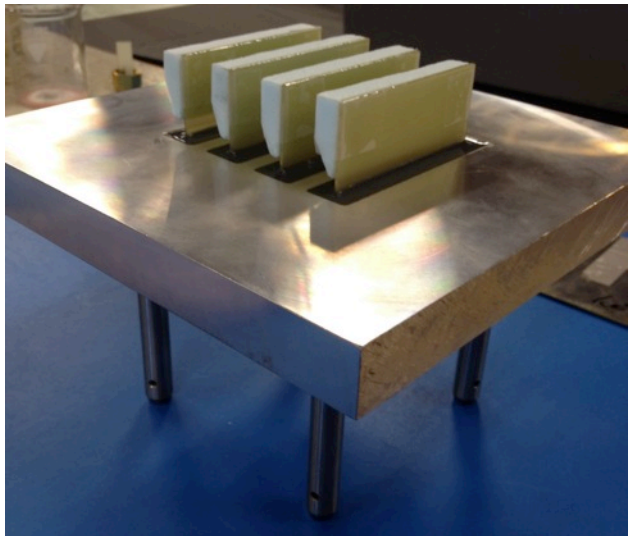
- Noise level between 55 and 65 ADC counts – similar to Test run detector
- Further testing is ongoing



Flange Boards - Vacuum Penetration

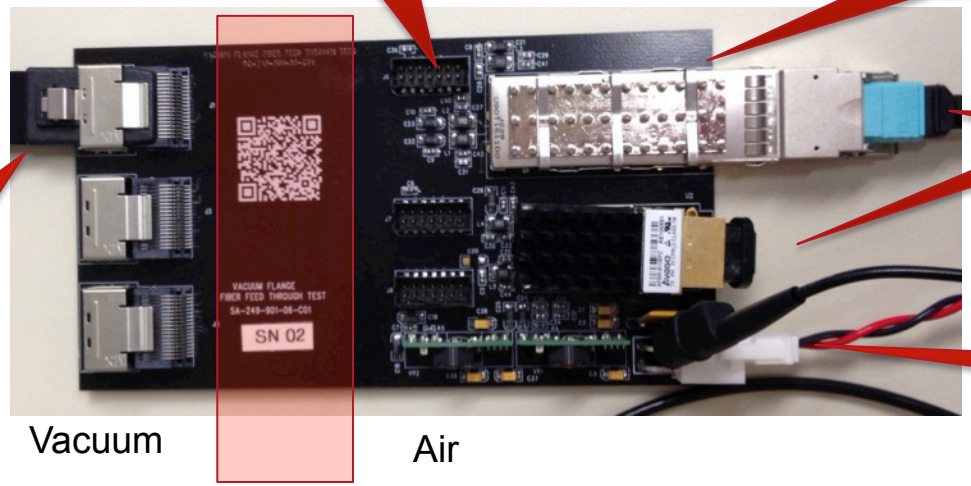






Potting procedure tested and vacuum seal verified
Standoff for strain relief & transport designed
M. McCulloch, S. Osier (SLAC engineers)

Signal Flange Board



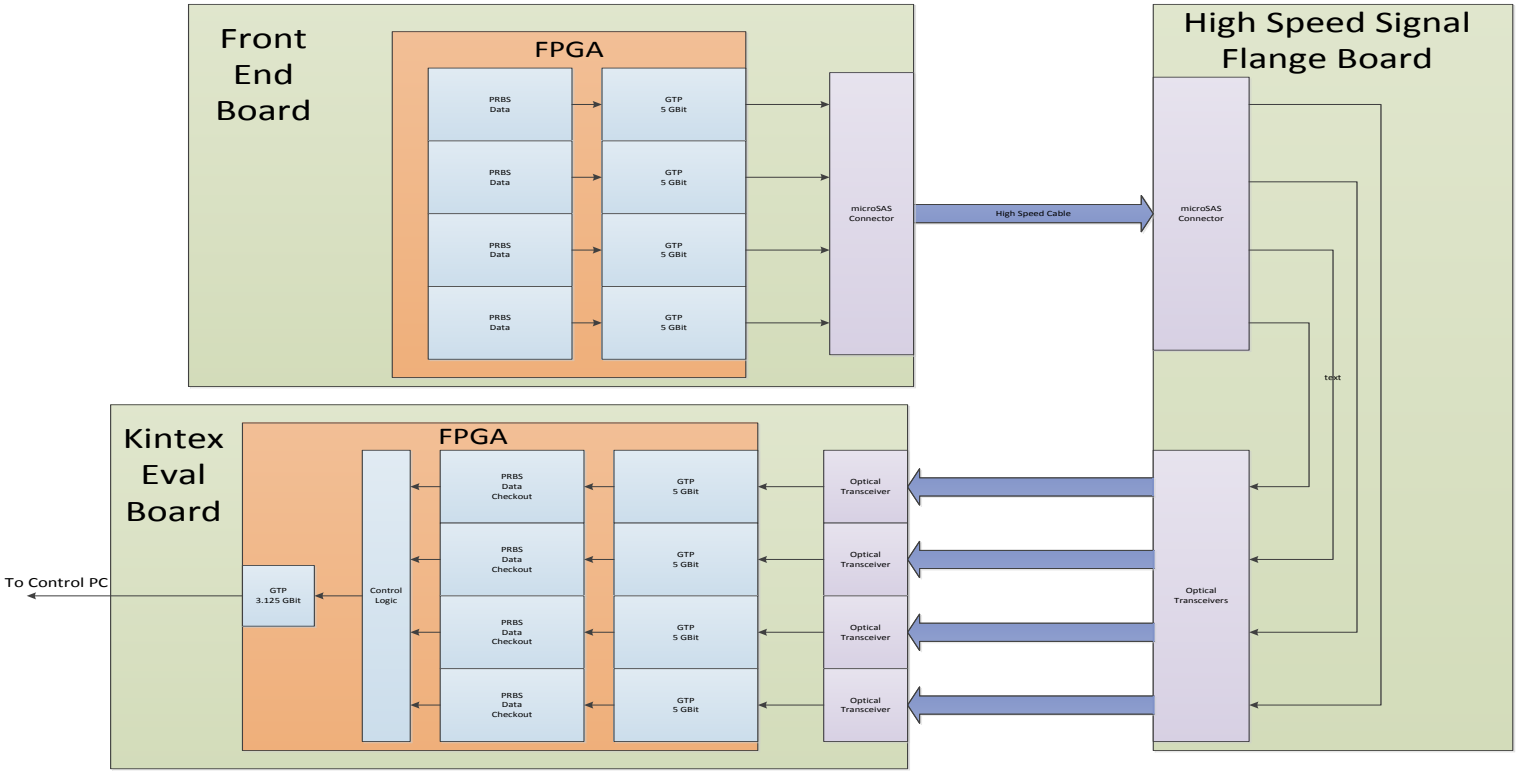
- Three front end boards per flange board
  - 1x2.5 Gbps full duplex link per FEB for control/configuration
  - 4x5.0 Gbps upstream high speed link per FEB for data
- Optical conversion outside vacuum
- Fully functional boards in hand
  - Used in all Front End board testing
  - 5Gbit links tested on all channels
- Rework needed
  - Minor grounding change to isolate front end boards
  - Mechanical (bonuses): holes for stress relief, potting surface finish
  - **All minor changes**

- Production boards ordered this week

High Speed Signal Test

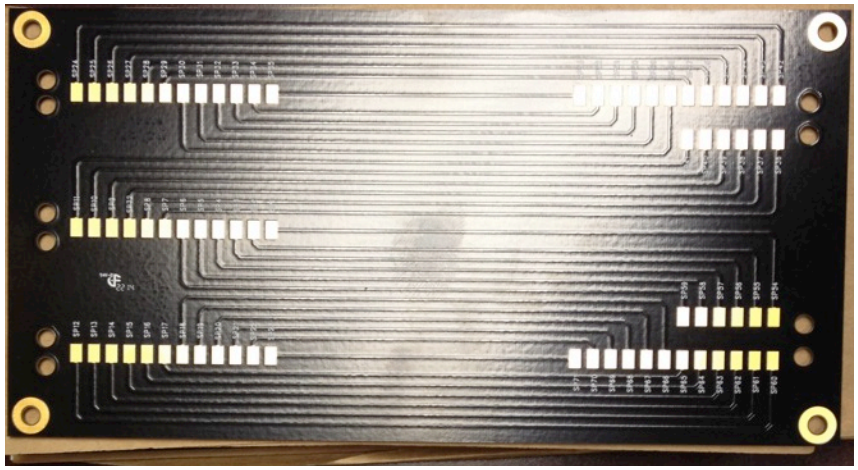
- Pseudo random data transmitted from FEB at 5 Gbit/s on all four channels
- Passed through high speed signal flange board – converted to optical
- Received on Kintex Evaluation Board – Converted back to differential
- Data verified on Kintex FPGA
- Verification status sent to control PC
- Repeat for each of the 3 FEB channels on the flange board

⇒ **All tests pass. No bit errors observed**

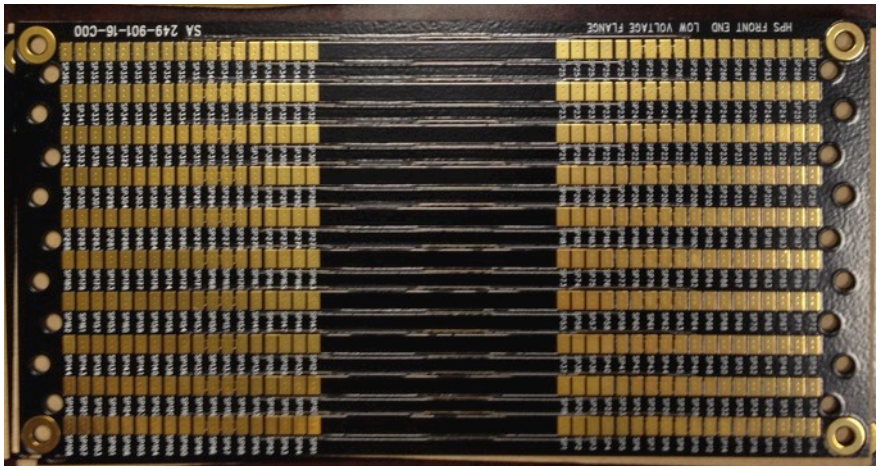


Power and HV Flange Boards

HV sensor bias board



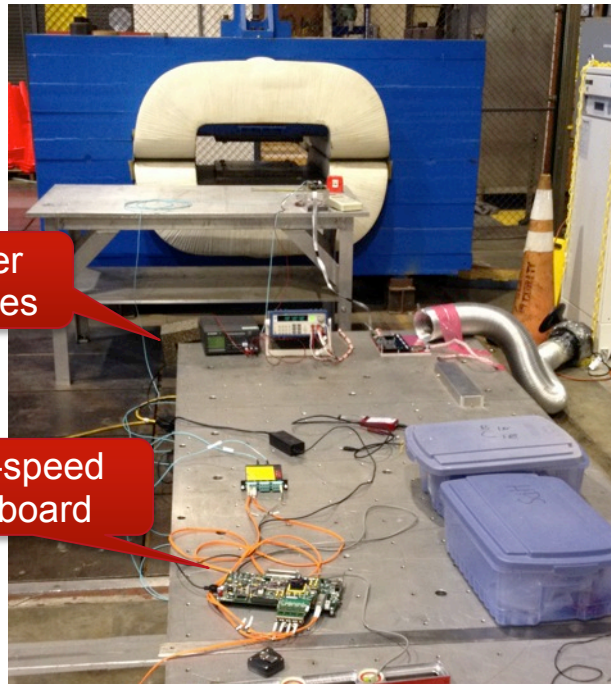
LV power board

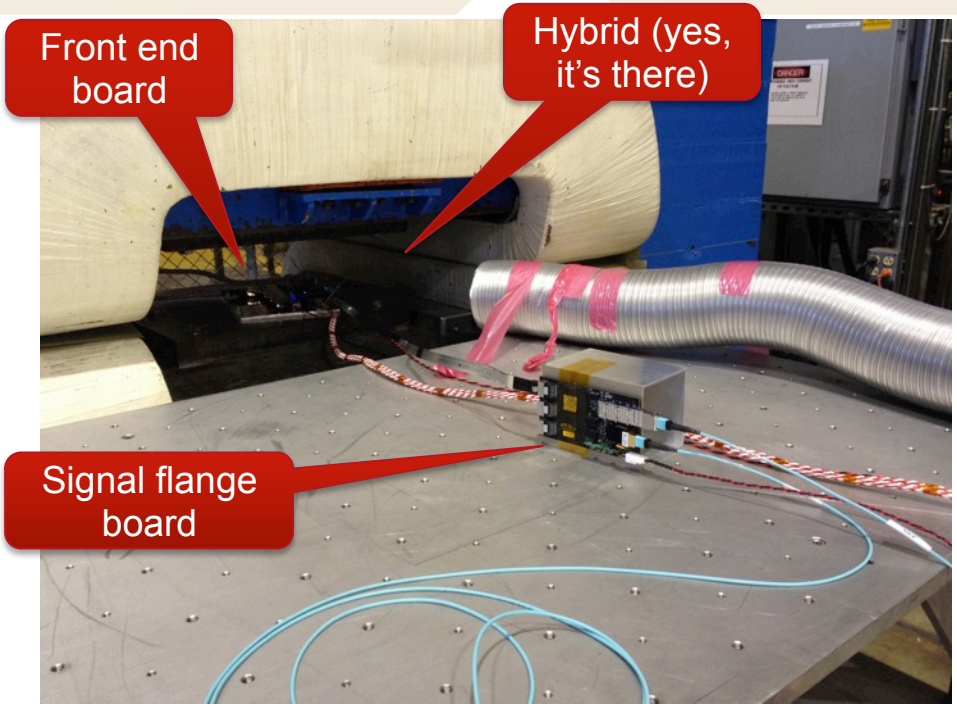


Low voltage power and HV sensor bias

- **Services all of SVT**
- "Simple" feed through boards
  - Pigtails soldered on both sides with connectors
  - Work focused on surface finish, stress relief, transportation and handling safety
- Status
  - All boards in hand
  - Pigtails soldered this week for testing
  - Potting setup ready, stress relief hardware designed

Magnetic Field DAQ Test





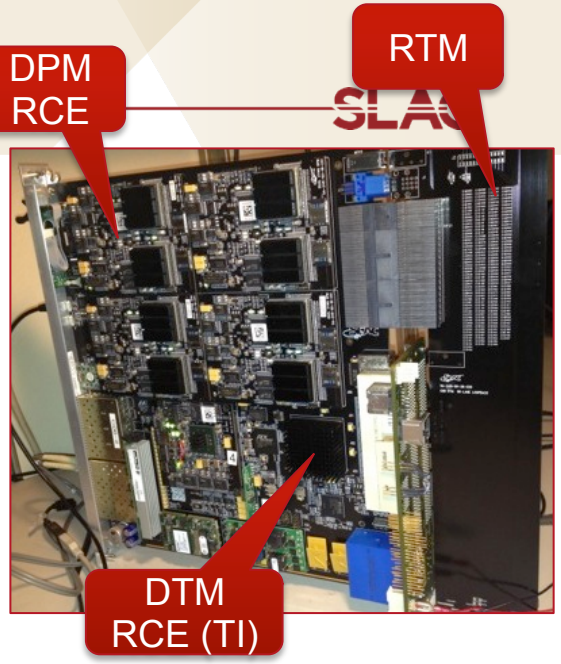
Front end board tested in bore of dipole magnet

- Studied hybrid noise characteristic and power distribution
- Could not detect effect up to at least 1.5T
- Early DAQ was unstable but no correlation with field was established

Flange board tested in fringe field

- Expect to be operated in fringe field of a at most few percent of bore field (~100Gauss)
- No detected high-speed bit errors up to 1000Gauss (in different orientations)

RCE Platform - Status



Hardware

- COB, DPM and DTM production boards in hand
- RTM (interface board) for HPS in hand but need minor rework
  - Use generic development board for now

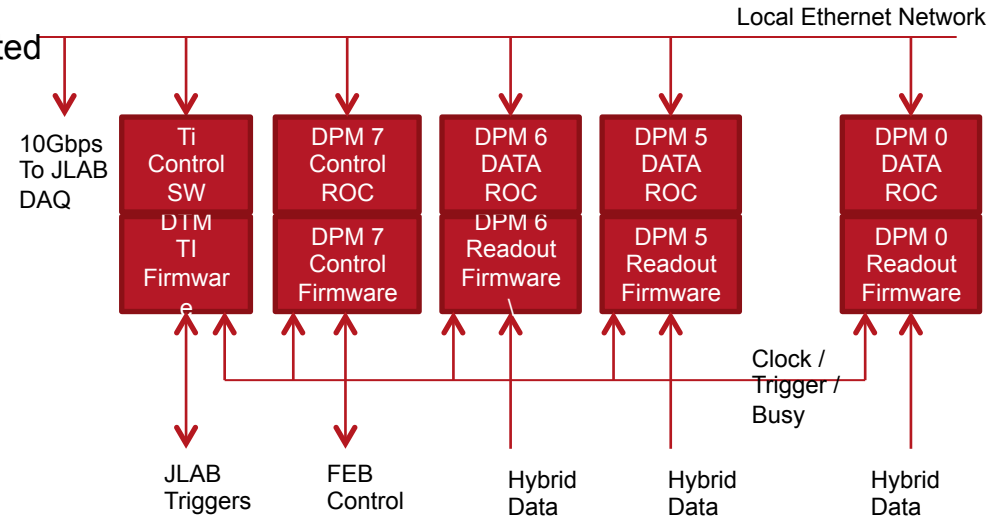
JLab integration

- New Multi-ROC trigger interface implemented and used on RCE platform
- New CODA version distributed by Sergey is used
- Currently hashing out system configuration for integrated high rate tests
- Other specific open items: SVT configuration and calibration implementation

High rate tests (see Ryan's talk tomorrow)

- >100kHz from standalone DMA tests with emulated data
- Working on CODA integration for final tests
  1. ROC and event builder
  2. Trigger interface
  - Expect factor 2 in performance loss based on experience

Dedicated integration week planned for JLab in early Aug.



Power Supply and External Cabling - Status

Hardware

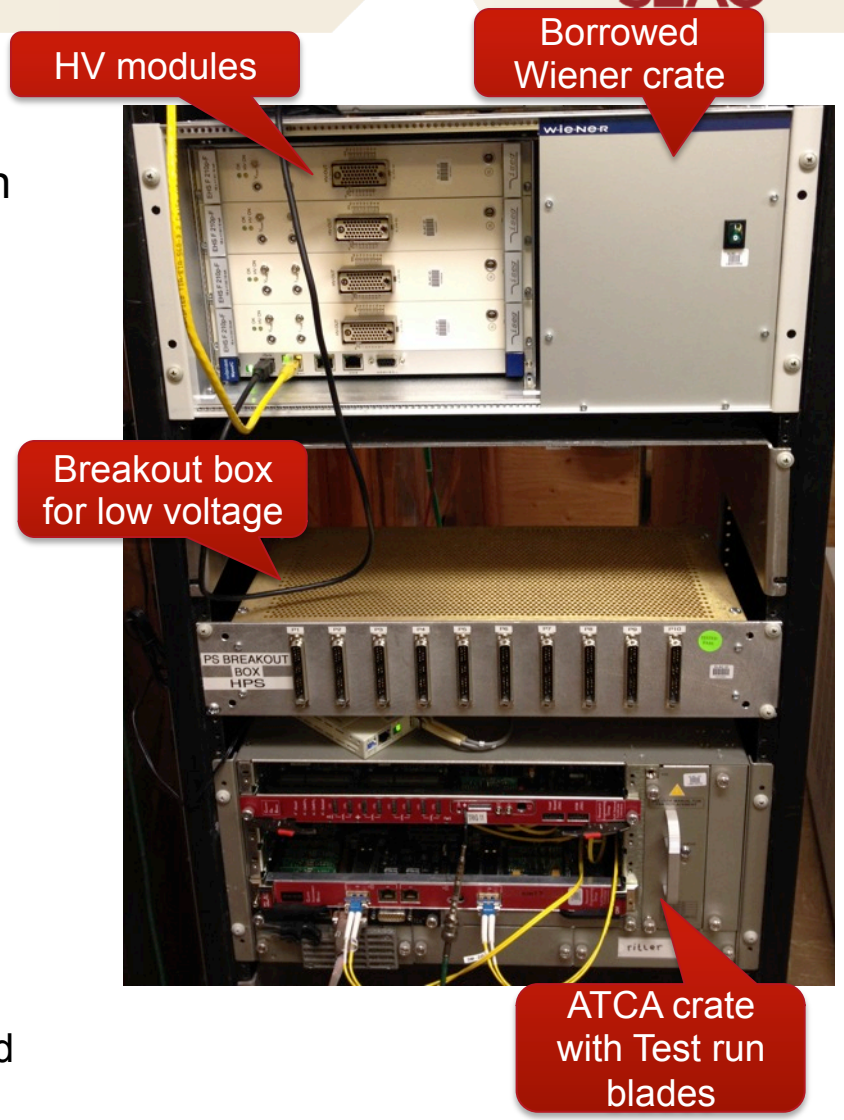
- High voltage cards in hand
- Wiener MPOD crate and low voltage cards in July (borrowed hardware in hand for testing)

Power & high voltage bias cabling

- Long runs from supplies to flange done
- Flange board pigtails undergoing testing
- Need to understand detailed cabling routes close to vacuum box

Slow control

- Slow control group develop controls on borrowed units at JLab
- EPICS IOC for SVT control being developed
  - Core functionality in EPICS and SVT DAQ verified
  - Good backup help from Hovanes, Nerses and Bryan



Budget and Schedule

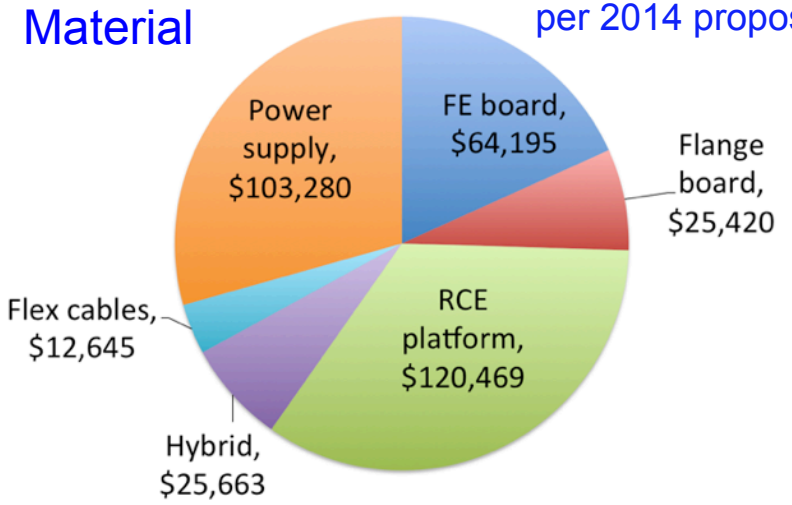
Budget

- Material costs roughly on budget (ask for small addition from contingency)
- Labor estimates were low
  - Balance between project items roughly correct
  - But overall the system is late compared to proposal
  - Need continuing large electrical engineering until Nov.

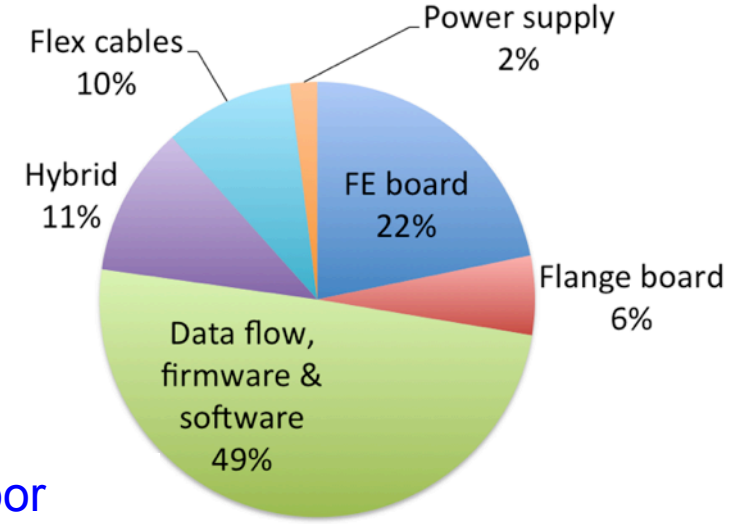
Schedule

- Hybrids, Front end board and internal cabling have largest delays
- Keep sufficient padding for large scale system testing at SLAC and JLab before installation
- Goal is to be ready for shipping in beginning of Sep. (see Marco's talk)

Material per 2014 proposal



Labor



Summary

SLAC

Major progress across the SVT DAQ project since last collaboration meeting (yes, it was planned and needed)

Material and manpower budget were well balanced

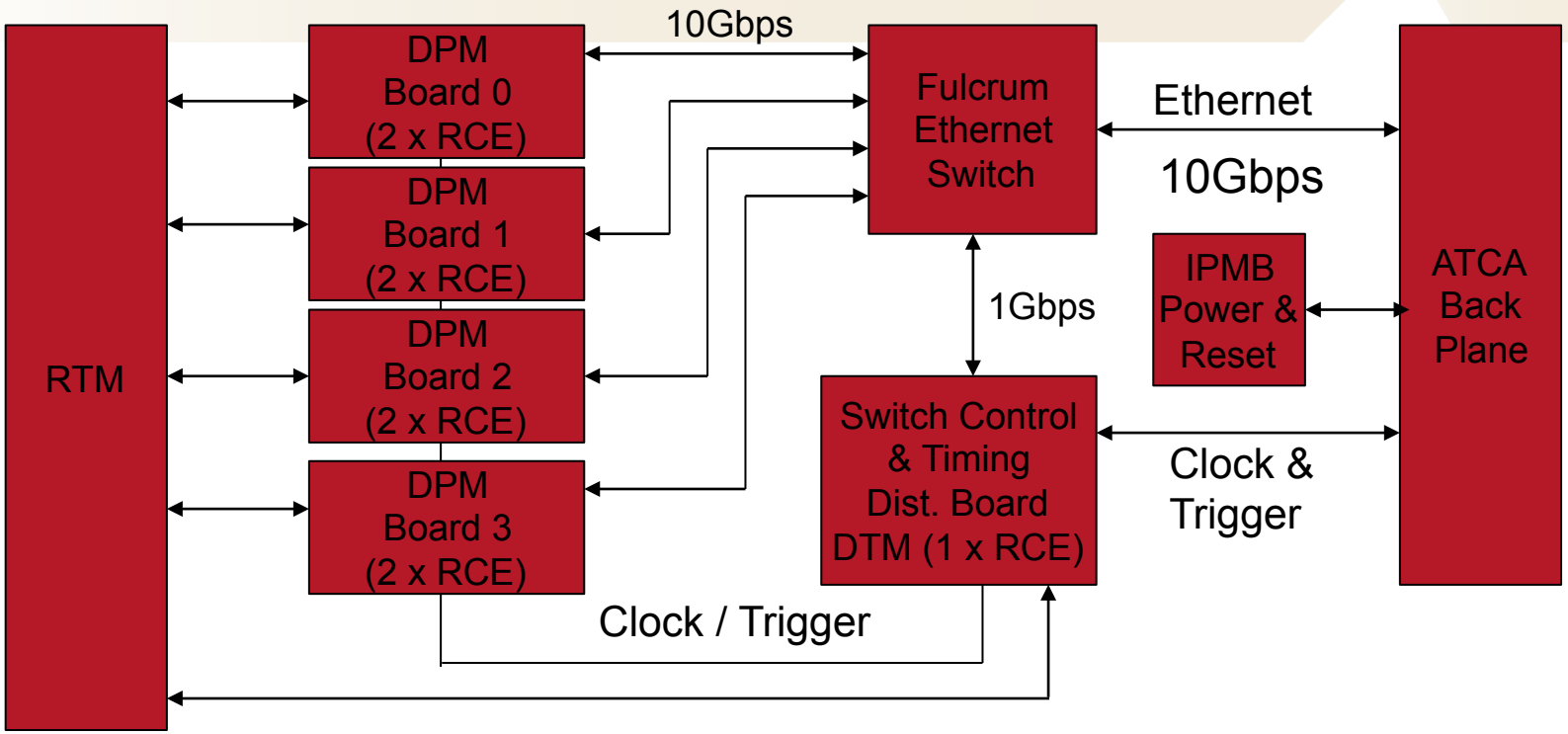
- But project is late compared to proposal
- Need significant contingency to cover electrical engineer labor continuing to Oct/Nov

Important key milestones coming up

- High speed tests with fully CODA integrated system
- Order of production front end boards

Backup

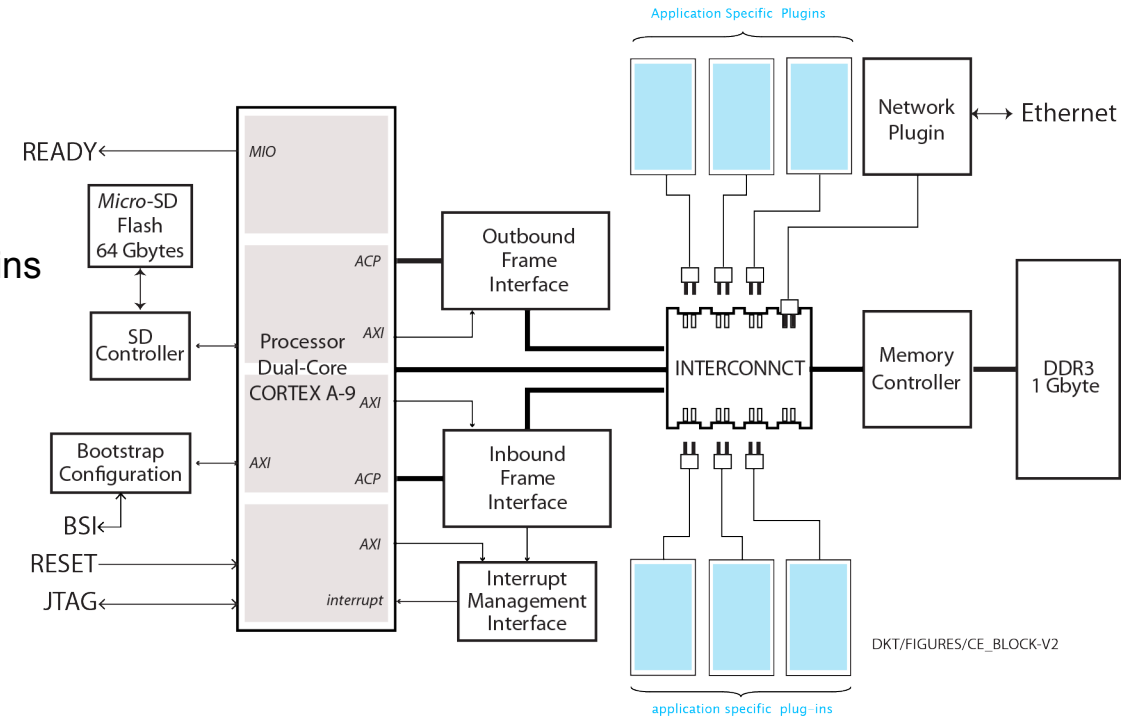
SLAC Gen3 COB (Cluster on Board)



- Supports 4 data processing FPGA mezzanine cards (DPM)
  - 2 RCE nodes per DPM
  - 12 bi-directional high speed links to/from RTM (GTP)
- Data transport module (DTM)
  - 1 RCE node
  - Interface to backplane clock & trigger lines & external trigger/clock source
  - 1 bi-directional high speed link to/from RTM (GTP)
  - 6 general purpose low speed pairs (12 single ended) to/from RTM
    - connected to general purpose pins on FPGA

RCE (Reconfigurable Cluster Element)

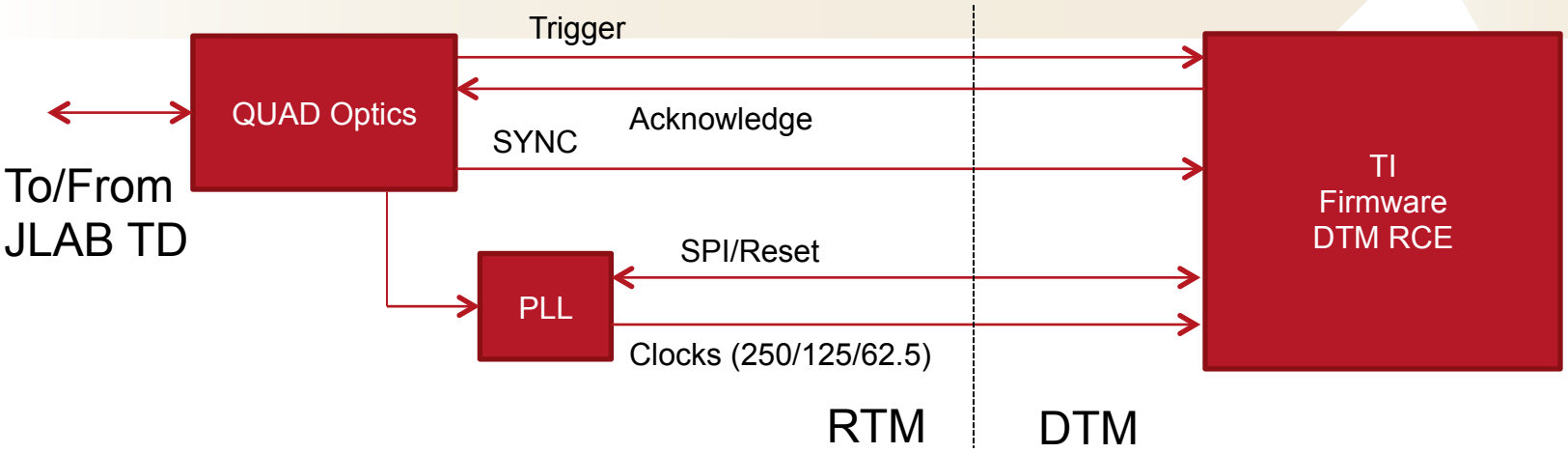
- Two versions
  - 2 x Zynq XC7Z045 FPGA for DPM
  - 1 x Zynq XC7Z030 FPGA for DTM
- ARM (dual-core) A-9 @ 900 MHZ
  - 1 Gbyte DDR3
  - Micro-SD (removable)
  - 10-GE MAC
- Bootstrap configuration via IPMI
- Frame based Socket Interface for plugins
  - 10Gbps bandwidth into memory
- Software (bundled with CE):
  - Linux
    - Based on 3 series kernel
    - Archlinux distribution
  - RTEMs
    - Open Source Real-Time kernel
    - POSIX compliant interfaces
  - TCP/IP stack
  - Plugin socket library
- External serial interfaces
  - 12 GTX channels per RCE (96 per COB)
  - Up to 10Gbps



SVT RCE Allocation

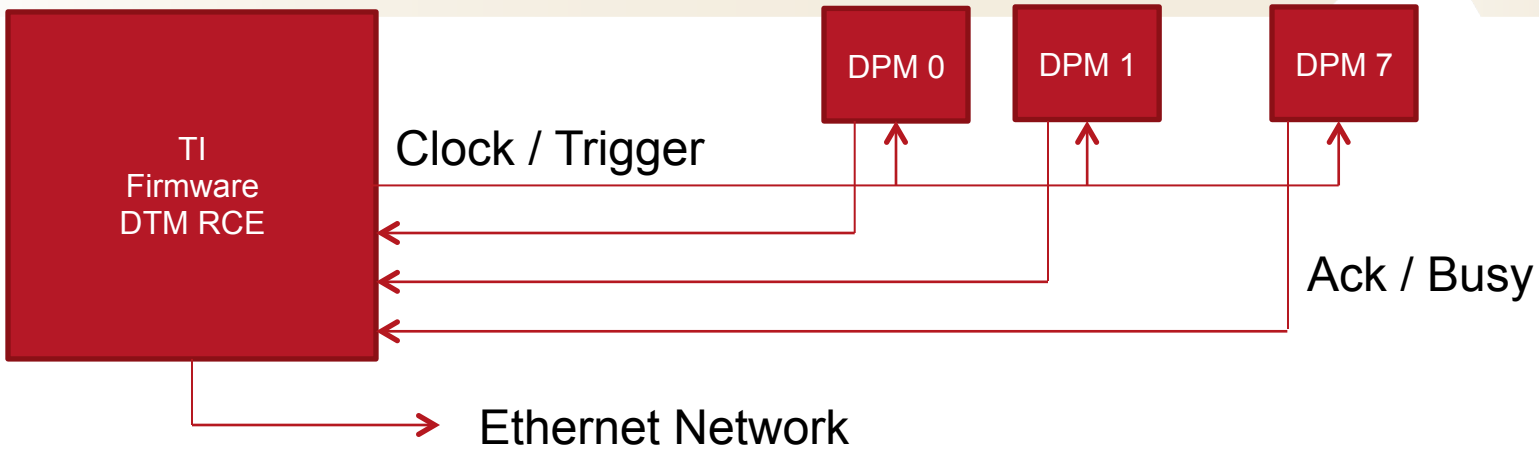
- Two COBs utilized in the SVT readout system
  - 16 RCEs On DPMs (2 per DPM, 4 DPMs per COB)
  - 2 RCEs on DTMs (1 per DTM, 1 DTM per COB)
- 7 RCEs on each COB process data from ½ SVT
  - 18 Hybrids total per COB
  - RCE 0 = 2 hybrids (layer 0)
  - RCE 1 = 2 hybrids (layer 1)
  - RCE 2 = 2 hybrids (layer 2)
  - RCE 3 = 3 hybrids (3 from layer 3)
  - RCE 4 = 3 hybrids (1 from layer 3 / 2 from layer 4)
  - RCE 5 = 3 hybrids (2 from layer 4 / 1 from layer 5)
  - RCE 6 = 3 hybrids (3 from layer 5)
- RCE 7 on COB 0 manages all 10 FE Boards
  - Configuration and status messages
  - Clock and trigger distribution to FE boards & hybrids
- RCE 7 on COB 1 has does not have an SVT specific purpose

SVT Trigger Interface



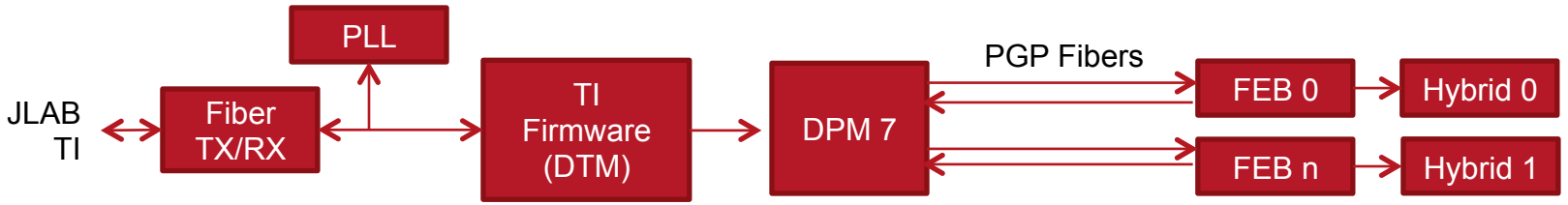
- Replicates portion of JLAB TI Board
- Quad optics and PLL exist on RTM
- TI firmware implemented in RCE FPGA
- Fully allocated available signals between RTM and DTM
  - 1 high speed pair for trigger & SYNC
  - 1 low speed pair for SYNC
  - 2 low speed pairs for PLL SPI and Reset signals
  - 3 low speed pairs for PLL generated clocks (250/125/62.5 Mhz)

SVT Trigger Distribution



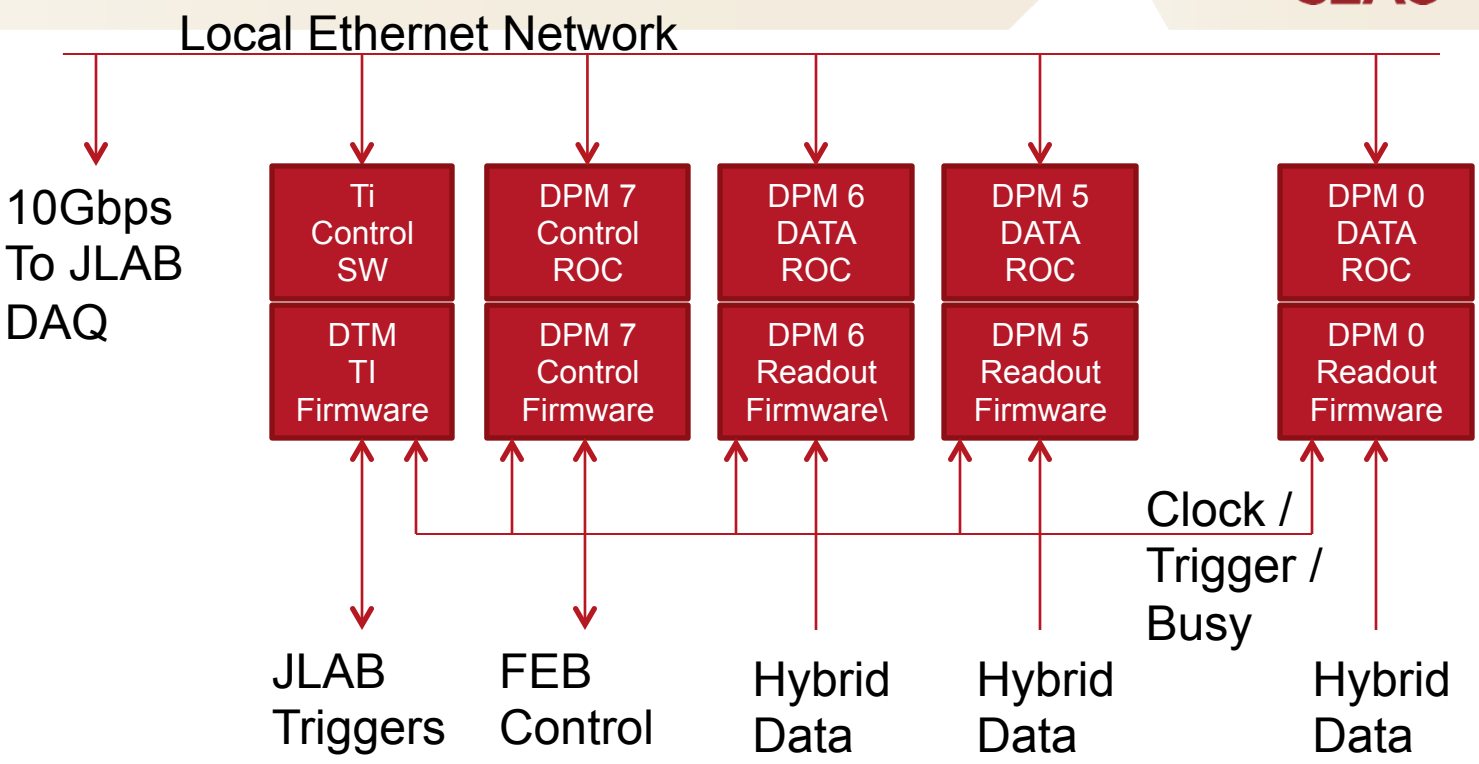
- DTM FPGA has ability to distribute clock and trigger to DPMs
  - Clock and trigger wired as fan out to DPMs
  - Individual feedback signals from each DPM
- 1 pair for clock fan out
- 1 pair for trigger fan out
  - 125Mhz serial protocol transfers 8-bit codes (easily expanded to longer words)
  - Used to distribute event codes to DPMs
    - System clock sync, APV25 sync & JLAB triggers
- 1 pair per DPM for feedback
  - Similar 8-bit op-code
  - Readout and trigger acknowledge
  - Busy
- Ethernet network used to distribute bulk trigger records to DPMs

Front End Timing Distribution



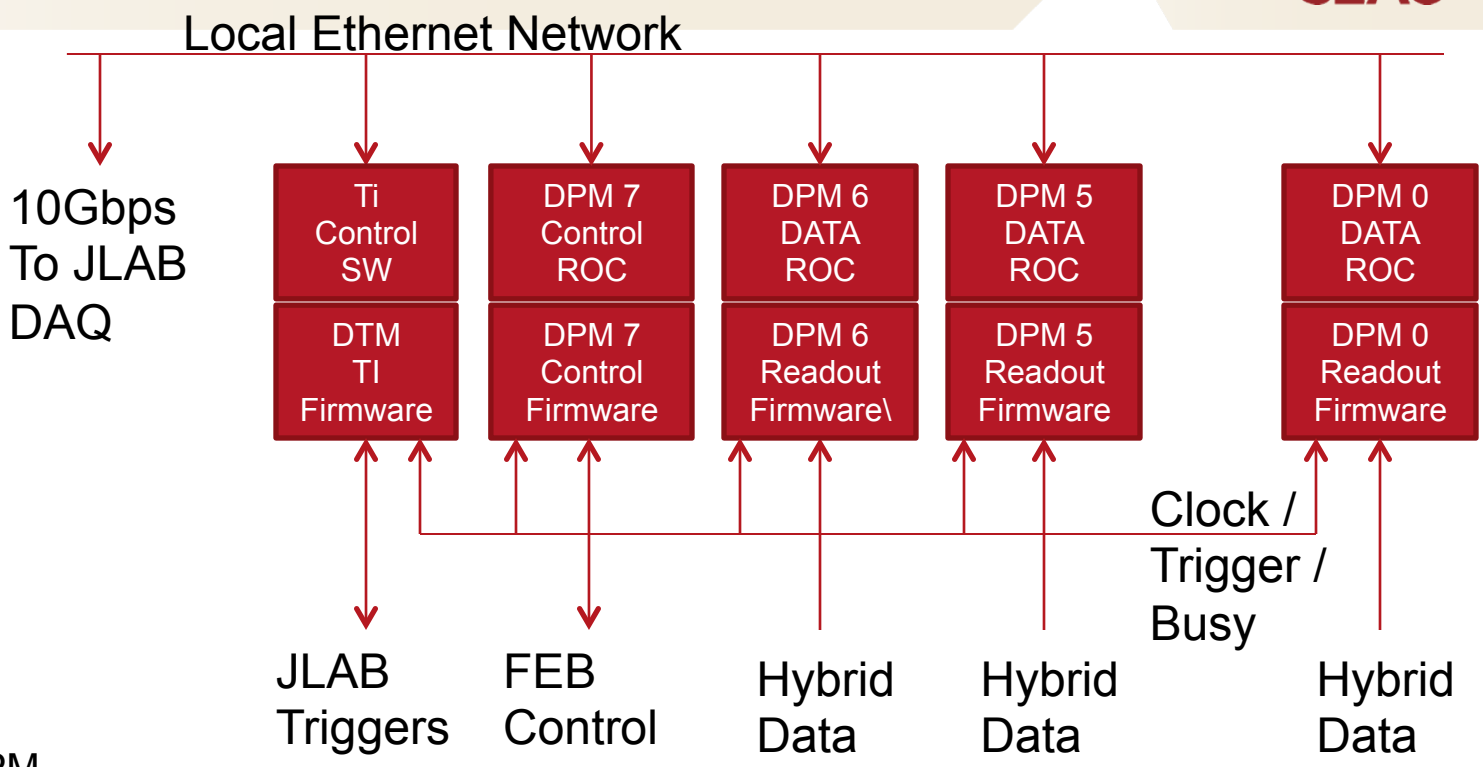
- Control DPM forwards timing information to front end boards over PGP
  - Clock encoded into serial data stream which the front end board recovers
  - Fixed latency path for encoded PLL reset and trigger signals
  - Upstream link echoes encoded clock and encoded signals back to DPM
  - Round trip latency is measured and compensated for by adjusting delay elements in DPM
    - Front end boards aligned in time domain

ROC Instances On SVT



- Data DPM
  - Data processing ROC application
  - Builds event record for 2 or 3 hybrids
    - APV25 ADC Data
    - Hybrid environmental data
  - Operates as slave when interfacing to TI firmware
  - Clock and trigger received over COB signals
  - Busy and acknowledge passed over COB signals
  - Trigger event data passed over Ethernet from TI control software

ROC Instances On SVT



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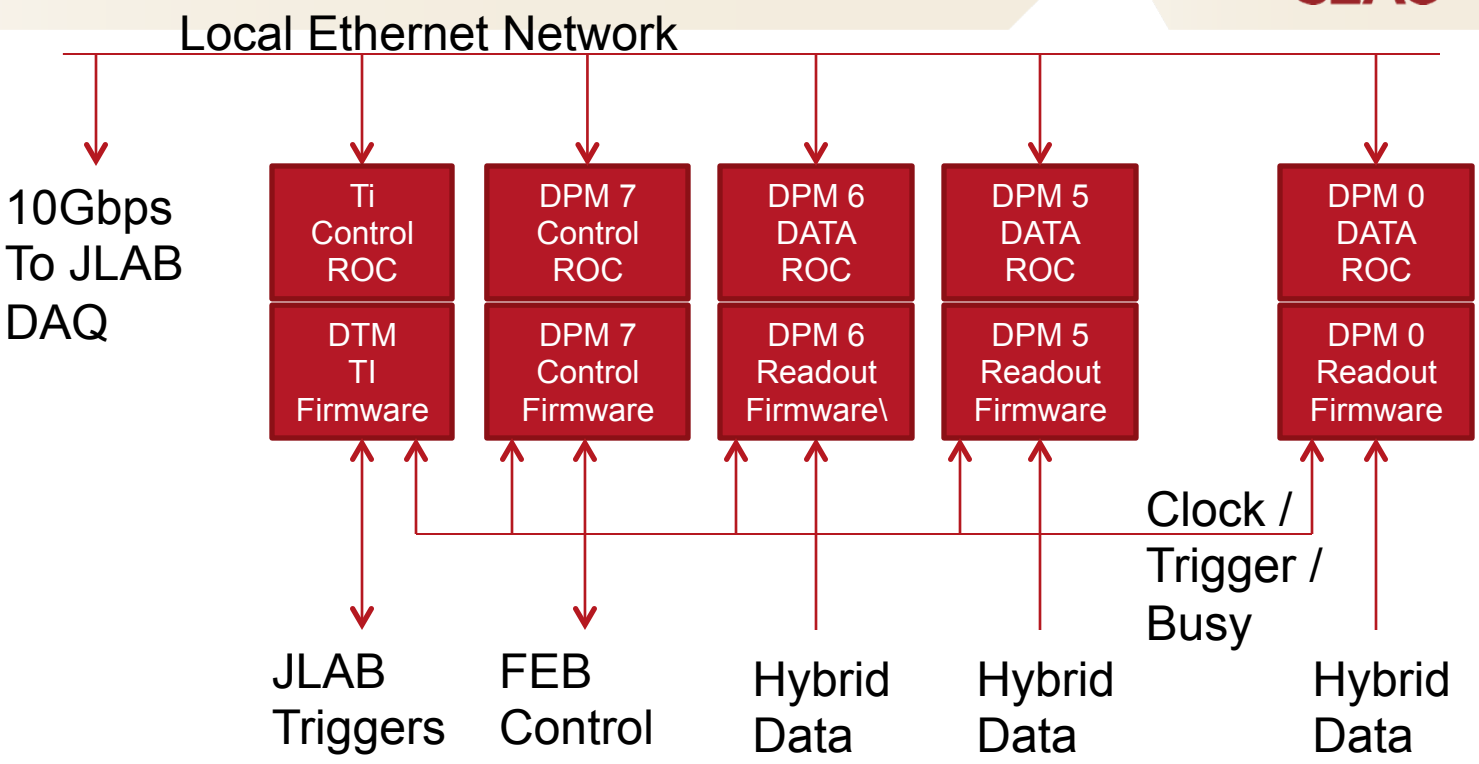
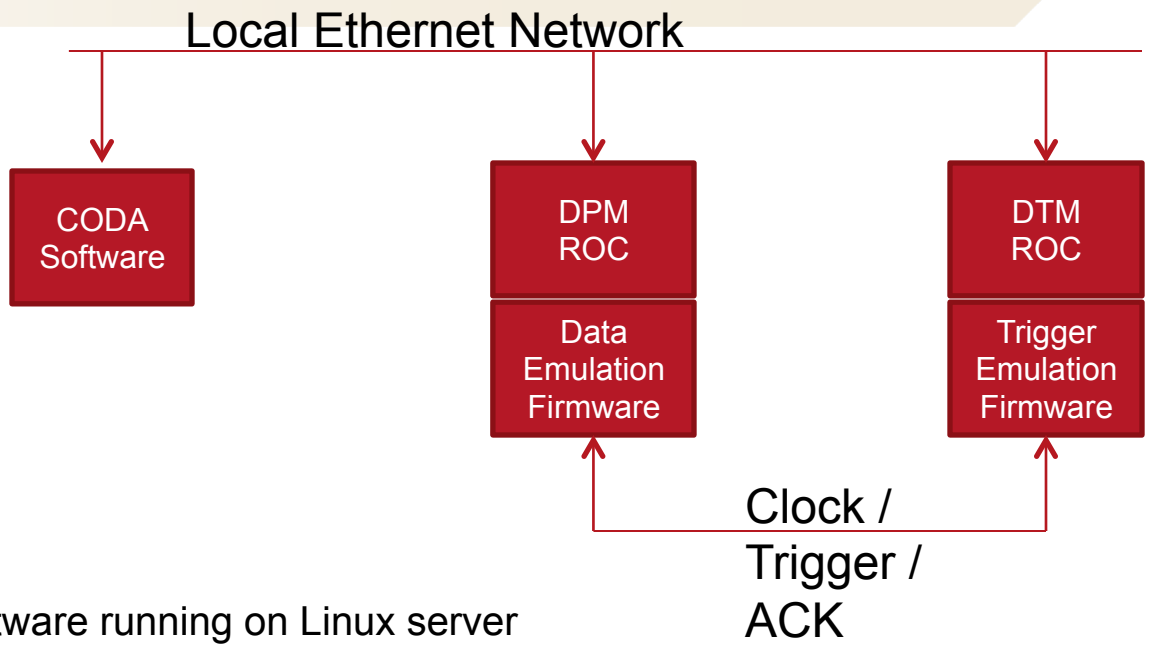
TI Control Software



- TI Control ROC
  - TI control and configuration
  - Formats trigger event data
  - Clock and trigger distributed over COB signals
  - Trigger event data passed over Ethernet to data and control DPMs

Trigger Rate Tests



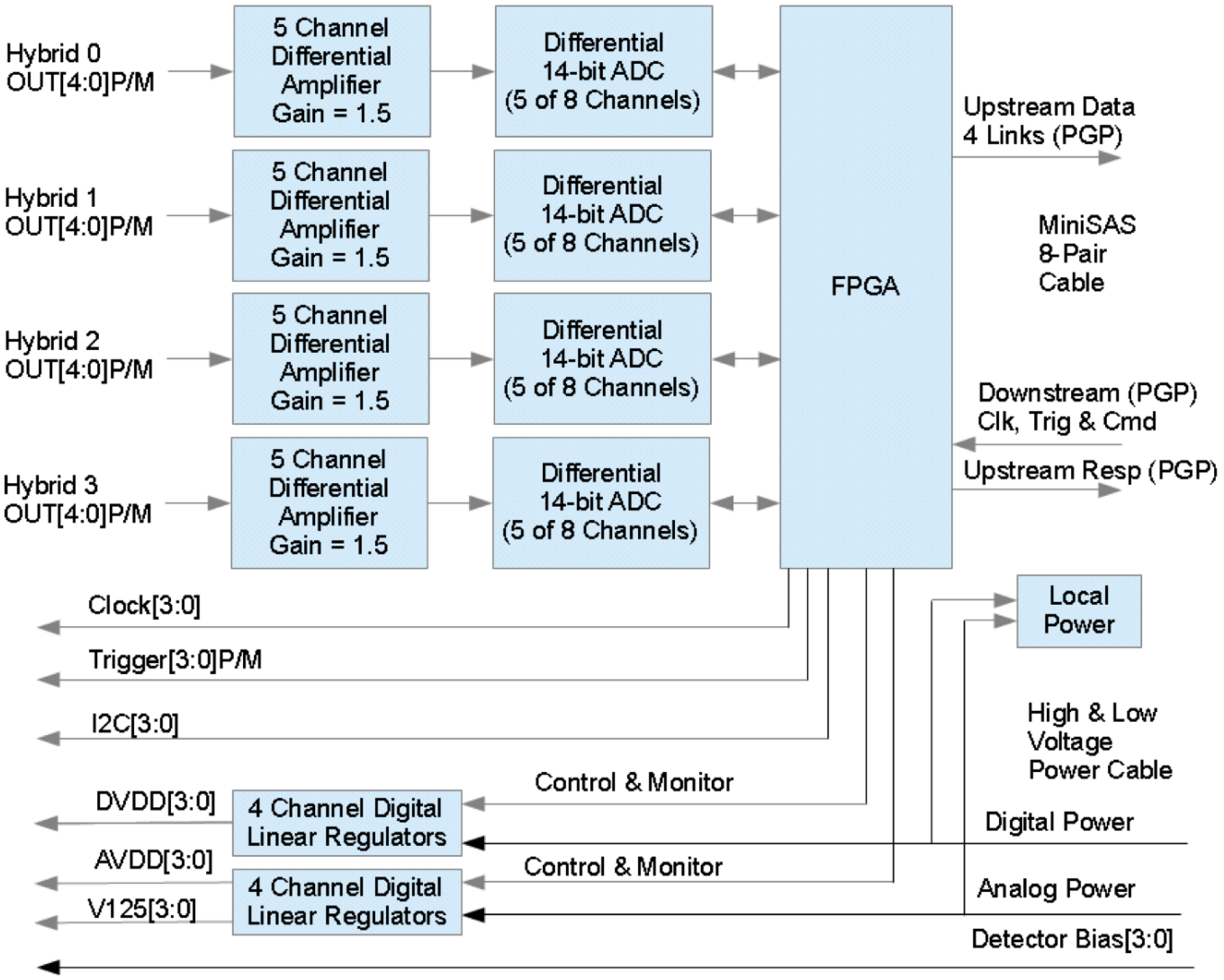
- CODA software running on Linux server
- DTM
  - Trigger emulation firmware
    - Generates triggers at defined rate
    - Configurable buffer depth
    - Distributes clock and trigger to DPM(s)
  - ROC software generates trigger emulation data
- DPM
  - Data emulation firmware triggered by DTM
  - Readout list accepts DMA data and passes it to CODA server
    - Configurable data sizes
  - DPM generates an ack per trigger to DTM

Trigger Rate Tests

- Status
  - CODA ROC software running on COB RCEs (thanks JLAB)
  - CODA software setup on Linux server
  - Successfully configured system with DTM & DPM
  - Readout attempted at low rates with small data sizes
  - Problems with readout even at low rates
    - Buffers fills up quickly
    - Most likely a problem in our configuration
    - Need some JLAB support
    - We got system running on Thursday
      - Not enough time to workout the bugs
    - We know this works. Something must be wrong in the setup!
    - Need another week or so go get rate data

FEB

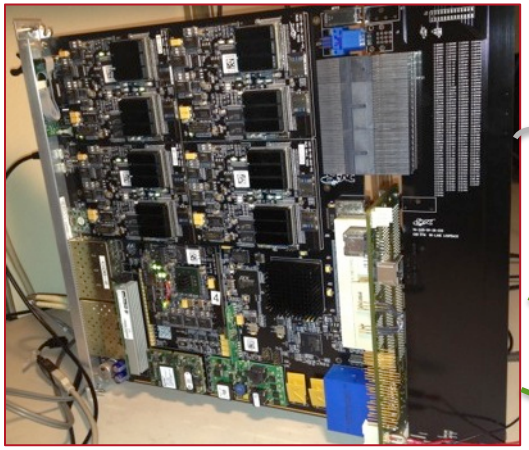
C


Hybrid 0
OUT[4:0]P/M
Hybrid 1
OUT[4:0]P/M
Hybrid 2
OUT[4:0]P/M
Hybrid 3
OUT[4:0]P/M
5 Channel Differential Amplifier Gain = 1.5
5 Channel Differential Amplifier Gain = 1.5
5 Channel Differential Amplifier Gain = 1.5
5 Channel Differential Amplifier Gain = 1.5
Differential 14-bit ADC (5 of 8 Channels)
Differential 14-bit ADC (5 of 8 Channels)
Differential 14-bit ADC (5 of 8 Channels)
Differential 14-bit ADC (5 of 8 Channels)
FPGA
Upstream Data 4 Links (PGP)
MiniSAS 8-Pair Cable
Downstream (PGP) Clk, Trig & Cmd
Upstream Resp (PGP)
Local Power
High & Low Voltage Power Cable
Clock[3:0]
Trigger[3:0]P/M
I2C[3:0]
Control & Monitor
Digital Power
Control & Monitor
Analog Power
Detector Bias[3:0]
DVDD[3:0]
AVDD[3:0]
V125[3:0]
4 Channel Digital Linear Regulators
4 Channel Digital Linear Regulators

SVT DAQ Reminder

SLAC

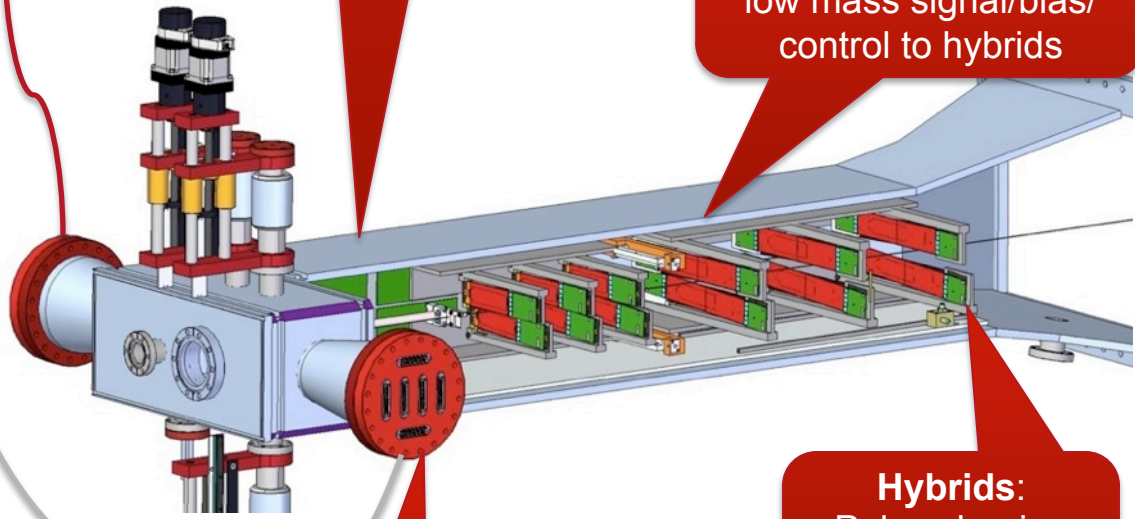
DAQ Platform
SLAC RCE (ATCA blade)



Power supplies
Low voltage
Sensor bias

FE boards:
Amplification
Analog to digital
Hybrid control/power

Flex cables:
Impedance controlled, low mass signal/bias/ control to hybrids

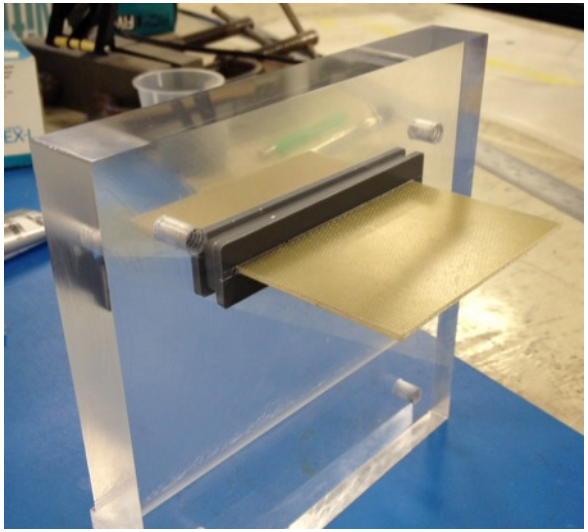


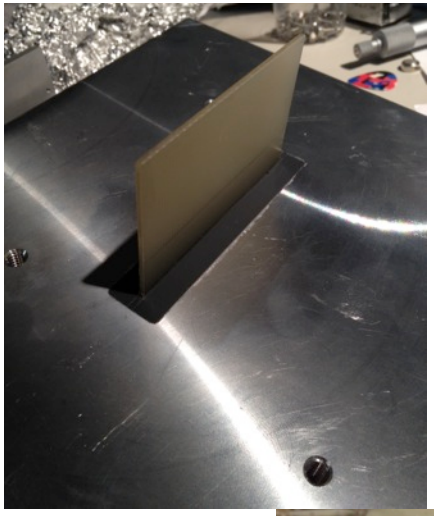
Hybrids:
Pulse shaping
Pulse sampling
Buffering

Flange boards:
Penetrate vacuum
Optical conversion for signals

JLab DAQ

Flange Boards Potting

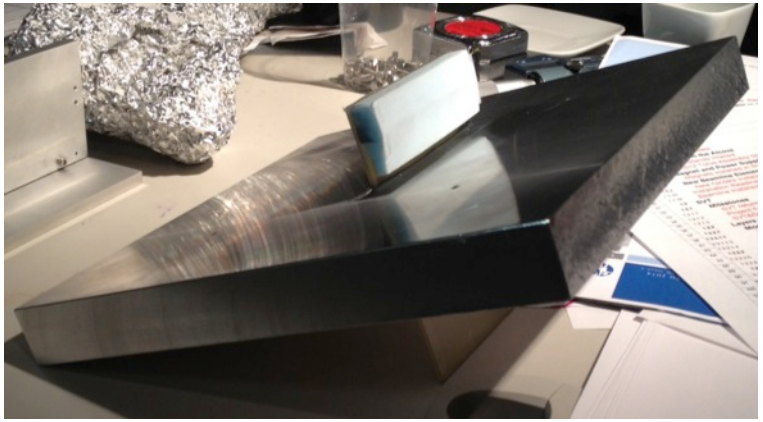


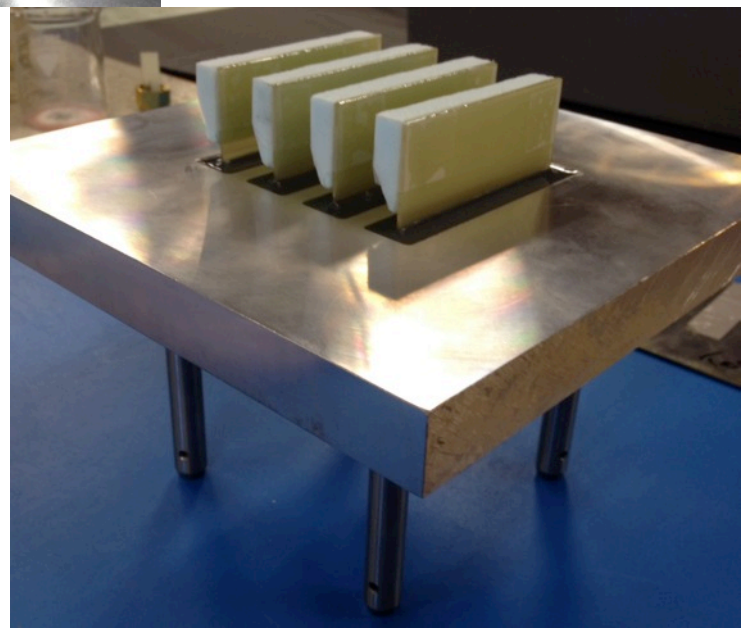


G10 dummy tests

- Single and four board using actual gluing fixtures
- Leak-checked to 9.1×10^{-10} Torr
- Glue and test real flange board next week

Actual vacuum flanges ready yesterday: ready for boards!





M. McCulloch

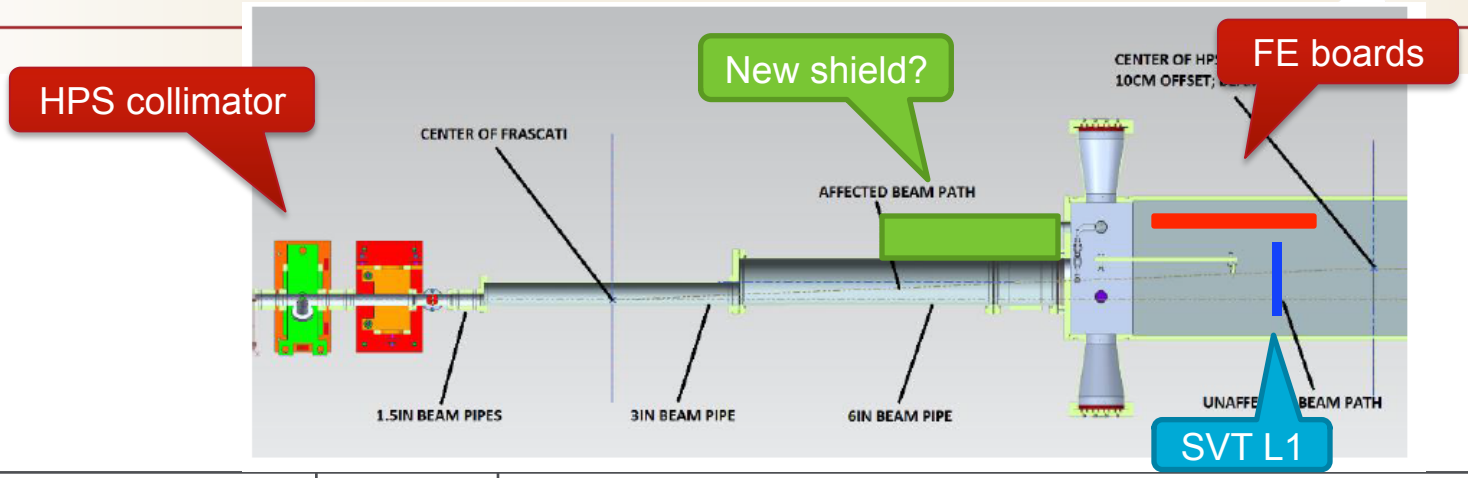
Experience from test run

SVT DAQ based on updates to successful Test run DAQ

- Mitigate test run issues
- Support additional 16 hybrids
- Improve performance

Test run issue	New DAQ
Large vacuum penetration count and long cable runs	• Digitize close to hybrids (inside vacuum) • Power distribution inside vacuum chamber • Optical conversion for reliability
ATCA crate power supply failure (radiation?)	• Optical conversion can place crate at arbitrary distance
Clock and trigger skews	• Per hybrid clock adjustments
Rate limited to ~<20kHz	• Use latest SLAC RCE platform • Support overlapping trigger/readout (“bursts”) on APV25 readout chip • Support multiple event buffer transfer on the JLab ROC application
Support for L4-6	• New hybrid w/ smaller physical footprint • Flex cables to optimize space and reliability

FE Board Radiation Environment Studies



Type	Worry?	Status
Neutron SEU in FPGA from target	No	FLUKA neutron production simulation/estimation. SEU normalized from BaBar results.
Neutron SEU in FPGA from vacuum chamber	No	
X-ray dose from target	No	Self shielding at low energy (6keV), too few high energy X-rays (70keV)
e^+e^- dose from halo scattering	Yes	100rad/month for assumed halo (10^{-5}), consider thick shielding (also to remove hadrons) to be conservative
X-ray dose from e^+e^- halo scattering	No	Not calculated, but much lower than e^+e^- dose (above), shielding should remove this background
Heavy ion power transistor damage	Not sure	Under investigation; estimate ion production (from neutrons), MOSFET gate rupture seems most dangerous(?)