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SVT DAQ Rate Testing

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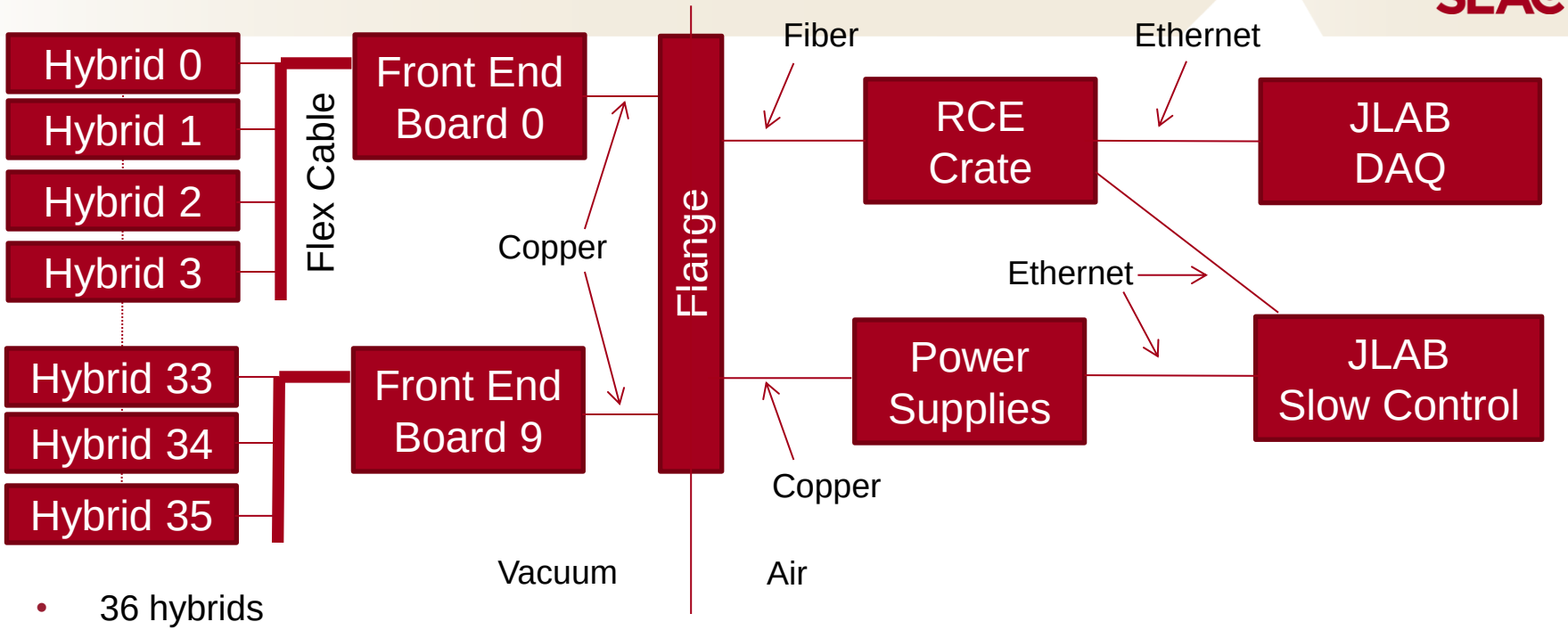
Overview

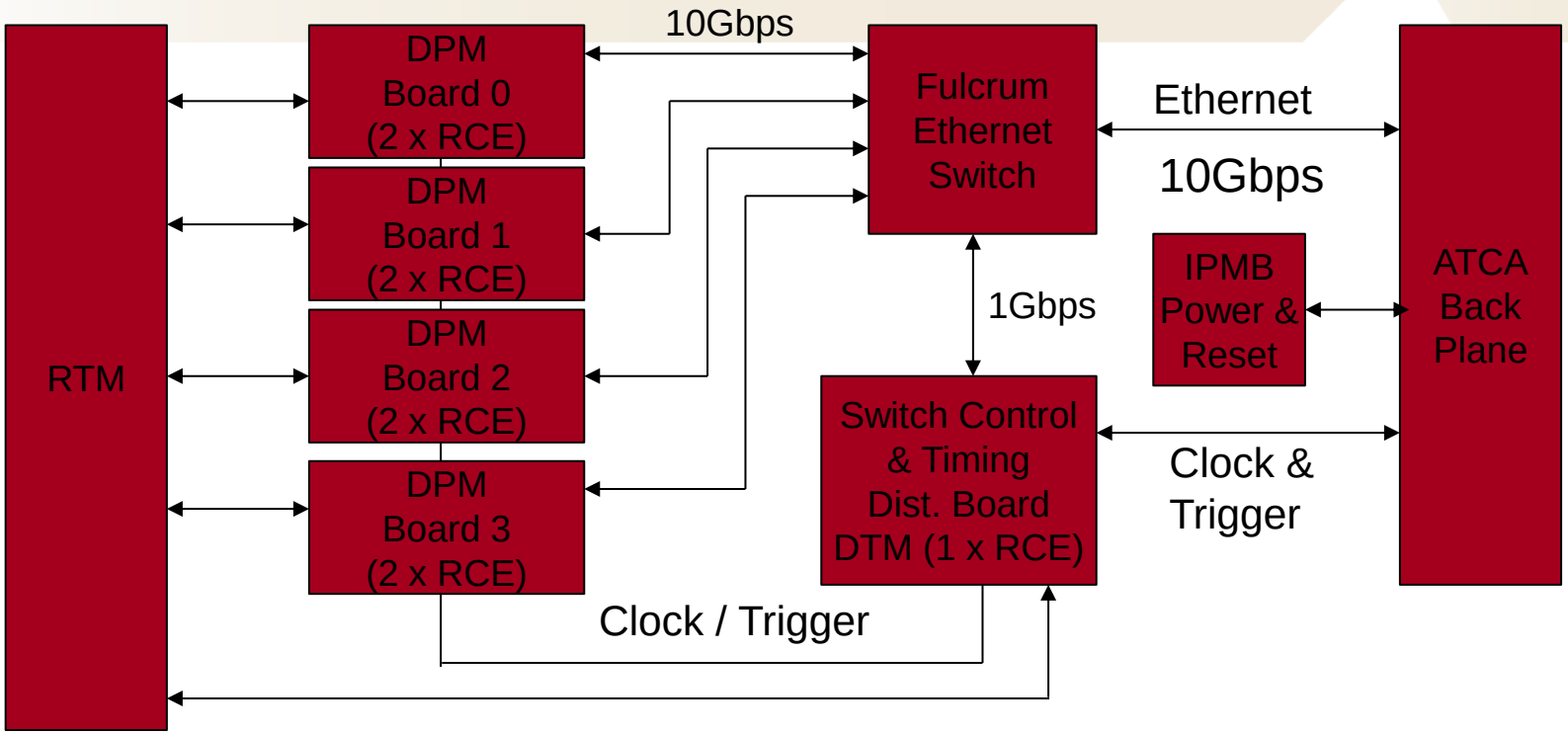
- SVT DAQ Overview
- Trigger Implementation in SVT
- Trigger distribution in SVT
- ROC Instances in SVT
- Data Rate Tests

SVT Overview



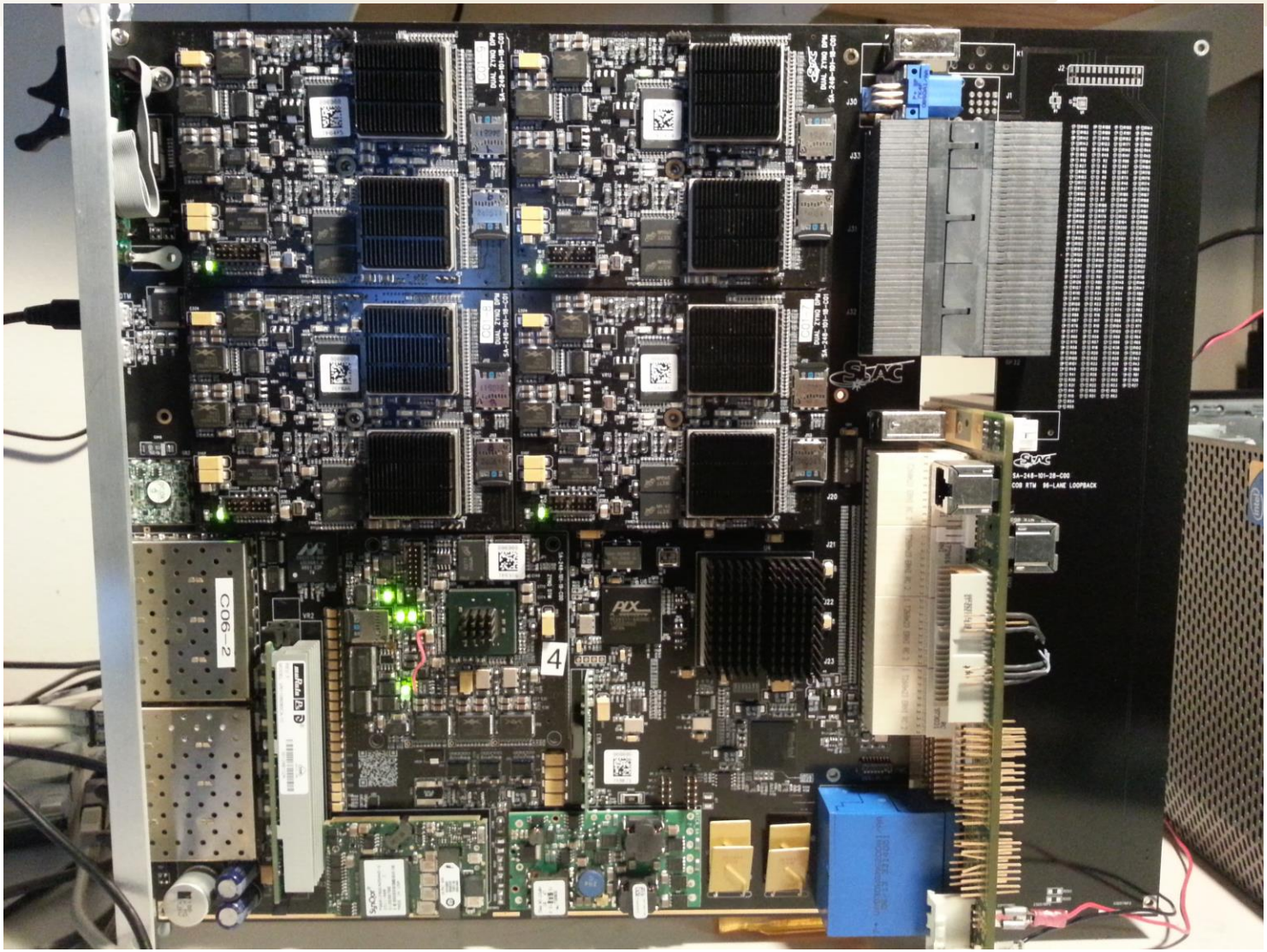
- 36 hybrids
  - 12 in layers 0 – 3 (4 per layer, 2 top, 2 bottom)
  - 24 in layers 4 – 6 (8 per layer, 4 top, 4 bottom)
  - 3.33Gbps raw ADC data per hybrid
- 10 front end boards
  - 4 servicing layers 1 – 3 with 3 hybrids per board
    - 10 Gbps raw ADC data per board
  - 6 servicing layers 4 – 6 with 4 hybrids per board
    - 13 Gbps raw ADC data per board
- RCE crate for event building and data reduction

SLAC Gen3 COB (Cluster on Board)



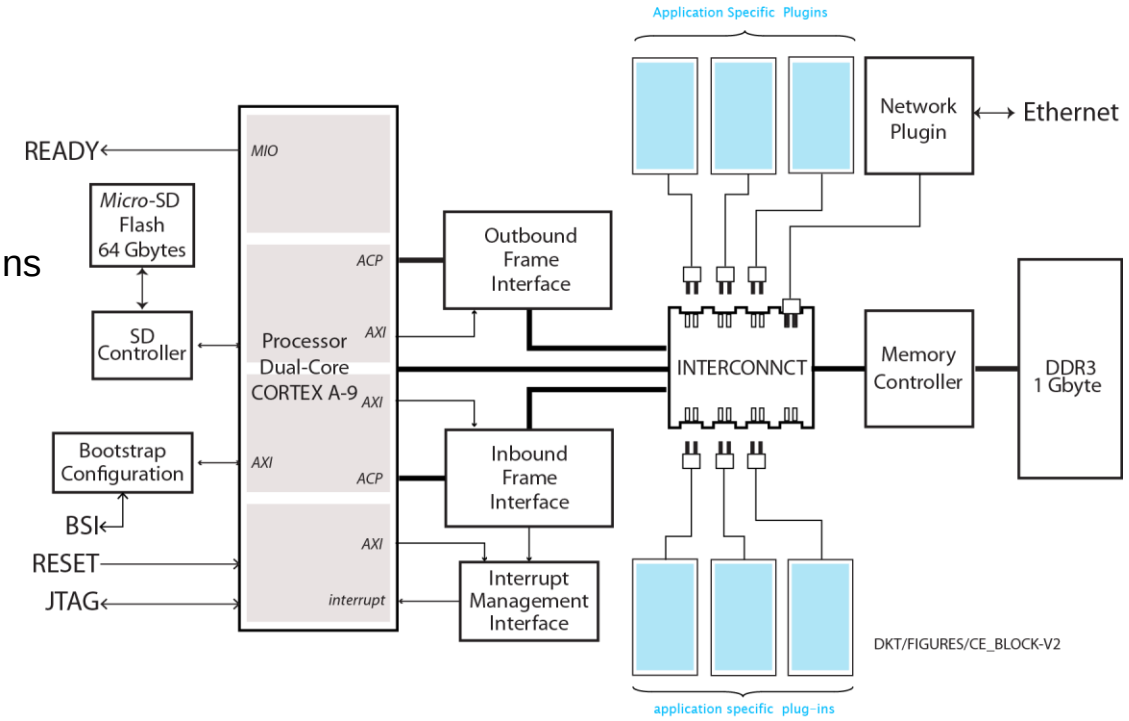
- Supports 4 data processing FPGA mezzanine cards (DPM)
  - 2 RCE nodes per DPM
  - 12 bi-directional high speed links to/from RTM (GTP)
- Data transport module (DTM)
  - 1 RCE node
  - Interface to backplane clock & trigger lines & external trigger/clock source
  - 1 bi-directional high speed link to/from RTM (GTP)
  - 6 general purpose low speed pairs (12 single ended) to/from RTM
    - connected to general purpose pins on FPGA

RCE GEN3 COB



RCE (Reconfigurable Cluster Element)

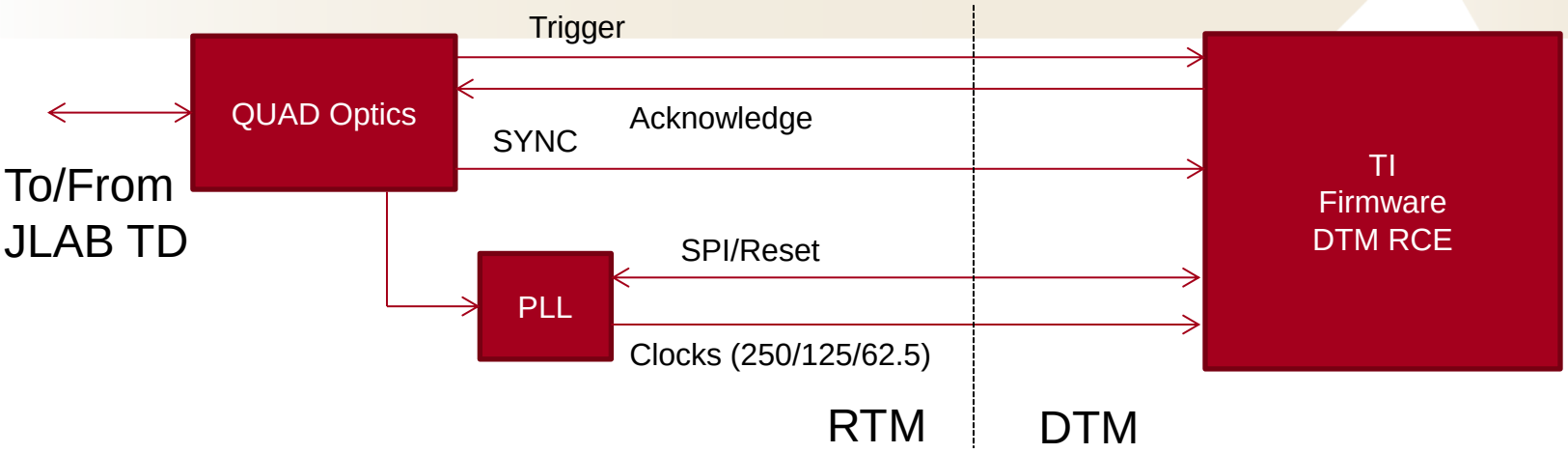
- Two versions
  - 2 x Zynq XC7Z045 FPGA for DPM
  - 1 x Zynq XC7Z030 FPGA for DTM
- ARM (dual-core) A-9 @ 900 MHZ
  - 1 Gbyte DDR3
  - Micro-SD (removable)
  - 10-GE MAC
- Bootstrap configuration via IPMI
- Frame based Socket Interface for plugins
  - 10Gbps bandwidth into memory
- Software (bundled with CE):
  - Linux
    - Based on 3 series kernel
    - Archlinux distribution
  - RTEMs
    - Open Source Real-Time kernel
    - POSIX compliant interfaces
  - TCP/IP stack
  - Plugin socket library
- External serial interfaces
  - 12 GTX channels per RCE (96 per COB)
  - Up to 10Gbps



SVT RCE Allocation

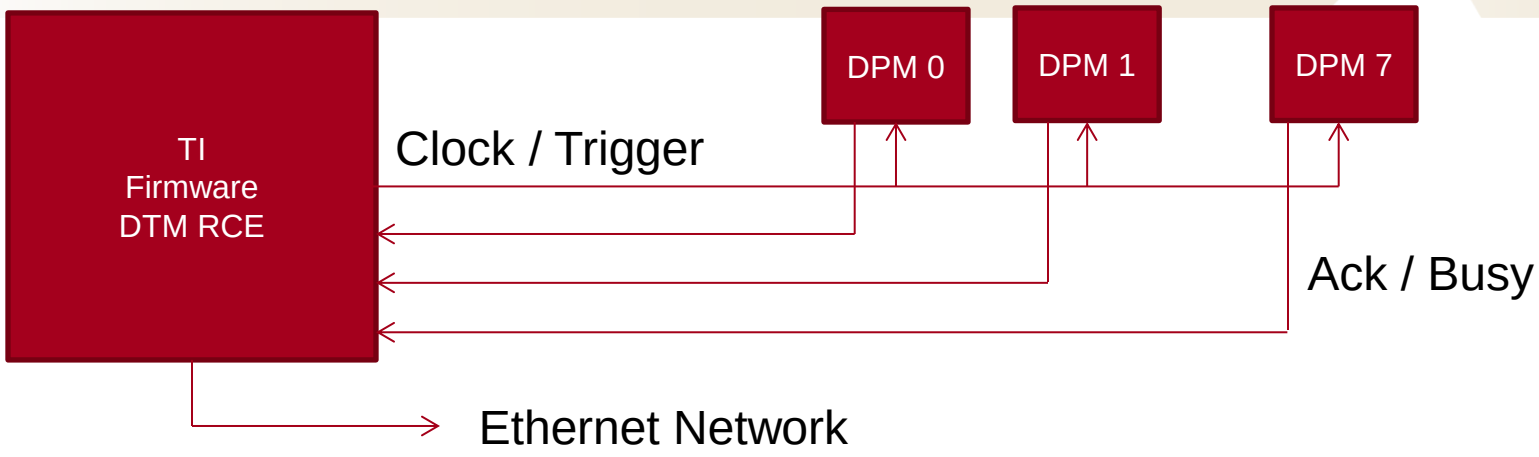
- Two COBs utilized in the SVT readout system
  - 16 RCEs On DPMs (2 per DPM, 4 DPMs per COB)
  - 2 RCEs on DTMs (1 per DTM, 1 DTM per COB)
- 7 RCEs on each COB process data from ½ SVT
  - 18 Hybrids total per COB
  - RCE 0 = 2 hybrids (layer 0)
  - RCE 1 = 2 hybrids (layer 1)
  - RCE 2 = 2 hybrids (layer 2)
  - RCE 3 = 3 hybrids (3 from layer 3)
  - RCE 4 = 3 hybrids (1 from layer 3 / 2 from layer 4)
  - RCE 5 = 3 hybrids (2 from layer 4 / 1 from layer 5)
  - RCE 6 = 3 hybrids (3 from layer 5)
- RCE 7 on COB 0 manages all 10 FE Boards
  - Configuration and status messages
  - Clock and trigger distribution to FE boards & hybrids
- RCE 7 on COB 1 has does not have an SVT specific purpose

SVT Trigger Interface



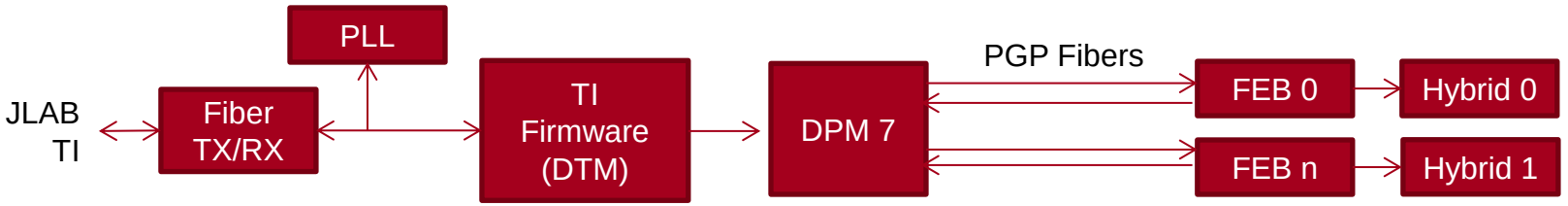
- Replicates portion of JLAB TI Board
- Quad optics and PLL exist on RTM
- TI firmware implemented in RCE FPGA
- Fully allocated available signals between RTM and DTM
  - 1 high speed pair for trigger & SYNC
  - 1 low speed pair for SYNC
  - 2 low speed pairs for PLL SPI and Reset signals
  - 3 low speed pairs for PLL generated clocks (250/125/62.5 Mhz)

SVT Trigger Distribution



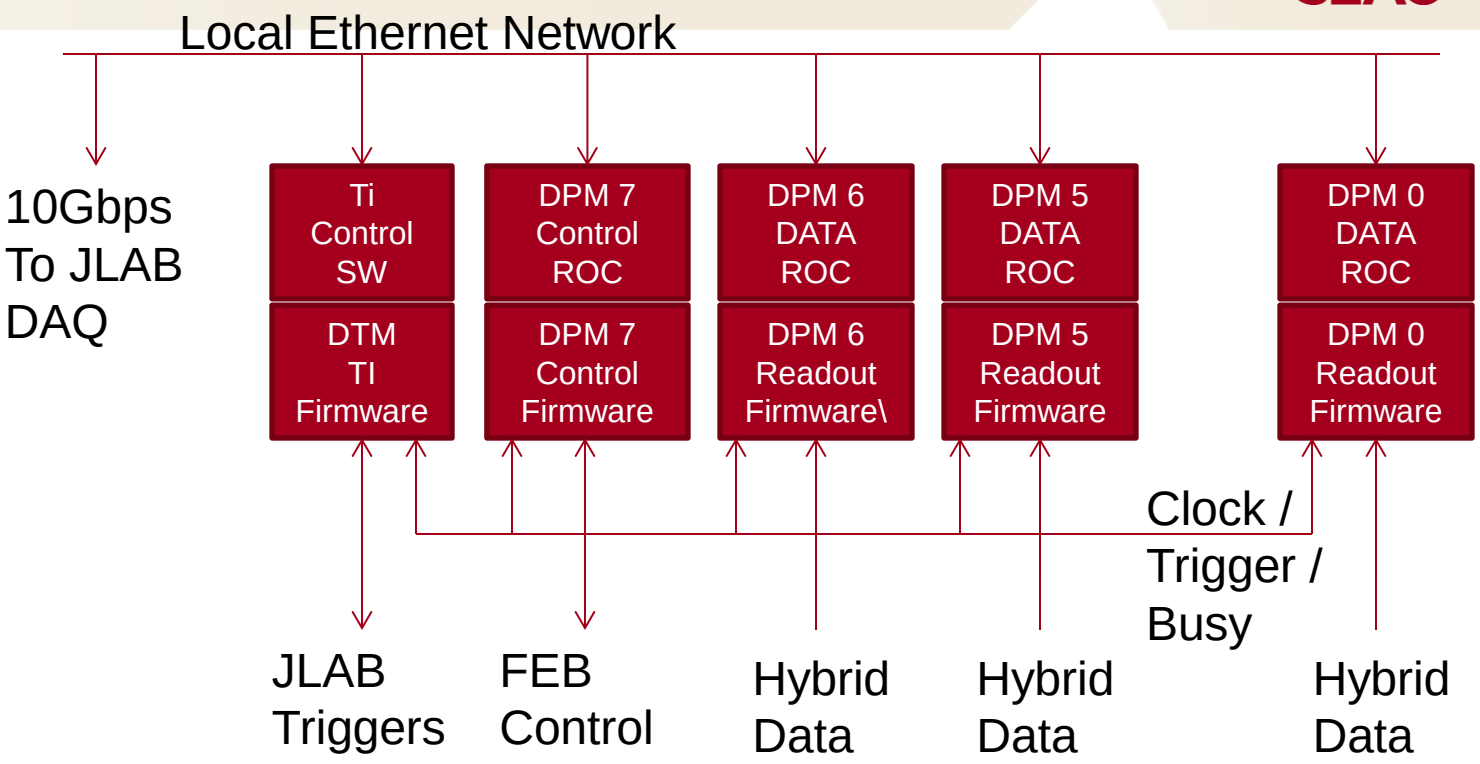
- DTM FPGA has ability to distribute clock and trigger to DPMs
  - Clock and trigger wired as fan out to DPMs
  - Individual feedback signals from each DPM
- 1 pair for clock fan out
- 1 pair for trigger fan out
  - 125Mhz serial protocol transfers 8-bit codes (easily expanded to longer words)
  - Used to distribute event codes to DPMs
    - System clock sync, APV25 sync & JLAB triggers
- 1 pair per DPM for feedback
  - Similar 8-bit op-code
  - Readout and trigger acknowledge
  - Busy
- Ethernet network used to distribute bulk trigger records to DPMs

Front End Timing Distribution



- Control DPM forwards timing information to front end boards over PGP
  - Clock encoded into serial data stream which the front end board recovers
  - Fixed latency path for encoded PLL reset and trigger signals
  - Upstream link echoes encoded clock and encoded signals back to DPM
  - Round trip latency is measured and compensated for by adjusting delay elements in DPM
    - Front end boards aligned in time domain

ROC Instances On SVT



- Data DPM
  - Data processing ROC application
  - Builds event record for 2 or 3 hybrids
    - APV25 ADC Data
    - Hybrid environmental data
  - Operates as slave when interfacing to TI firmware
  - Clock and trigger received over COB signals
  - Busy and acknowledge passed over COB signals
  - Trigger event data passed over Ethernet from TI control software

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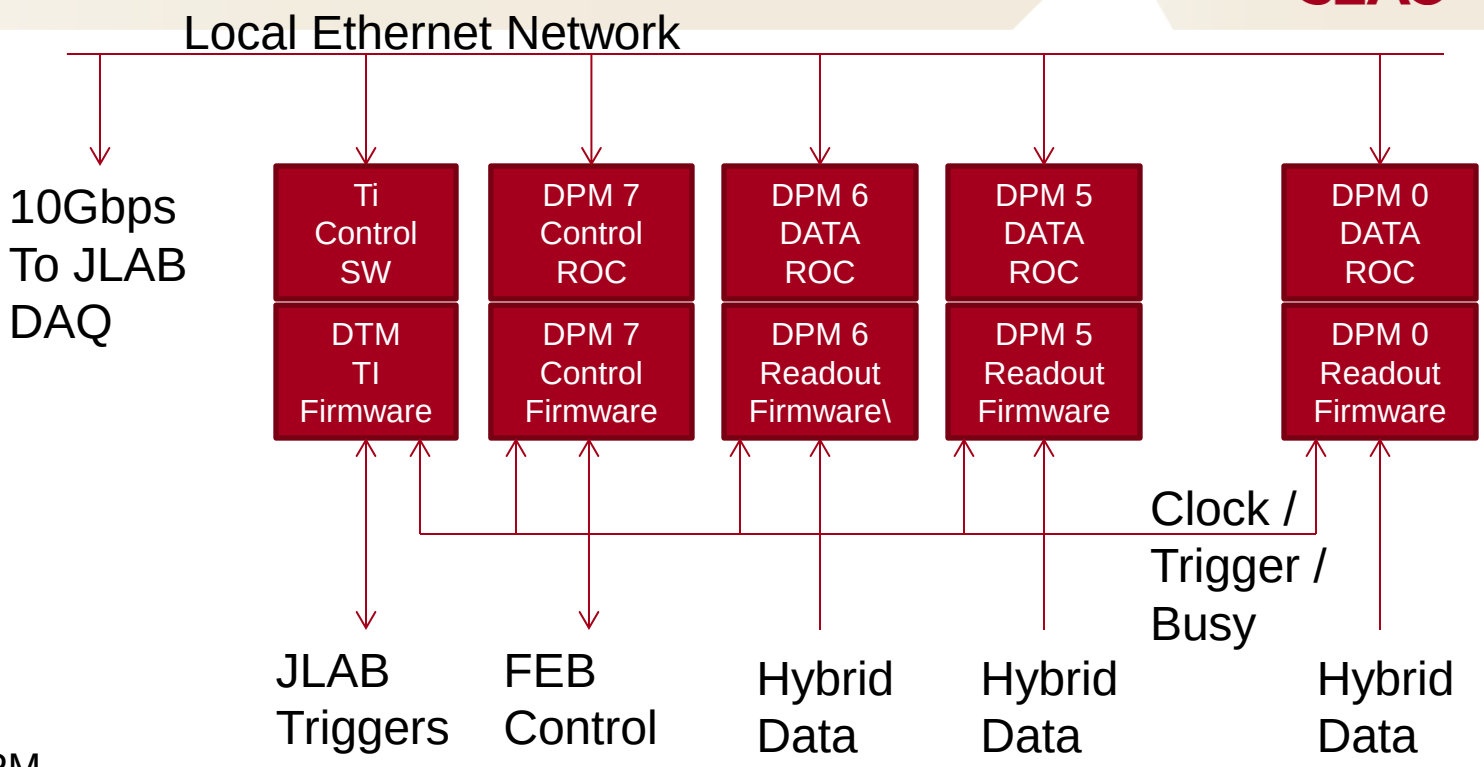

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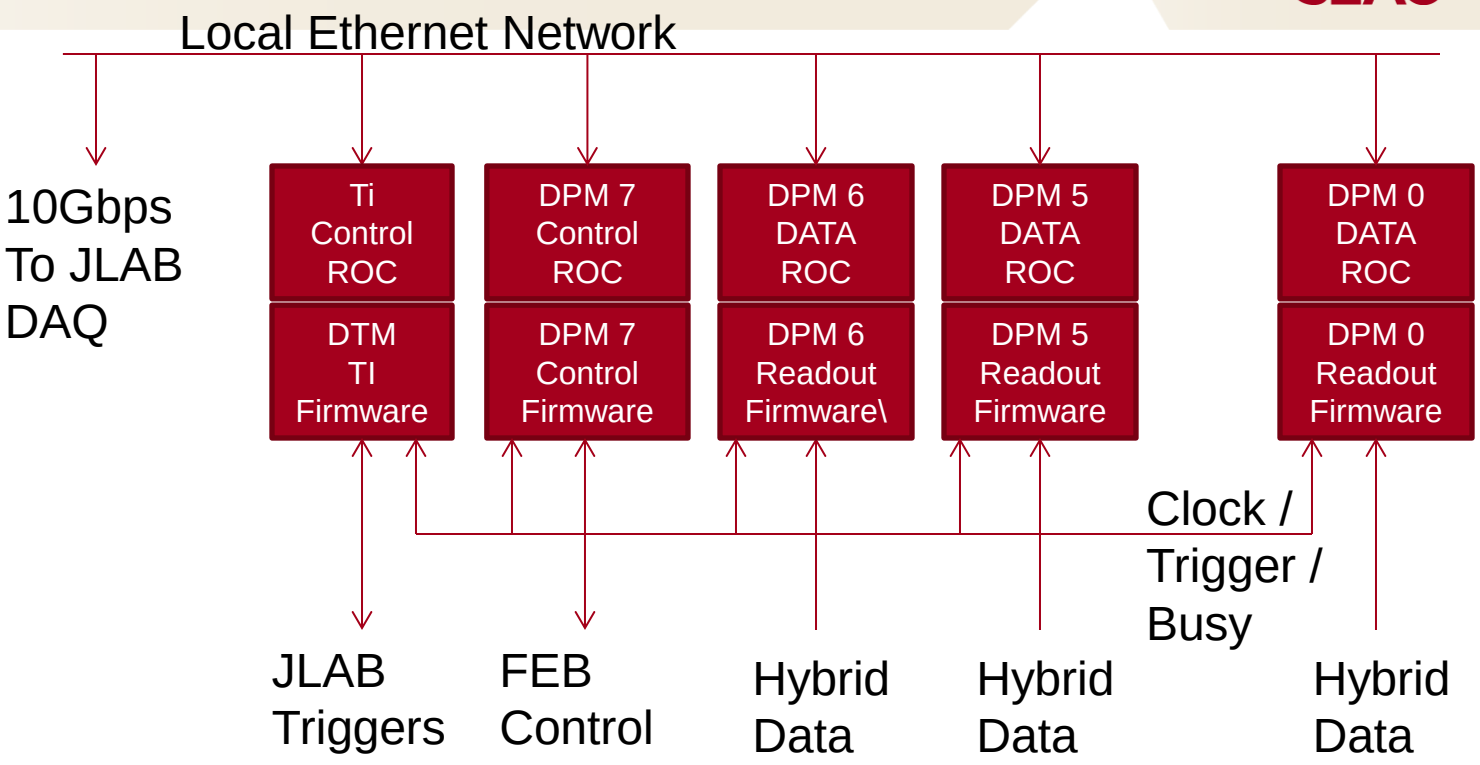
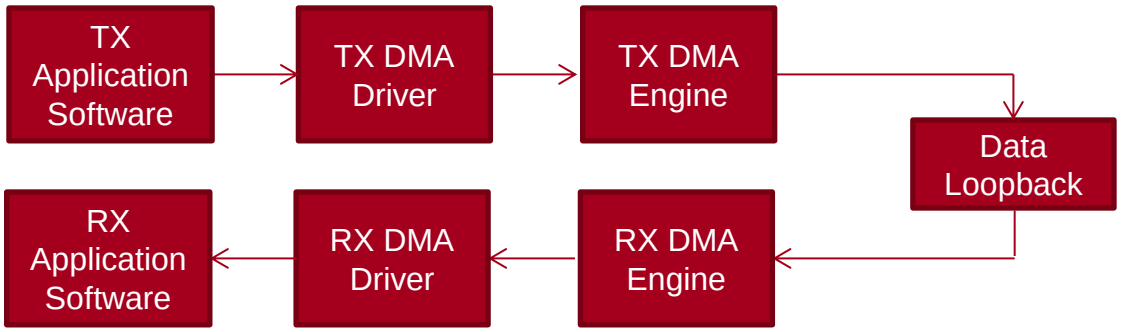
TI Control Software



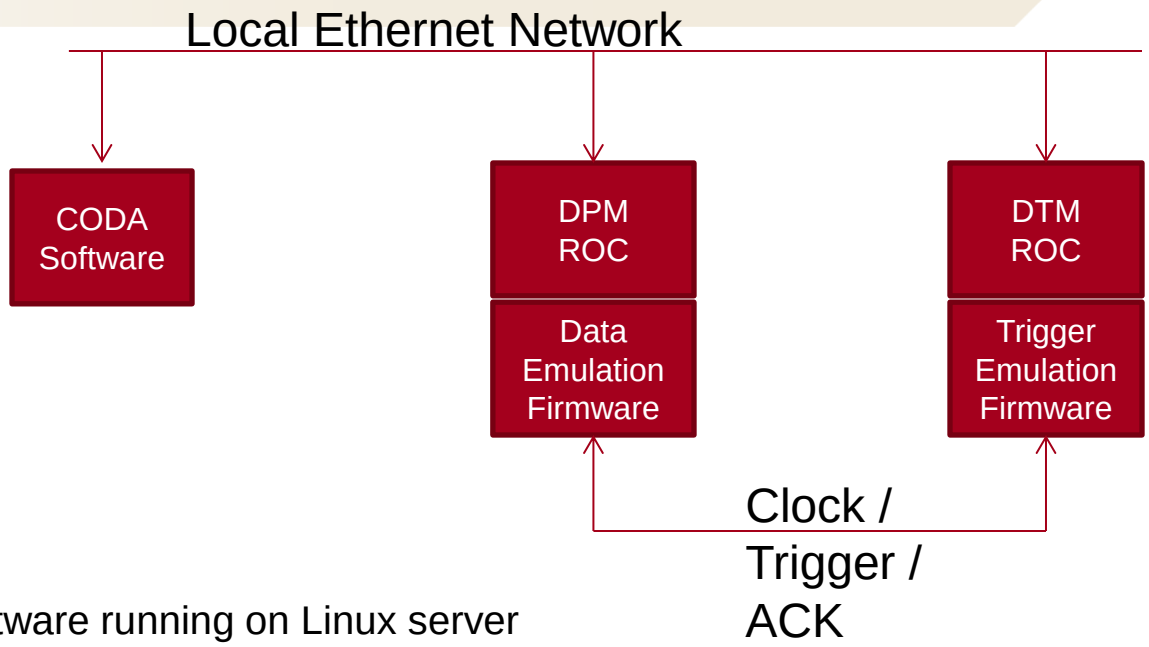
- TI Control ROC
  - TI control and configuration
  - Formats trigger event data
  - Clock and trigger distributed over COB signals
  - Trigger event data passed over Ethernet to data and control DPMs

DMA Rate Tests



- Polling based DMA engine
  - Firmware DMAs a frame at a time to pre-allocated kernel buffers
  - Linux kernel module driver with copy from kernel buffer to user space
- Transmit application generates fixed size data frames
  - Transmits as much data as possible while buffers are available
- Transmitted frames are looped back in firmware
- Receive application reads data and compares to transmitted pattern
- Testing included expected event sizes for single events as well as blocks of 40 events
  - Single event rate ~150Khz
  - 40 event block rate ~20 Khz (20khz * 40 events = 800Khz effective event rate)

CODA Based Trigger Rate Tests



- CODA software running on Linux server
- DTM
  - Trigger emulation firmware
    - Generates triggers at defined rate
    - Configurable buffer depth
    - Distributes clock and trigger to DPM(s)
  - ROC software generates trigger emulation data
- DPM
  - Data emulation firmware triggered by DTM
  - Readout list accepts DMA data and passes it to CODA server
    - Configurable data sizes
  - DPM generates acknowledged per trigger to DTM

CODA Based Trigger Rate Tests

SLAC

- Status
  - CODA ROC software running on COB RCEs (thanks JLAB)
  - CODA software setup on Linux server
  - Successfully configured system with DTM & DPM
    - Configure, Download, prestart, run states operational
  - Readout attempted at low rates with small data sizes
    - Ran into problems in our configuration
      - Need some JLAB support
    - System first run last Thursday
      - Not enough time to workout the bugs
    - Need another week or so go get data rate results
- Integration exercise planned for second week of August
  - Will take single COB with TI and 8 ROC nodes
  - Test both data integration at rate and TI interface