HPS DAQ Performance

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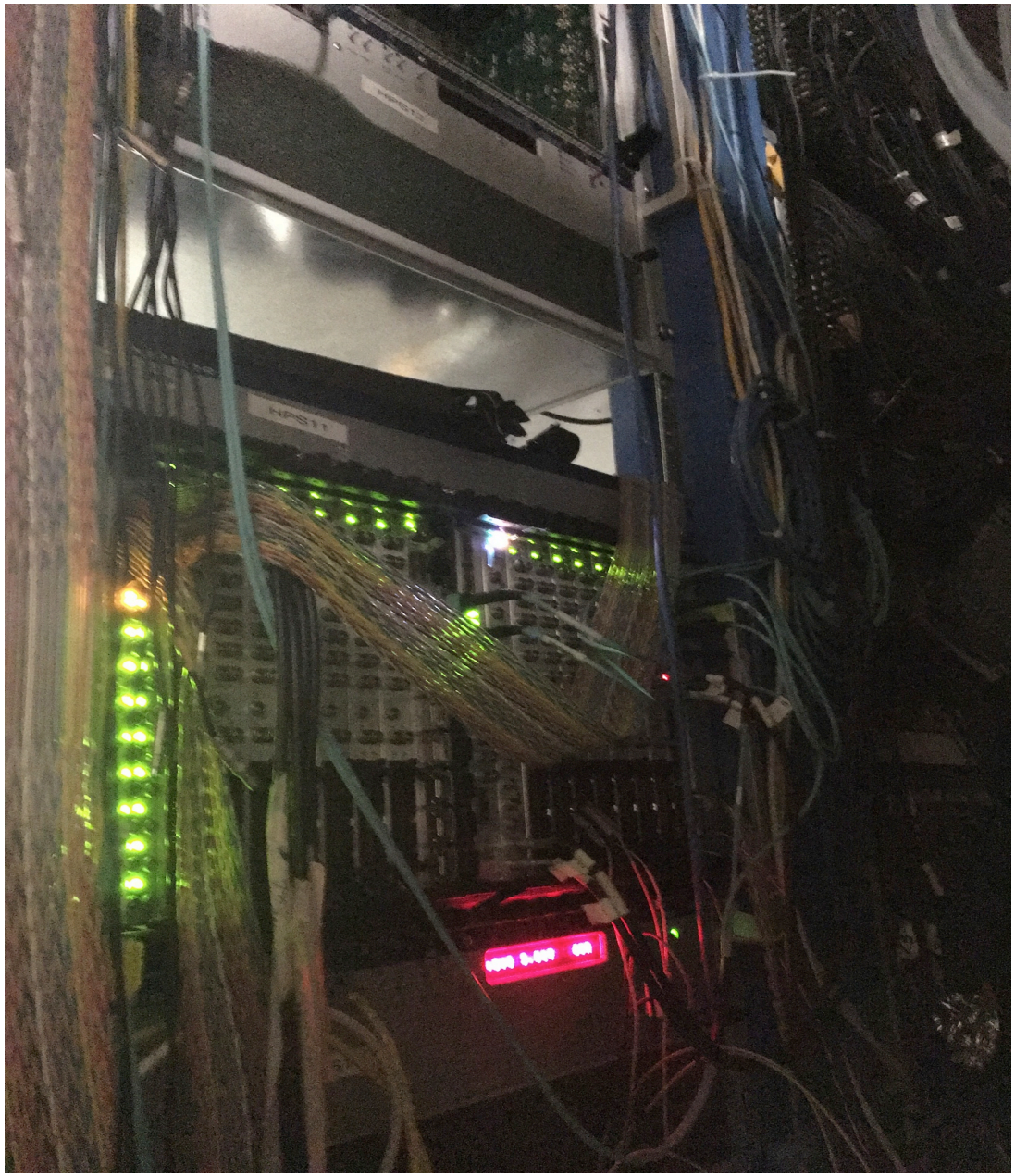
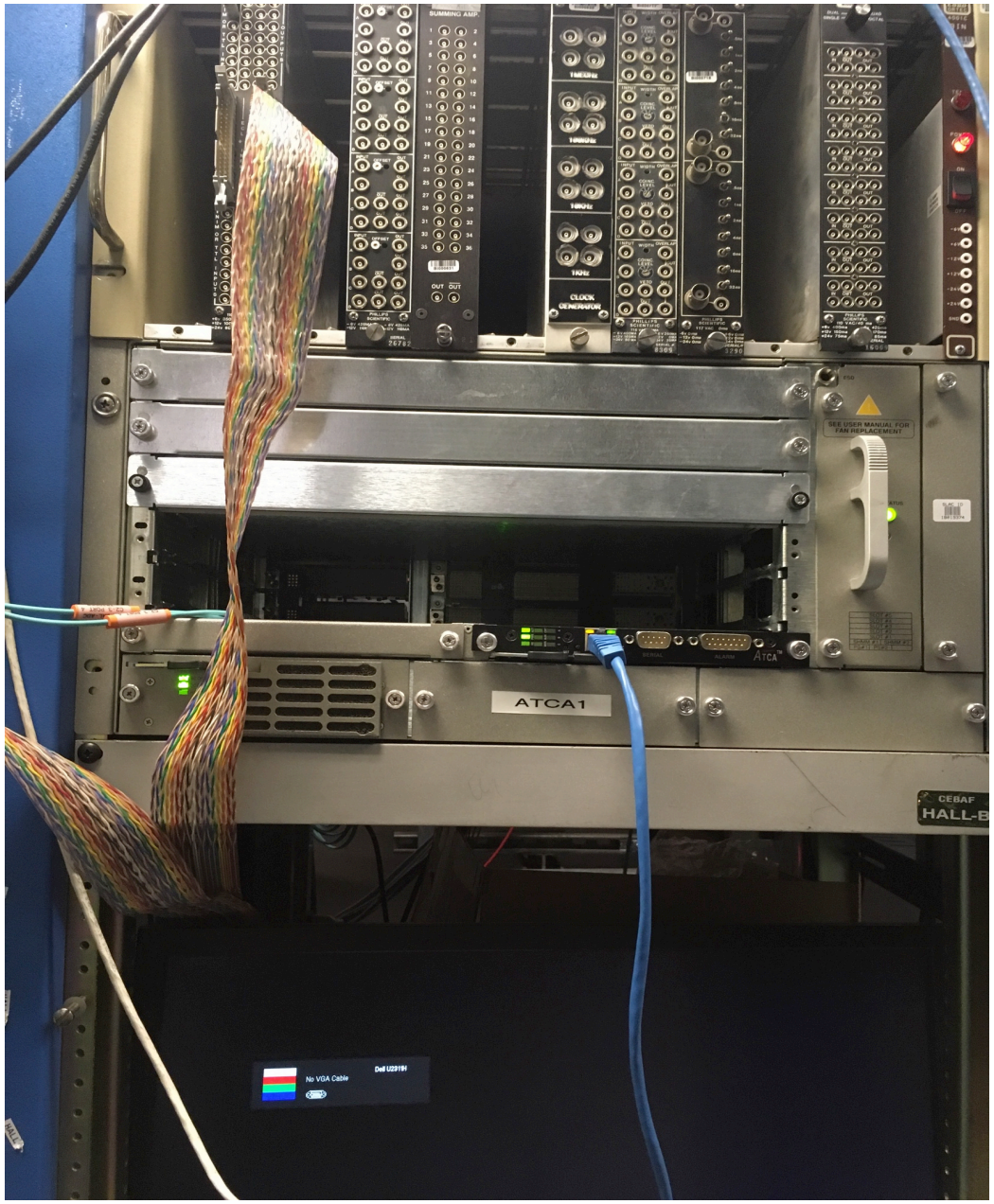
1. Electronics status
2. Last run experience
3. Possible upgrades

HPS DAQ Setup



FADC/Trigger electronics is operational, only 3 CPUs were relocated to CLAS12, can be installed if needed

HPS SVT ATCA crate



SVT ATCA crate is in place, readout blades were moved to SLAC for upgrade; when reinstalled, whole system will be ready for testing

DAQ: achieved performance

- 100kHz event rate - FADCs only
- 80kHz event rate – FADCs and TDCs
- 17kHz event rate – full system (FADCs+TDCs+SVT)
- 200MB/s data rate
- Livetime 90-92%
- Transfer to the tape: 146MB/sec/tape
- It was possible to increase livetime by decreasing holdoff parameters in trigger rules, but we decided to keep “conservative” settings to avoid possible beam time losses

DAQ: problems observed

- FADCs does not propagate busy condition, have to set it conservatively high
- Some reliability issues: crates ‘not connected’, end run fails, event builder crashes etc

DAQ improvements: computing and software

- Transfer to the tape: up to 800MByte/sec
- General performance improved using 64bit Linux and 40GBit network
- Network/computing is 100% ready, will be used by CLAS12 (and HPS)
- CODA DAQ software is improving, we are working on issues in CLAS12 as the number of components being increased (expect up to 100 readout controllers, HPS has 21)

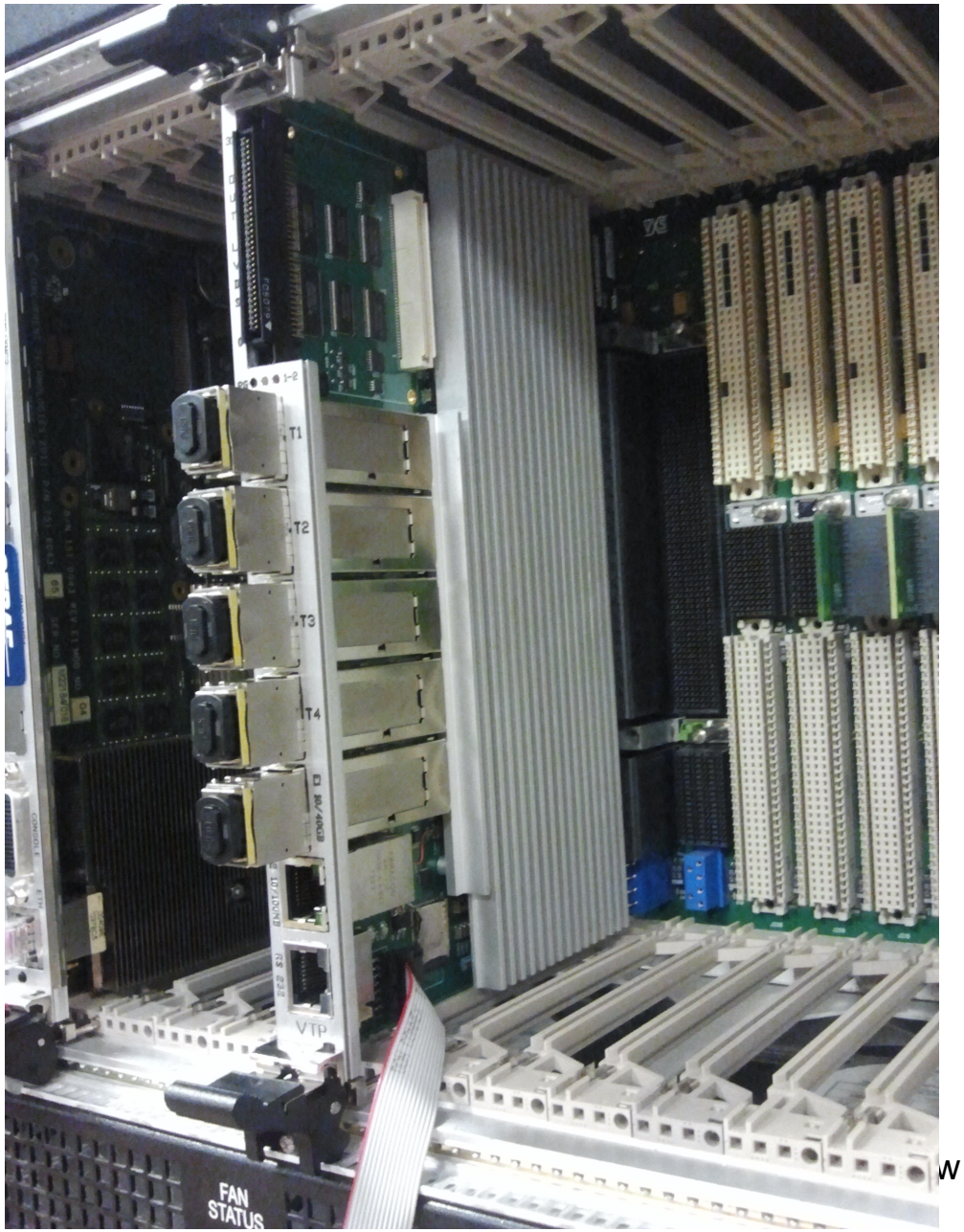
DAQ improvements: FADC firmware changes

- Trigger chain: auto continuous-calibrating pedestal subtraction (would eliminate the need to worry about beam current pedestal variations)
- Trigger chain: reduce FADC pulse walk-time in trigger (by using mode 7 time fit, rather than threshold crossing time)
- FADC busy is implemented, allowing Hall D to set rule 1 hold-off timer to 160ns and rule 4 to about 2 usec; will be used by CLAS12 and by HPS

DAQ improvements: GTP firmware changes

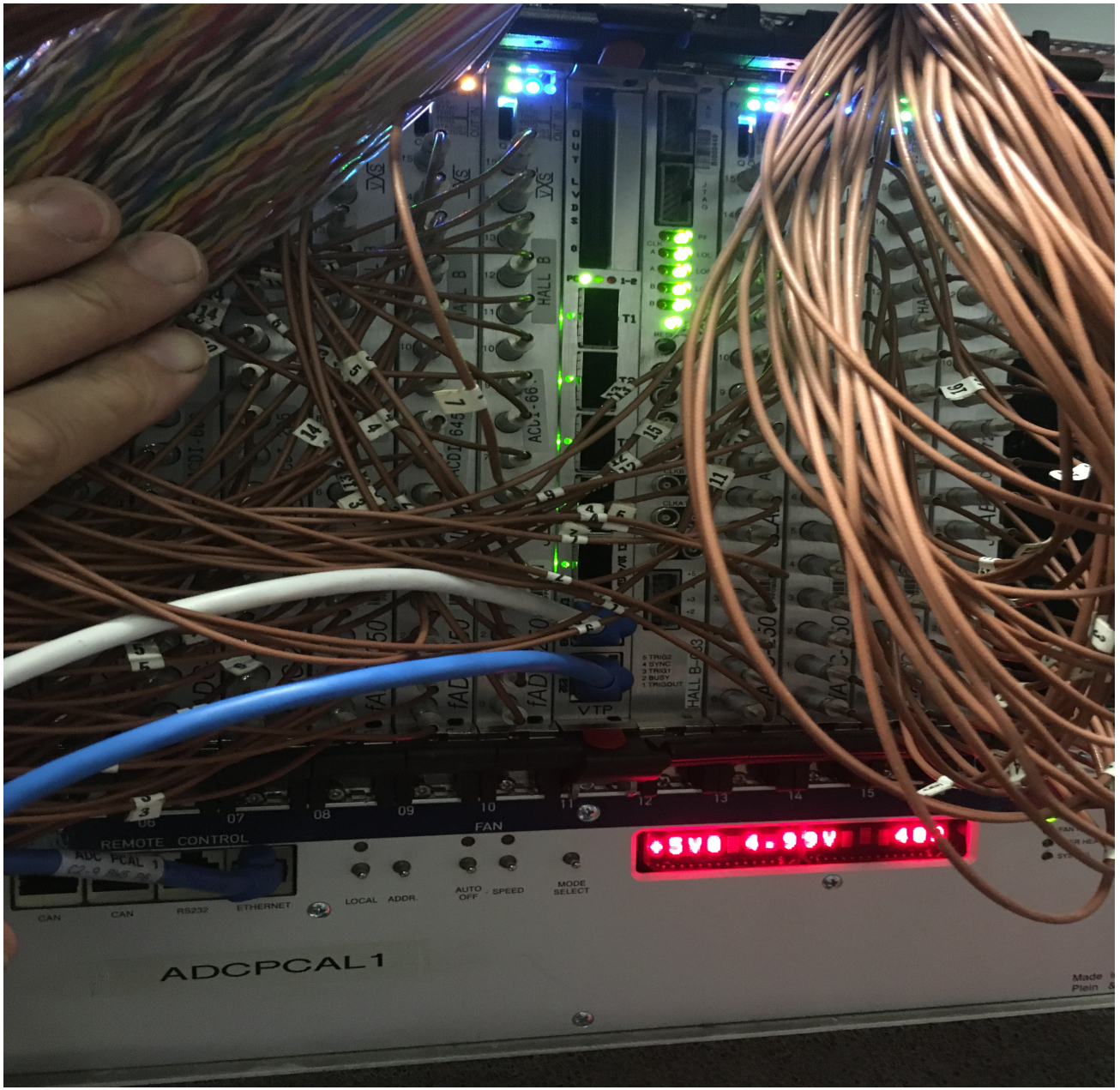
- Lower FADC pulse dead-time (currently ~32ns dead-time for each FADC channel when hit is seen) - could be made as low as ~8ns
- Can use new VTP board if needed

VTP (VXS Trigger Processor)



1. Four 5GBit links from each VXS slot (more bits for ADC integral, better timing resolution, possible use for readout)
2. 40GBit fiber uplinks (faster data transfer, connect several crates in parallel to form the trigger)
3. Big FPGA and 4GB memory
4. LVDS output to Trigger Supervisor, and custom IO card

VTP in adcpcal1 crate (CLAS12)



Conclusion

- After SVT reinstalled, HPS DAQ setup will be ready to run any time
- Recent CLAS12-related changes allows to improve performance and reliability, work continues as part of CLAS12 commissioning