Two Applications of Direct Digital Down Converters in Beam Diagnostics*

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Abstract. The technologies of direct digital down converters, digital frequency synthesis, and digital signal processing are being used in many commercial applications. Because of this commercialization, the component costs are being reduced to the point where they are economically viable for large scale accelerator applications. This paper will discuss two applications of these technologies to beam diagnostics. In the first application the combination of direct digital frequency synthesis and direct digital down converters are coupled with digital signal processor technology in order to maintain the stable gain environment required for a multi-electrode beam position monitoring system. This is done by injecting a CW reference signal into the electronics as part of the front-end circuitry. In the second application direct digital down converters are used to provide a novel approach to the measurement of beam intensity using cavity current monitors. In this system a pair of reference signals are injected into the cavity through an auxiliary port. The beam current is then calculated as the ratio of the beam signal divided by the average of the magnitude of the two reference signals.

INTRODUCTION

The technologies of digital down converters (DDC) and digital frequency synthesis (DDS) are coming into wide use in the telecommunications industry. Specifically the down converters produced by many manufacturers are designed for the cellular telephone market. Generally the chip set consists of a variable gain amplifier, a high speed 12 or 14 bit ADC, and digital down converter. Typically the parts are designed for conversion rates of 50 MHz to 65 MHz with sample apertures and jitters that allow the parts to be used at signal frequencies up to 300 MHz. They allow programmatic flexibility of frequency and bandwidth in the down conversion process. Because the down conversion process and filtering is digital, it is inherently linear.

The function of a DDC is that of a digital I/Q demodulator with a programmable frequency. A block diagram of the device is shown in Figure 1. The mathematics for an I/Q demodulator is as follows:

$$I = F(t) * \cos w_0 t \qquad (1)$$

$$\text{and} \quad Q = -F(t) * \sin w_0 t \qquad (2)$$

* Supported by DOE contract DE-AC05-84ER40150

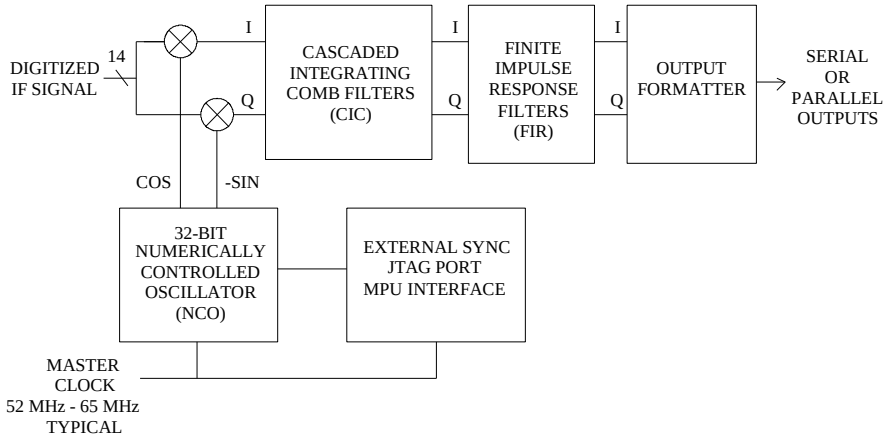

Figure 1. Block diagram of a typical digital down converter.

Letting

$$F(t) = A(t)\cos(w_1 t + j) \qquad (3)$$

where *A* is a function of t with bandwidth that is less than w_0. Substituting equation (3) into equations (1) and (2) and simplifying leads to the following:

$$I = \frac{A(t)}{2}\{\cos[(w_1 - w_0)t + j] + \cos[(w_1 + w_0)t + j]\} \qquad (4)$$

and

$$Q = \frac{A(t)}{2}\{\sin[(w_1 - w_0)t + j] + \sin[(w_1 + w_0)t + j]\} \qquad (5)$$

Applying the appropriate digital low pass filters to eliminate the frequency component that is due to the sum of w_1 and w_0 results in the following:

$$I = \frac{A(t)}{2}\cos[(w_1 - w_0)t + j] \qquad (6)$$

$$\text{and} \quad Q = \frac{A(t)}{2}\sin[(w_1 - w_0)t + j] \qquad (7)$$

Letting $w_1 = w_0$ results in equations (8) and (9) which are the solution for a synchronous I/Q demodulator:

$$I = \frac{A(t)}{2}\cos[j] \qquad (8)$$

$$\text{and} \quad Q = \frac{A(t)}{2}\sin[j] \qquad (9)$$

Further calculating the magnitude of the output, which is the critical parameter for beam position and intensity measurements, leads to the following:

$$Mag^2 = I^2 + Q^2 = \frac{A^2(t)}{4}\{\cos^2[(w_1 - w_0)t + j\ ] + \sin^2[(w_1 + w_0)t + j\ ]\} \quad (10)$$

which can be reduced to:

$$Mag = \frac{A(t)}{2} \quad (11)$$

Thus any small error in frequency only shows up in calculations relating to I and Q where the frequency of I and Q represents the error frequency. An example of this is shown in Figure 2 which is a plot of the I, Q, and magnitude data taken from a proof of principle study for the two tone BPM system described later in this article. In this example the down converter frequency is in error by 55 Hz. In an implemented system this frequency error could be corrected automatically using a software algorithm. Aliasing issues must also be addressed when designing the analog filter, which is applied to the signal just prior to digitization. This anti-alias filter is generally the limiting factor in the bandwidth of *A(t)*. This will ensure that the content from these frequencies does not corrupt the output signal.

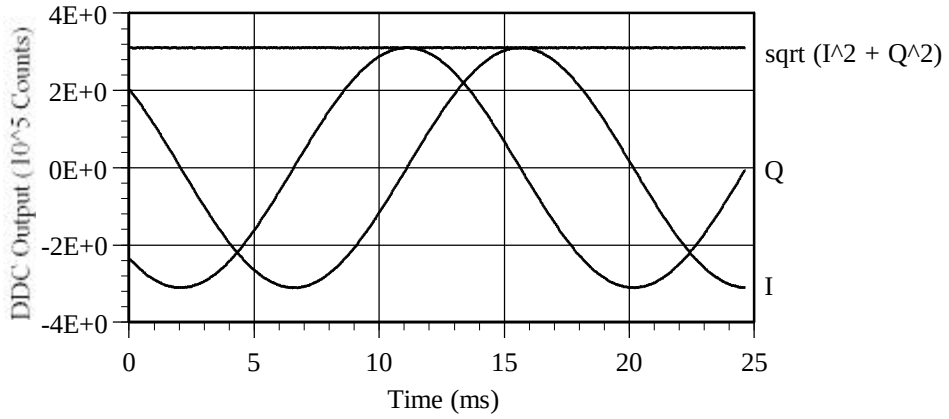

FIGURE 2. Output data from a DDC tuned to 20 MHz with an applied signal with equal harmonic content at 20,000,077 Hz and 11.53 MHz. The raw data are the values for I and Q. The magnitude value was calculated on a point-by-point basis.

In addition to the per-channel costs, some of the practical considerations which must be addressed when choosing a DDC based receiver are the throughput and latency. The throughput or output data rate is a function of the chosen decimation and the input sampling rate. Each device has a required minimum decimation which is determined by the characteristics of the CIC filter. For instance the National Semiconductor CLC5902 allows a minimum decimation of 32 which would give an output data rate of 1.6 MHz for a 52 MHz sample rate. Conversely, the decimation

can be programmed to a value as high as 16,384 which would provide an output sample rate of 3.17 kHz. The minimum latency is a characteristic of the type of FIR filter and its ability to be bypassed. The CLC5902 was implemented with a 21-tap symmetric FIR filter followed by 63-tap symmetric FIR filter, neither of which may be bypassed. This, coupled with the minimum decimation of 32, means that the minimum latency is 53 μs for this device. Similar devices produced by Analog Devices and Intersil have FIR filters which can be configured as asymmetric filters or bypassed completely. Thus the National Semiconductor parts have a latency which must include the FIR filter response time while latency of the Analog Devices and Intersil DDC's can be reduced to that of the CIC filter. Table 1 includes a summary of the characteristics of a DDC devices produced by a number of different manufacturers.

TABLE 1. Characteristics of Digital Down Converters.

Mfg./Part Number	Bits	Sample Rate	Minimum Latency	Output BW	Minimum Decimation	Maximum decimation	Bypass Filters
Intersil IS50214B	14	65 MS/s	60 nS	982 kHz	4	16384	Yes
Nat'l Semi. CLC5902	14	52 MS/s	53 μs	650 kHz	32	16384	No
Analog Dev. AD6620	14	65 MS/s	30 ns	3.6 MHs	2	16384	Yes
Greycode GC4014	14/16	64 MS/s	1.6 μs	886 kHz	32	64000	No
Intersil 50016	16	75 MS/s	1.8 μs	645 kHz	32	131072	No

BEAM POSITION MONITOR EXAMPLE

One of the more common measurement techniques for determining the beam position is to calculate the ratio of the difference and sum of the voltage induced on a pair of diagonal electrodes. One must be able to calibrate the system and expect that the channel-to-channel gain difference will remain constant between calibrations. Switched electrode electronics systems [1] overcome this differential gain problem by using the same RF, IF and baseband electronics for the pair of electrode signals. Other systems have been developed which use a set of matched calibration signals at the beam frequency that are injected into the front end electronics at times when the beam signal is not present. This concept has already been implemented for the BPM system in the Swiss light source [2]. The design proposed below makes use of the frequency selectivity of the DDCs and the ability of DDS devices to generate precise frequency sources which are used as a set of calibration signals that are injected, detected, and processed even when a beam signal is present.

Figure 3 shows a block diagram of the proposed BPM system. The 10 MHz machine master oscillator signal is multiplied to generate a 50 MHz signal that is synchronous with the 1497 MHz beam signal. A DDS device is used to generate a 11.539 MHz signal which is the 128^{th} sub-harmonic of the 1477 MHz local oscillator signal used in by the RF section. The 11.539 MHz signal is also mixed with the 1477 MHz signal in order to generate the 1488.6 MHz and 1465.4 MHz reference

signals. The level of the reference signals is adjusted to a level which is equal to or slightly less than the beam induced signals. These reference signals are then split into four signals and coupled into the RF chain using a directional coupler. The summed 1497 MHz beam signal and the pilot signals are amplified and down converted using the 1477 MHz local oscillator signal. Thus, after low pass filtering, two frequencies are generated by the RF module and transmitted from the radiation area local to the beam line to the service buildings. The beam current signal is at 20 MHz and the reference signal is at 11.539 MHz.

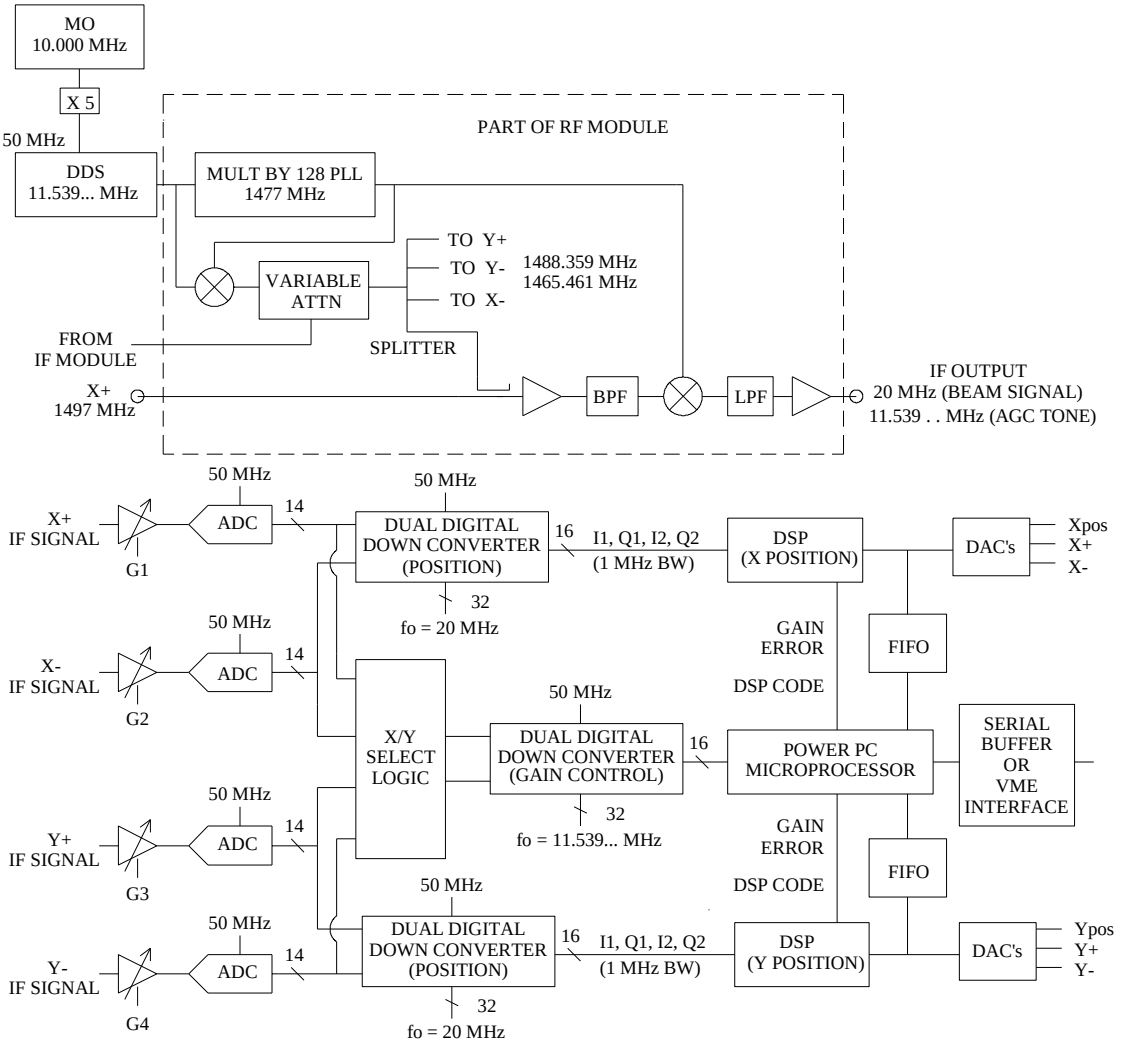

FIGURE 3. Block diagram of a DDC based BPM system with an AGC reference signal.

The IF signals, which are generated in the RF module, are applied to the four inputs of the IF down converter module. These signals are amplified using a variable gain amplifier and digitized using a 12 bit, 50 MS/s analog to digital converter that has an effective bit count of 10 ½ bits. Once the signal is digitized it is sent to two places. First it is routed to a DDC which is set to "synchronously" detect the 20 MHz beam signal. It is simultaneously sent to a DDC which is set to detect the 11.539 MHz reference signal. This reference signal is used to maintain the stability of the gain

difference between the positive and negative signals and to generate a precise gain-error signal. The gain error signal is periodically transmitted to the fast signal processing device, the DSP chip in this example, for use in the position calculation. Because of the flexibility of the on board filtering of the DDC devices as well as the computing power of the DSP devices, the bandwidth and output sampling rates of the system can be varied as required through software changes.

A critical component of the design is the four-way power splitter used in the RF section. It must be stable over the anticipated temperature range. The selection of the reference signal is another consideration. The 8.461 MHz difference in frequency between the reference signal and the beam signal is rather arbitrary. Such a difference allows the low pass filter between the mixer and line driver in the RF module as well as the band pass filter (not shown) between the IF amplifier and the ADC to be rather broad. The tradeoff is that this increases the noise level at the input to the ADC. A reasonable change to the system design would be to modify the 11.539 MHz signal generated by the DDS to 11.593 MHz. This frequency would generate an IF frequency of 13 MHz while providing a reference signal of 11.593 MHz. This would allow one to use a band pass filter with a bandwidth that is an order of magnitude narrower than the original design. Thus the broadband noise would be reduced by a factor of 3.2. Other options that may be considered are using only a single DSP and a PowerPC microprocessor; just a PowerPC microprocessor; or an FPGA for the required processing after the digitization and down conversion.

BEAM LOSS ACCOUNTING EXAMPLE

The beam loss accounting system currently in place at Jefferson Lab consists of five resonant cavity monitors which each generate a 1497 MHz signal proportional to the beam intensity. One of these cavities is located at the exit point of the injector and the remaining cavities are located at the exit points of the machine. These signals are down converted locally to 1 MHz and then connected to a centralized down converter/summer module via coaxial cables. The 1 MHz signals are down converted to a baseband signal using an RMS-to-DC converter. The baseband signals for the machine exit points are summed and subtracted from the signal from the injector. Continuous beam loss greater than 2 μA or a pulsed beam loss greater than 25,000 μsec-μA is sufficient to cause a loss event which interrupts beam delivery. Drifts in the electronics and non linearity associated with the RMS-to-DC converters limit the resolution of the sensitivity of the system. The example presented in this paper is intended to overcome these limitations through the use of a set of stable reference signals and digital down converter technology.

A pair of stable reference signals at frequencies just above and below that of the beam frequency are to be injected into each cavity. Since high amplitude stabilization (one part in 10^4) of the signals is critical to system performance, an absolute power reference must be established. The intention is to use a temperature stabilized multi-stage AGC limiter configuration. The signals will be detected in a manner similar to that used in the BPM example. There is a single ADC for each channel, the output of which is routed to two DDC devices, one of which is set to the 3 MHz “beam”

frequency. The second DDC is switched between 2 MHz and 4 MHz. The beam current will be then calculated as the ratio of the measured beam harmonic divided by the average value of the reference signals. Additionally, the imbalance of the reference signal amplitudes can be used to perform cavity tuning adjustments. The resultant calibrated intensity signal will be routed to a DSP or FPGA-based VME comparator card via a custom interconnection which makes use of the P2 connector. A block diagram of one channel of such a system is shown in Figure 4.

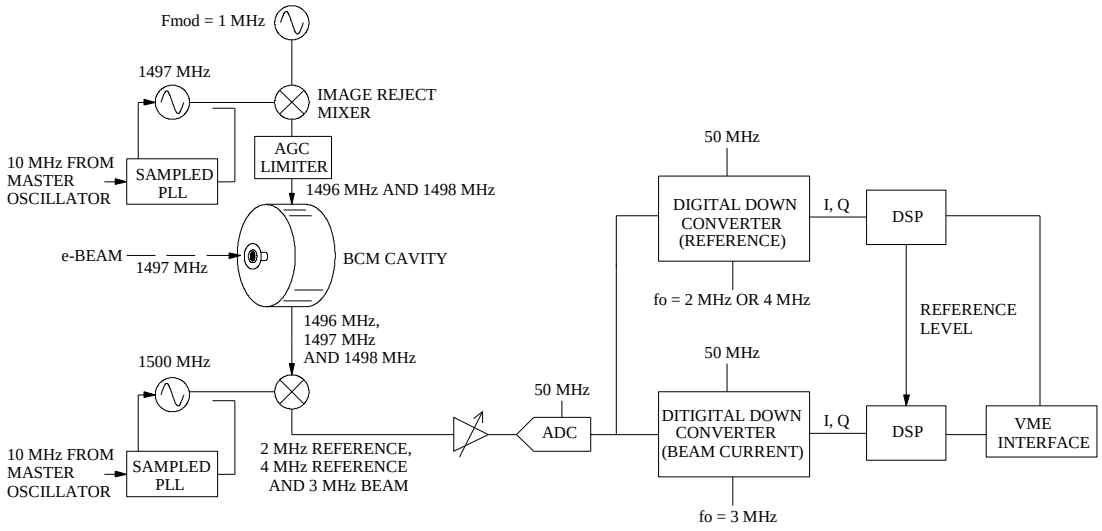

FIGURE 4. Block diagram of one channel of a DDC based beam loss accounting system.

CONCLUSIONS

The basic concepts of a DDC have been presented. Many of the tradeoffs and considerations that must be made when choosing a DDC device were also discussed. Two applications of beam diagnostics systems that make use of DDC technology were described. The beam loss accounting system is currently being refined for development. Preliminary studies for these two systems indicate that the DDC technology is a valuable, versatile, and easy to implement technology. The combination of good linearity and low noise floor expected for systems built with this technology rivals that of any of the available analog technologies.

REFERENCES

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