1.0 Wireless, Hand-Held Data Acquisition System for Imaging Detector

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Project Status

In the preceding two quarters the project has progressed much as expected, with effort distributed between acquiring test and evaluation modules, assessing several of those modules and refining the dataflow conceptual design in response to findings for their analog, interface and RF capabilities. We have identified and acquired modular electronics for the analog front end, acquired and tested demonstration/evaluation circuitry for the RF and processor sections and have acquired evaluation components for the battery/power supply section but have not yet proceeded with power supply tests. A safety review of the battery hazards and controls was completed on 4-14-2014.

There were several candidate approaches to consider initially for the dataflow, each depending to some extent on the matching of and achievable throughput from the A/D through to the wireless communication system. Lack of sufficient technical support from the RF modue manufacturers for high data rate operation was the disappointing limiting factor in choosing an RF module. We have now settled on a dataflow concept: A low power, 4-channel, 12-bit synchronously sampled A/D followed by FPGA-based triggering and integration, transmitting selected integrated event data via 802.11-based wireless at an 8 Mbit/s rate. Two RF modules are available that support that approach without upfront NRE costs. This would support a theoretical maximum detector event rate of ~80 kHz.

The digital electronics platform requires an FPGA approach to manage the four simultaneous sampled data streams and provide the integrated data stream to the wireless module. As the estimates of gate usage are developed further a target FPGA device can identified with lower power consumption than the development platform.

Project Plan

We expect to continue with the development of firmware for testing the analog front end and coupling that to the RF section. With selection of the FPGA/processor for demonstration we expect to proceed with configuration and testing of the power supply and battery subsystem. Test software will be developed to validate the throughput of the RF link. A simple user interface for the host computer will be developed to provide a test platform for command uplink and data downlink.

We currently appear to be on schedule for a demonstration of system components by the end of the project period. The following table compares milestones with current status and expectations for completion.

Original project milestones and status/expectations to date:

Month 1-4	Technology Review (DAQ, RF, PWR)	Complete
Month 4	Preliminary Technology Selection	Complete
Month 6	Acquisition of Candidate Subsystems	Complete
Month 10	Initial Data Acquisition System Tests	In Progress, Expected 7/2014
Month 12	Data Stream Test of RF Subsystem	In Progress, Expected 8/2014
Month 12	Bench top Demonstrations	On Schedule for 9/2014

Budget

Funds from the first period of performance have been allocated reasonably close to the original plan but are currently undershooting initial estimates. The availability from the manufacturers of a number of ready-made and moderately flexible evaluation PCB assemblies has resulted in some cost savings realized by avoiding the cost of custom PCB fabrication to perform the initial evaluation of candidate components. We were fortunate to find manufacturer-supplied boards that were suitable for testing. In particular, the A/D converter is available with supporting circuitry and a compatible connector that allows testing with one of the digital subsystem candidates with no additional wiring at all. Testing with the lower power digital subsystem will require fabrication of a simple interface.

The testing strategy may require fabrication of additional custom PCBs as we get closer to integrating subsystems, but overall, much of the FY14 funds allocated to Consultants and Subcontractors (PCB fabrication contracts) could be reallocated.

Software and firmware development will become a larger part of the effort in the remaining months of the period of performance. We would allocate some of the funding from the FY14 consultants and subcontracts category to the labor category to support the additional assistance of Wenze Xi and/or Hai Dong in the firmware development for FPGA.

We have requested and expect to have a student from the Science Undergraduate Laboratory Intern program for this coming summer assigned to the project. The project is reasonably well-suited to provide an engaging and challenging multi-disciplinary experience for a student, and the intern's time is without cost to the program. With an intern, the PI is expected spend additional supervisory time on the project. Those additional hours will also be reallocated from the Consultants and Subcontracts category.

Publications

none

Workshops/Conferences

none