# Hall B RICH Cooling System Tests

**Date: October 14, 2019**
**Time: 9:00AM – 10:00AM**

*Attendees: Aaron Brown, Peter Bonneau, Pablo Campero, Brian Eng, Tyler Lemon, Vincenzo Lucherini, Marco Mirazita, Sandro Tomassini*

1. Overview of compressors' status and timeline
    - 1.1. Compressor naming convention:
        - 1.1.1. Compressor 1 – compressor used in previous experimental run who recently underwent routine maintenance.
        - 1.1.2. Compressor 2 – compressor previously used in EEL during RICH assembly and was left unpowered in Hall B.
    - 1.2. October 7, 2019
        - 1.2.1. Compressor 1 powered to allow RICH electronics to be powered.
        - 1.2.2. Noted that buffer tank pressure was lower than normal and not showing saw-tooth pattern of compressor's on-off cycle.
    - 1.3. October 9, 2019
        - 1.3.1. Power transferred to Compressor 2.
        - 1.3.2. Leak found and repaired on buffer tank supply hose.
        - 1.3.3. Compressor 2 behaved as expected, showing saw-tooth pattern of compressor's on-off cycle when left running for ~24 hours.
    - 1.4. October 10, 2019
        - 1.4.1. Power transferred back to Compressor 1.
        - 1.4.2. After a few hours, noted that pressure in buffer tank was steadily decreasing and holding constant at ~80 psi.
        - 1.4.3. During further investigation, heard squealing sound coming from compressor; hit emergency stop button to shut down compressor.
        - 1.4.4. Cooling system left in off and depressurized state.

2. Sandro Tomassini and Dario Orecchini will be at JLab from October 22 to October 31, 2019 for cooling tests.

3. Plan for cooling test
    - 3.1. Goal of tests is to keep RICH FPGA temperatures under ~75 °C.
    - 3.2. Ideal total airflow would be < 600 slm.
        - 3.2.1. In theory, 600 slm for one RICH sector would allow two RICH sectors to be cooled by one compressor, with second acting as backup.
    - 3.3. Compressor settings will also be optimized to limit time compressor is running while still providing enough flow to RICH.

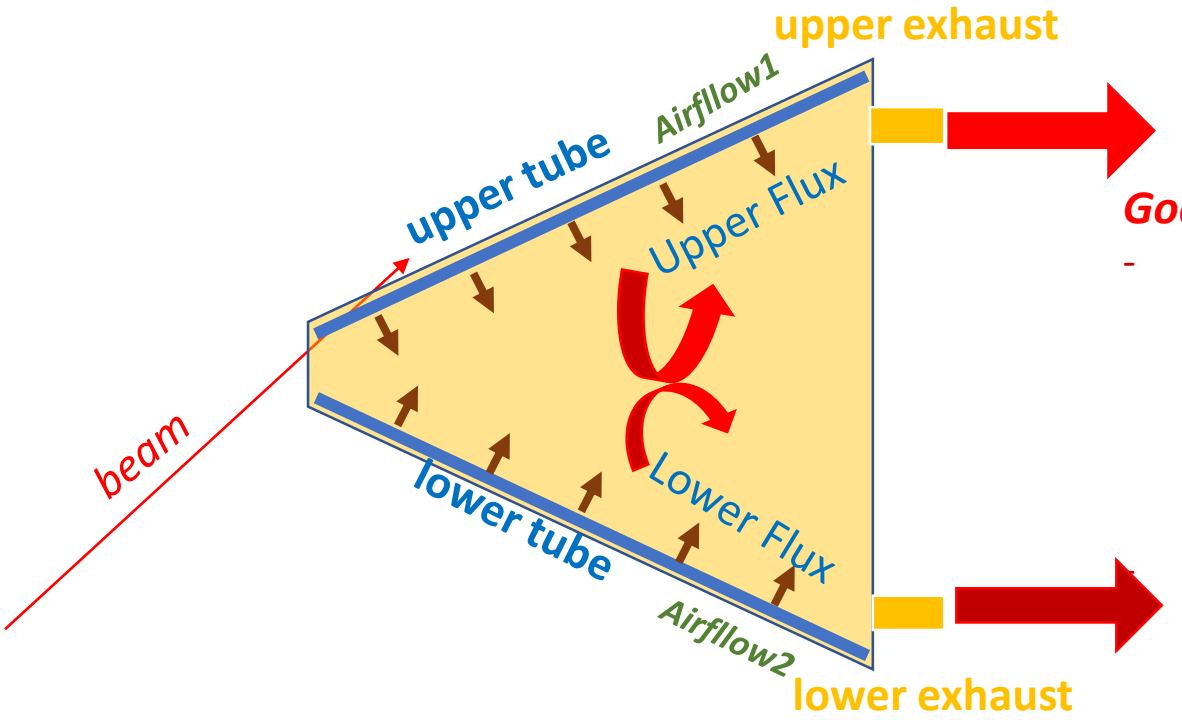
4. Test procedure
    - 4.1. Turn RICH on with 900 slm total airflow (Airflow 1 (AF1) at 500 slm and Airflow 2 (AF2) at 400 slm).
        - 4.1.1. Settings previously used in experimental run to run RICH.
    - 4.2. Change AF1 to 400 slm and AF2 to 500 slm (900 slm total).
        - 4.2.1. If interlock trips, stop tests. 900 slm (AF1 = 500 slm, AF2 = 400 slm) must be used for RICH operations.
    - 4.3. Adjust AF1 to 400 slm and AF2 to 400 slm; wait for steady state or interlock.
    - 4.4. If no interlock, decrease total airflow in 100 slm steps, waiting for steady state or interlock between changes.
    - 4.5. Settings before test with flowrates where interlocks tripped will be used during RICH operations.
        - 4.5.1. Example: if interlock trips with AF1 = 300 slm and AF2 = 300 slm, settings used for RICH operation will be AF1 = 350 slm and AF2 = 350 slm.

# *Optimizing & Minimizing the air flux to cool the RICH's E.P.*

**- Being a test, it is correct to over-stress the set-up above the usual limits selected for the normal working conditions in the operative mode.**
**That means that the safety temperature upper bound, during the tests, should be the highest allowed not to permanentely damage any hardware.**

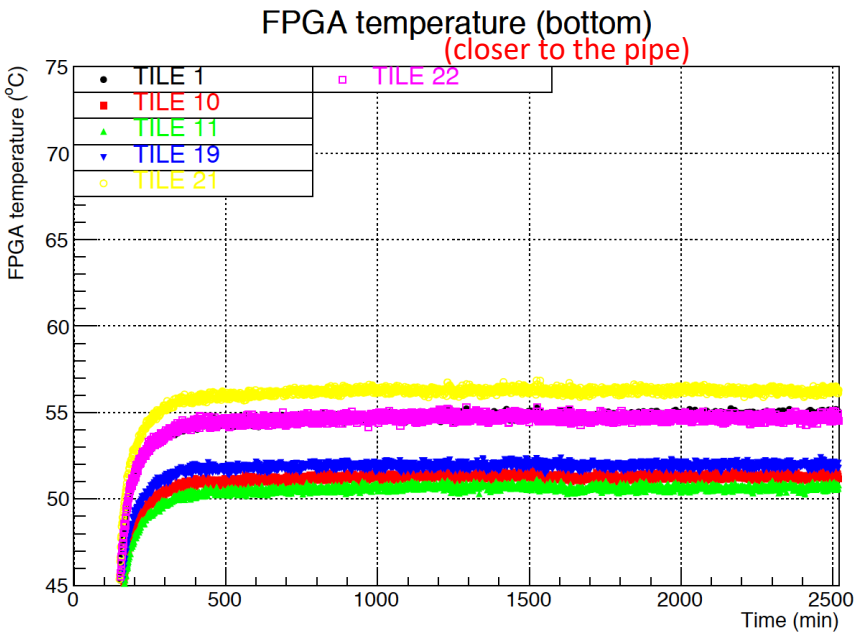
*The 75 $^{0}$C actually used is OK*

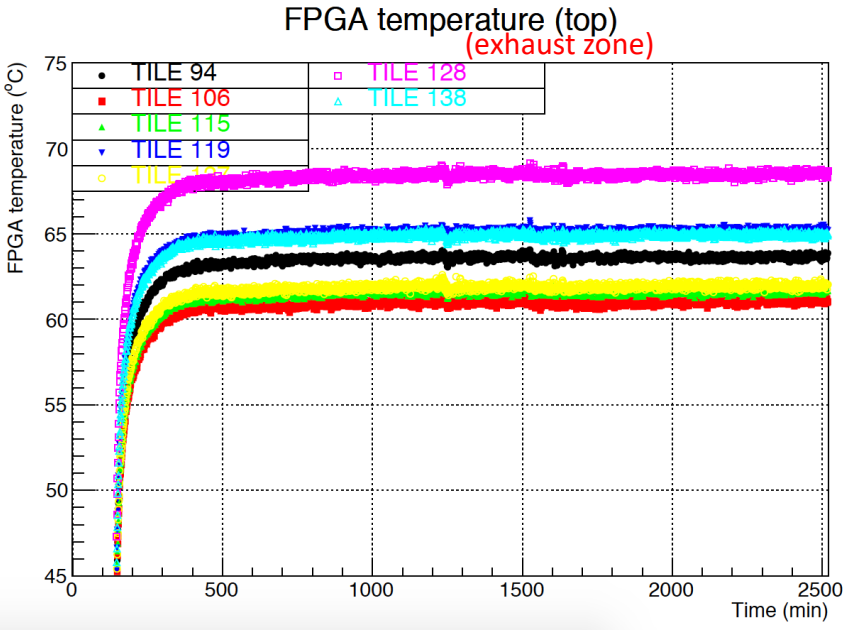
**- Undestand the geometry-topology!!!**

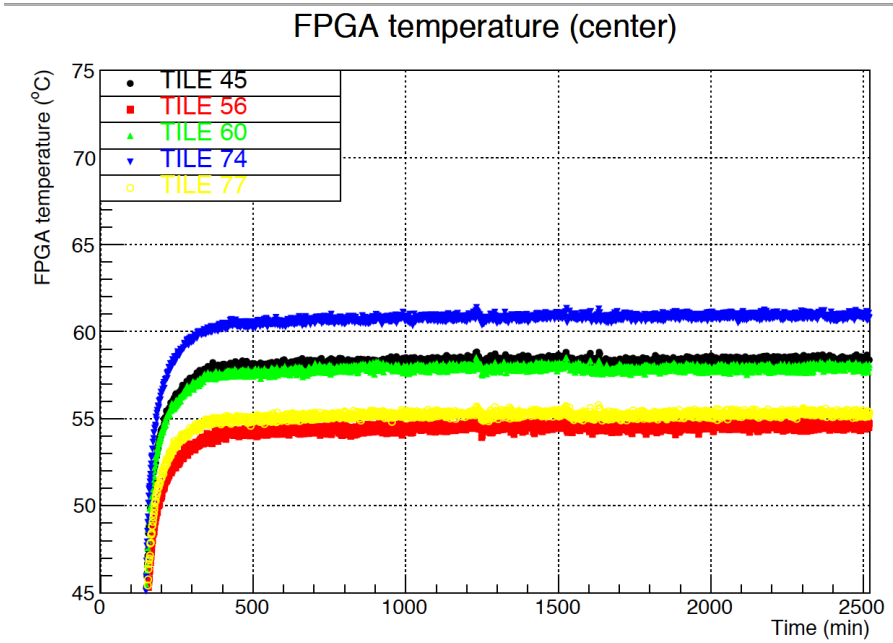


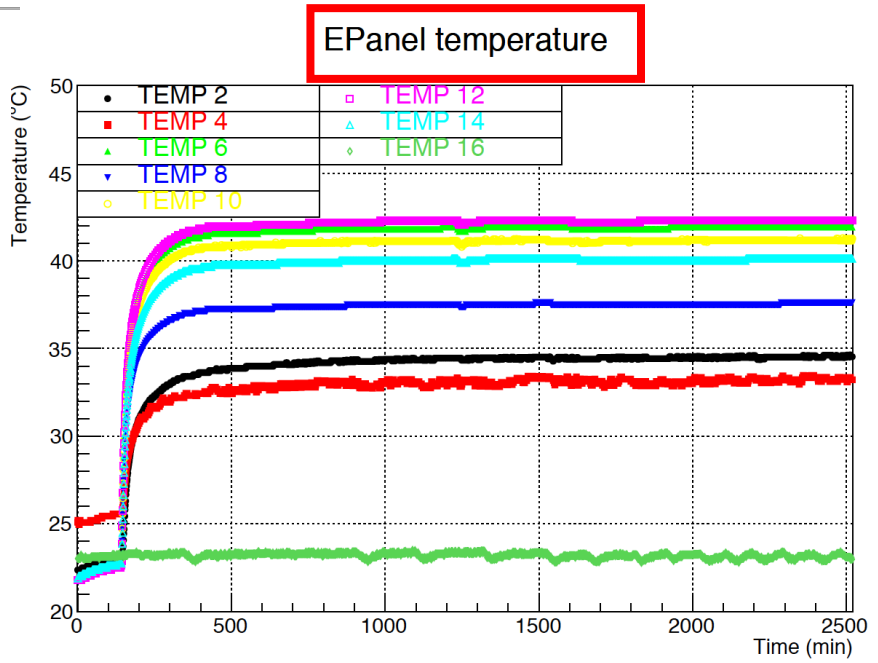

***Goal***

- ***Operate the compressors to deliver the minumm air flux compatible with a prolonged operations in a safety temperature region. Possibly use 1 compressor for 2 RICH, the other spare.***
- ***Undestand the 'hottest' probe.***

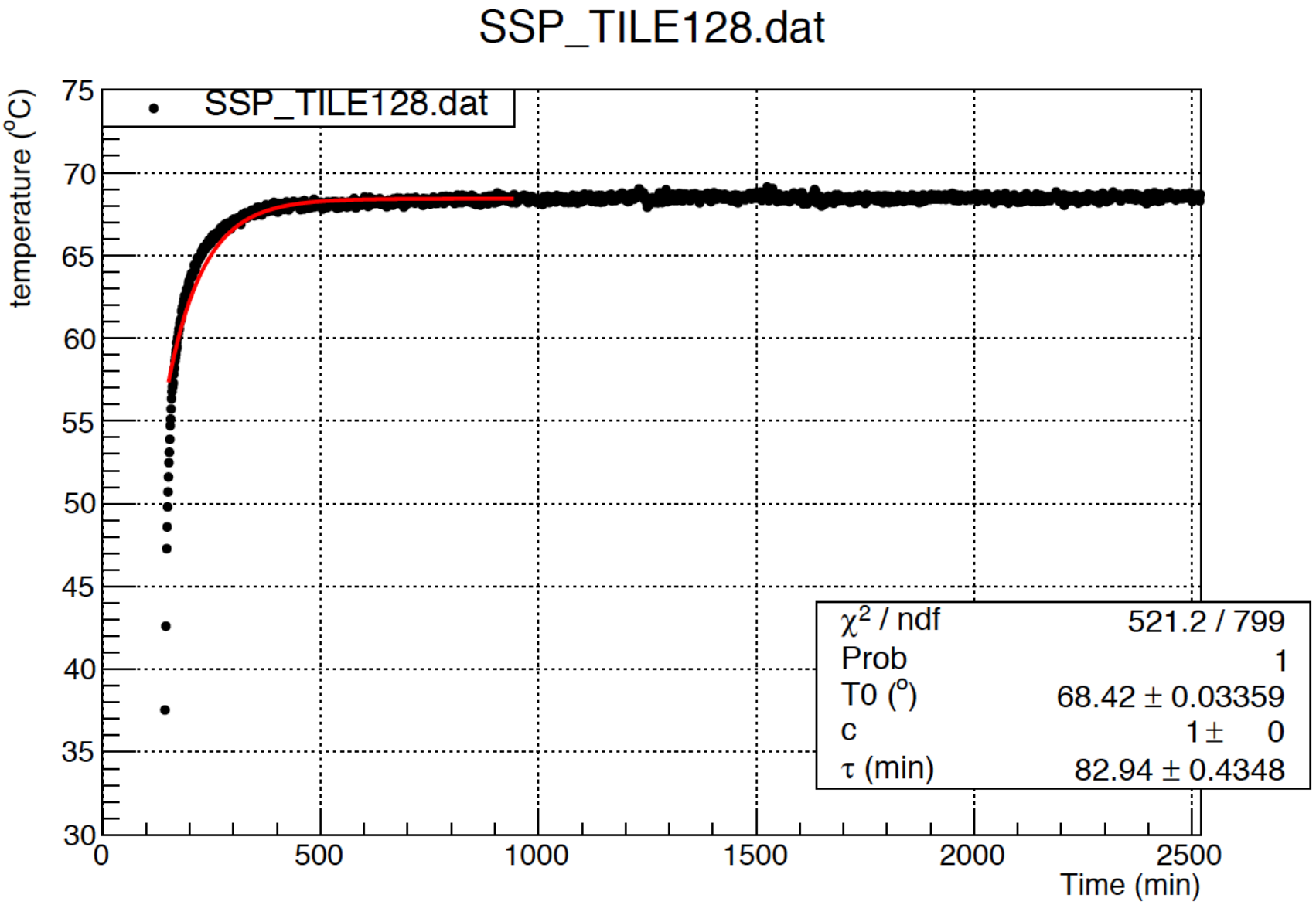

FPGA temperature (bottom)
(closer to the pipe)
TILE 1
TILE 10
TILE 11
TILE 19
TILE 21
TILE 22
FPGA temperature (°C)
Time (min)


FPGA temperature (top)
(exhaust zone)
TILE 94
TILE 106
TILE 115
TILE 119
TILE 128
TILE 138
FPGA temperature (°C)
Time (min)


FPGA temperature (center)
TILE 45
TILE 56
TILE 60
TILE 74
TILE 77
FPGA temperature (°C)
Time (min)


EPanel temperature
TEMP 2
TEMP 4
TEMP 6
TEMP 8
TEMP 10
TEMP 12
TEMP 14
TEMP 16
Temperature (°C)
Time (min)

# The hottest


SSP_TILE128.dat
SSP_TILE128.dat
temperature (°C)
Time (min)
75
70
65
60
55
50
45
40
35
30
0
500
1000
1500
2000
2500
χ² / ndf 521.2 / 799
Prob 1
T0 (°) 68.42 ± 0.03359
c 1 ± 0
τ (min) 82.94 ± 0.4348

# A possible strategy

*Steps of 100slm each?*

Switch ON Compressor(s),
Put: AF1 (500slm) & AF2(400slm) wait stable fluxes
Then switch on EP electronics (LV & HV)
Start measurement
Wait equilibrium (it means 6-7 hours from past experience)

↓

Switch OFF EP electronics
Wait room thermalization
with previous air fluxes on

↓

Put: AF1=400slm; AF2=500slm; stable fluxing.
switch on EP electronics (LV & HV)
Wait equilibrium (the time can depend from the airflow) or Interlock

↓

**Interlock?** —**Yes**→ Sorry, apparently nothing can be changed from the previous working conditions.

↓ **NO**

(1) Switch OFF EP electronics Wait room thermalization
with previous air fluxes on

↓

(2) Put: AF1=400; AF2=400; stable fluxing.
switch on EP electronics (LV & HV)
Wait equilibrium or Interlock

↓

Interlock? —**Yes**→ this cannot be the working condition: the OK was the one with the previous Air fluxes

↓ NO

Repeat the previous two steps (1)&(2) reducing fluxes of -100slm steps (both separately and at the same time) till interlock happens. indicating the new working conditions as the next previous one, with no interlock.

*If we could reach total 600slm, we could use only one compressor for 2 RICHs, in case one compressor fault.*