FPGA Command Engine Development for the RICH Hardware Interlock System

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A data acquisition (DAQ) system for the Sensirion SHT85 sensors [1] using the sbRIO-9627 CompactRIO Single-Board Controller [2] is being developed for the RICH detector. This DAQ system will be integrated into the Hardware Interlock System for the next RICH sector.

The DAQ code is divided into two sections: FPGA Command Engine (FCE) and System Scan Engine (SSE). FCE generates all command functions and signal timings needed to read and program 48 SHT85 sensors; SSE determines which command function is used and determines on which individual sensor the command is executed. Additionally, SSE performs all interlock functions of the Hardware Interlock System.

FCE communicates with the SHT85 sensors using the 2-wire I²C serial bus. To generate the required clock and signal timing specific to the SHT85 sensors, a LabVIEW library [3] of I²C sub-VI functions is used as the basis of each of the SHT85 FPGA command programs.

The commands initialize, set up operating parameters, execute the main function, check the validity of the read data, and return the data and command status to the SSE.

Fig. 1 shows the flowchart for the single shot DAq mode (SSDM) [4] command. Table I summarizes the commands developed for the FCE.

The commands are shown in the top level of the LabVIEW FPGA command engine block diagram in Fig. 2. In addition to the data and status returned to the SSE by each command, the FPGA command engine transmits its overall operational status back to SSE.

In conclusion, the FPGA command engine code was developed, tested, and debugged to support all command functions needed to read and program 48 SHT85 sensors. This code will be integrated into the Hardware Interlock System for the next RICH sector.

- [1] P. Bonneau, et al. *Proposed Integrated Temperature and Humidity Digital Sensor for the RICH Detector*, DSG Note 2019-12, 2019.
- [2] P. Bonneau, et al. Proposed Controller for the Readout of the Temperature and Humidity Digital Sensors Sensi¬rion <u>SHT85 Envisioned for the RICH Detector</u>, DSG Note 2019-27, 2019.
- [3] P. Bonneau, et al. *Developing a Readout System for the* Sensirion SHT85 Sensors, DSG Note 2019-28, 2019.
- [4] P. Bonneau, et al. Development of Data Acquisition to <u>Read out Sensirion SHT85 Temperature and Humidity</u> <u>Sensors for the RICH Detector</u>, DSG Note 2019-31, 2019.



FIG. 1. Flowchart of Sensirion SHT85 single shot DAq mode.



FIG. 2. Top level of LabVIEW FPGA command engine block diagram.

Command name	Function	Comments
FPGA read sensor serial #	returns sensor unique serial #	serial # assigned by manufacturer
FPGA read sensor status	returns sensor's internal status register	includes heater and checksum status
FPGA enable/disable sensor heater	sensor internal heater control	heater increases sensor temp by a few $^\circ \mathrm{C}$
FPGA general call reset	resets all devices on an I ² C bus	Uses general call mode as defined by I ² C spec
FPGA clear status registers	sets all status flags to zero	clears checksum and command errors
FPGA sensor soft reset	resets specifically addressed SHT85 sensor	initializes sensor and loads calibration constants
Single shot DAq mode	instructs sensor to return single measurement	every measurement is verified by cyclic redundancy check
Periodic DAq mode	after initialization, sensor transmits stream of measurements on preset interval	.5, 1, 2, 4, 10 measurements/second in- tervals
Periodic start/stop	initializes and starts or stops periodic mea- surement stream	sensor will respond with not acknowl- edge if no data is available for readout

TABLE I. Sensirion SHT85 commands developed for the FPGA command engine.