# Upgrade of the Hardware Interlock System for the Hall B Silicon Vertex Tracker

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May 4, 2020

This note reports on the current hardware configuration, operational history, and the planned upgrade to the hardware interlock system of the Silicon Vertex Tracker (SVT) [1].

EPICS is the primary means of continuous real time monitoring, controlling, and interlocking of all important parameters of the SVT, a part of Hall B's Central Detector.

The hardware interlock system [1][2] is a separate, standalone system that protects the SVT by monitoring key detector parameters and taking corrective action if a monitored signal is outside pre-programmed limits. It was developed and integrated into the controls and monitoring system to protect the SVT from damage if EPICS were to fail or network communication was to be lost.

The hardware configuration is based on National Instruments' model 9035 compact reconfigurable input output (cRIO) controller—a modular, embedded controller designed for industrial control and monitoring applications. The cRIO-9035 features a dual-core CPU running at 1.33 GHz, a Xilinx FPGA, and an 8-slot chassis.

The components for the hardware interlock system are housed in a 5U (8.75") rack-mounted chassis. Figure 1 shows the block diagram of the chassis components, signal lines from the SVT, power lines to enable the low voltage/high voltage crates, and the power line to the humidity sensors.

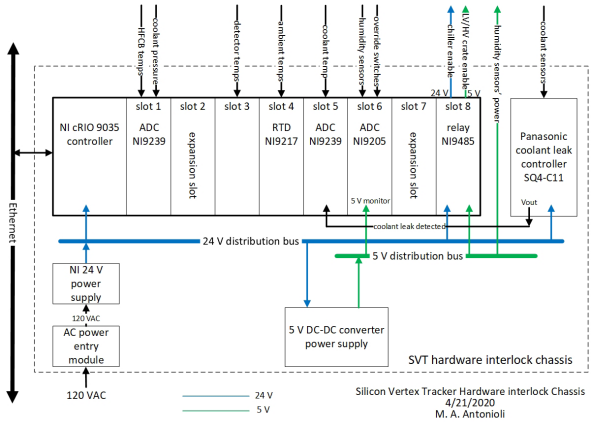


FIG. 1. Block diagram of SVT Hardware Interlock chassis.

The cRIO controller, Panasonic liquid leak sensor controller, and the 5 V DC to DC converter are powered by a 24 VDC distribution bus sourced by a National Instruments industrial power supply, Fig. 1.

The 5 VDC distribution bus connects to the output relay module and powers the humidity sensors. To monitor the hardware interlock system itself, the 5 VDC distribution bus is connected to an ADC input, which enables monitoring of the 24 VDC source, thereby the state of the system.

ADCs in the system measure voltage signals from coolant and module temperature sensors, humidity sensors, and the coolant leak detector. Additionally, the ADCs monitor the positions of the two front panel interlock override keys, which allow system experts to update the cRIO software while the SVT is powered. The RTD input modules measure the internal temperatures of the SVT and the local ambient temperatures around the detector.

During operations, the output relays are energized on normally open contacts. The 5 VDC relay output enables the low voltage/high voltage power supply crates. The 24 VDC relay output enables the chiller, Fig. 1.

The signals monitored by the hardware interlock system to detect fault conditions are summarized in Table I.

Under fault conditions, the cRIO uses a relay output module to disable the SVT chiller and/or the low voltage and high voltage crates powering the detector. This disabling action overrides EPICS controls of the chiller, low voltage, and high voltage.

The hardware interlock system was designed, fabricated, and installed in June, 2015. Since its commissioning, it has been operating continuously, dependably, and reliably. Typically, the continuous running period—between annual system software updates of LabVIEW—is about 8000+ hours. The SVT hardware interlock system is the longest operating NI cRIO-based system in Jefferson Lab's Physics Division.

To date, the basic system design has been duplicated for the calorimeter, the time of flight detectors in the Forward Tagger [3][4], and the nitrogen volume and the electronics panel of the RICH detector [5][6].

An upgrade of all hardware interlock systems is planned first for future sectors of the RICH detector [7,8,9,10,11]. The new hardware interlock system design features Sensirion temperature and humidity sensors, which are integrated into a single package, thereby reducing the size of the board and the number of cables required for the readout sensors. The Sensirion temperature and humidity sensors have an accuracy of +/-0.1° C and +/-1.5% RH, respectively. The sensors have a digital communication interface and are individually calibrated and programmed at the factory with linearization and temperature compensation calibration data specific to the sensor. The FPGA-based readout system by National Instruments features a high density digital interface supporting 48 sensors on a single board.

An upgrade to the SVT system that is to be implemented in 2020 is the installation of cable disconnects for the hardware

| Signal name | NI I/O module | Type | # of signals | Description |
|---|---|---|---|---|
| HFCB temp. | NI9239 | ADC | 3 | monitors top side modules in regions 1, 2, 3 |
| Detector internal temp. | NI9217 | RTD | 3 | mounted in module support rings |
| Internal humidity | NI9205 | ADC | 3 | mounted in module support rings |
| Internal dew point | calculated | | 3 | calculated from sensors in module support rings |
| Ambient temp. | NI9217 | RTD | 2 | sensors externally mounted onto detector |
| Ambient humidity | NI9205 | ADC | 2 | sensors externally mounted onto detector |
| Ambient dew point | calculated | | 2 | calculated from external sensors on detector |
| Coolant pressure | NI9239 | ADC | 1 | measures coolant pressure (external from chiller) |
| Coolant temp. | NI9239 | ADC | 1 | measures coolant temp. (external from chiller) |
| Coolant leak detection | NI9239 | ADC | 1 | checked by sensor mounted in detector drip pan |

TABLE I. Signals monitored by the hardware interlock system.

interlock system's chassis. The original cable connection design was based on the assumption that once the SVT was installed and commissioned, it would rarely be uninstalled during its operational lifetime. Therefore, all the cables from the SVT and associated instrumentation were hard-wired to the hardware interlock system. Unfortunately, over the years the detector has had to be uninstalled several times. Hence, the new cable disconnects should in principle reduce the time and effort required for the installation or removal tasks associated with the SVT and the hardware interlock system. The location of the cable disconnect system is shown in Fig. 2.

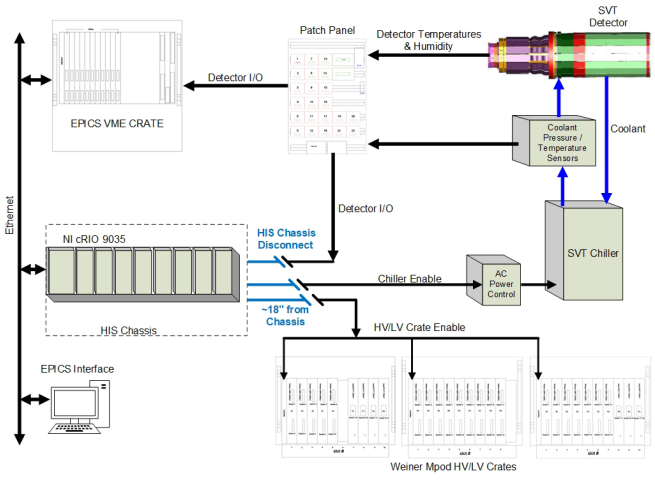


FIG. 2. SVT hardware interlock system block diagram.

Located approximately 18 inches from the hardware interlock system chassis, the disconnect system uses cables assembled with circular plastic connectors (CPC), which are keyed to prevent incorrect mating and lock to avoid inadvertent cable disconnects.

In conclusion, the hardware interlock system protects the SVT detector from damage in the event the primary EPICS controls and monitoring system fails, or in the event the network communication is lost. Since it's commissioning in February, 2015, the hardware interlock system has been protecting the SVT, operating continuously, reliably and dependably. The addition of the cable disconnects will reduce the time and effort required for installation or uninstallation of the system.


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