

The EPICS User Interface for Hardware Interlock Systems

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In the program for the hardware interlock systems [1], the EPICS user interface subroutine handles the communication and control between the interlock system and external EPICS client applications. This note summarizes the communication and control signals translated by the subroutine, and the EPICS input/output (I/O) configuration and functionality. For the Hall C Neutral Particle Spectrometer (NPS) [2], a new configuration is being developed.

Hardware interlock systems for the SVT, Forward Tagger, and RICH I [3, 4, 5, 6, 7, and 8] are standalone systems that monitor key detector parameters and interlock the system when a monitored signal is outside pre-programmed limits.

The EPICS user interface subroutine translates the hardware interlock system signals to EPICS process variables (PVs) through an EPICS server. These PVs communicate with an EPICS client user interface program installed and running on computers on the same subnet.

Figure 1 shows a diagram of an EPICS user interface subroutine. Due to differences in the detector systems, each EPICS user interface subroutine is written specifically for that detector system. The signal categories shown in Fig. 1 and detailed in Table I are common to all hardware interlock systems.

Other subroutines within the hardware interlock program communicate with the EPICS user interface via the inter-process communication bus.

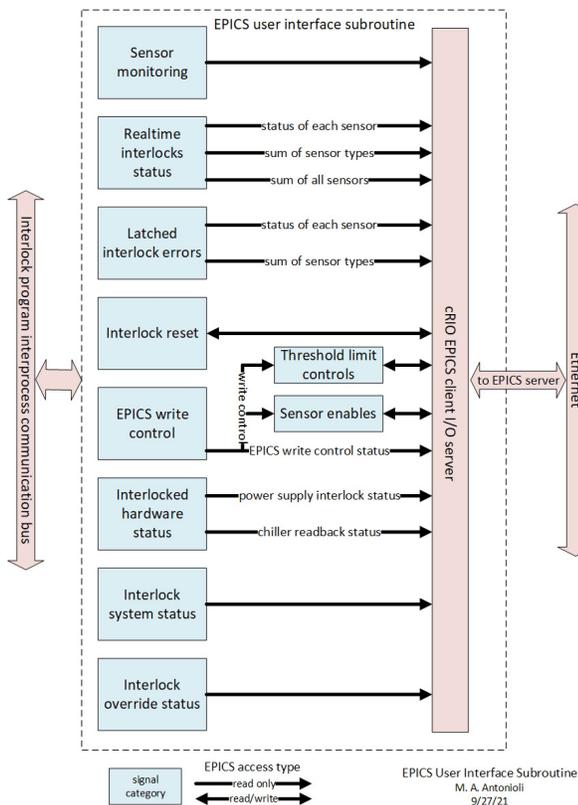


FIG. 1. Diagram of the EPICS user interface subroutine.

Each signal listed in Table I has a corresponding variable (data storage location) within the EPICS user interface, with an EPICS access type parameter assigned to it by the EPICS user interface subroutine, so that an external EPICS client program can either read it, write to it, or both read and write, depending on the access type. The EPICS write privilege must be enabled for EPICS client programs to write the interlock threshold limits and sensor enables to the system. The EPICS write privilege is enabled by default at system startup.

The conversion from the interlock system's internal signal variables to EPICS PVs is accomplished in part by the cRIO EPICS client I/O server. To function, this server must be supported by a separate EPICS server on the same network subnet that serves the PV names of the hardware interlock system client.

As shown in Fig. 2, upper section, an EPICS client cannot directly write a PV to the network. It must be requested through the specific network EPICS server for that particular PV. In EPICS systems, identical process variable names on multiple servers are not allowed on the same subnet. When the cRIO controller is configured as an EPICS client, the hardware interlock system depends on the external EPICS server computer, EPICS server program, and the interconnecting Ethernet network to be properly operating for the EPICS user

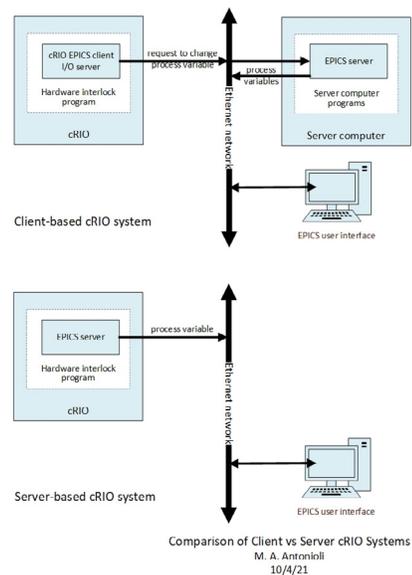


FIG. 2. Comparison of PV write in client vs. server cRIO systems.

interface to function. All the hardware interlock systems in operation are EPICS client-based cRIO systems due to standardization in the experimental hall where they are used.

For the NPS hardware interlock system, a new EPICS I/O configuration is being developed. When the cRIO controller is configured as an EPICS server, bottom portion of Fig. 2, the EPICS communication directly reads and writes PVs to the network. This circumvents possible points of failure present in the current EPICS client-based configuration.

In conclusion, the EPICS user interface subroutine handles the communication and control between the interlock system and external EPICS client applications. For the Hall C Neutral Particle Spectrometer, a new EPICS I/O configuration is being investigated.

- [1] [P. Bonneau, et al., *Program for the Hardware Interlock System of the Hall C Neutral Particle Spectrometer*, DSG Note 2021-21, 2021.](#)
- [2] [P. Bonneau, et al., *Hardware Interlock System for the Hall C Neutral Particle Spectrometer* DSG Note 2021-15, 2021.](#)
- [3] [M.A. Antonioli, et al., *The CLAS12 Silicon Vertex Tracker*, Nucl. Instrum. Methods Phys. Res. A 962 \(2020\).](#)
- [4] [P. Bonneau, et al., *Hardware Interlock System of the Hall B Silicon Vertex Tracker*, DSG Note 2016-04, 2016.](#)
- [5] [A. Acker et al., *The CLAS12 Forward Tagger*, Nucl. Instrum. Methods Phys. Res. A 959 \(2020\).](#)
- [6] [P. Bonneau, et al., *Interlock System for the Hall B Forward Tagger*, DSG Note 2017-07, 2017.](#)
- [7] [M. Contalbrigo, et al., *The CLAS12 Ring Imaging Cherenkov Detector*, Nucl. Instrum. Methods Phys. Res. A 964 \(2020\).](#)
- [8] [M.A. Antonioli, et al., *Proposal for RICH Hardware Interlock System*, DSG Note 2017-01, 2017.](#)

Signal category	Description	EPICS access type	Data type
Sensor monitoring	real-time measurement values of sensors: temperature, humidity, flow, pressure	read only	numeric
Real-time interlocks status	real-time interlock status of each sensor. Indicates if sensor is presently outside of high or low limits	read only	Boolean
Real-time interlocks status	real-time sum of interlock status for a sensor type: temperature, humidity, flow, pressure (includes high and low limits)	read only	Boolean
Real-time interlocks status	real-time interlock status of all sensors (i.e. is any sensor presently outside of limits)	read only	Boolean
Latched interlock errors	latched interlock error status of each sensor; indicates if sensor has been outside of high or low limits since last reset	read only	Boolean
Latched interlock errors	latched sum of interlock error status of a sensor type: temperature, humidity, flow, pressure (includes high and low limits)	read only	Boolean
Interlock reset	clears all latched interlock errors	read/write	Boolean
Sensor interlock enable	enables interlock for each individual sensor	read/write*	Boolean
Threshold limit controls	high and low interlock threshold limit controls for each sensor	read/write*	numeric
EPICS write control status	write enable status for EPICS interface; must be enabled to write sensor enables and threshold limits from EPICS client user interface to interlock system	read only	Boolean
Interlocked hardware status	status of hardware interlocked by system (i.e. if detector power supplies and chiller are enabled by system)	read only	Boolean
Interlock override status	status of hardware interlock system maintenance override keys (i.e. if power supplies and chiller are enabled by keyed switches on front panel of hardware interlock system)	read only	Boolean
Interlock system status	hardware interlock system heartbeat; indicates that cRIO controller and interlock program is active	read only	Boolean
Interlock system status	indicates percentage of cRIO controller CPU usage and hours of system uptime since last boot of controller	read only	numeric

TABLE I. EPICS user interface signals. *For EPICS clients to write to these variables, the interlock system write control must be enabled.