Development of the CS-Studio Phoebus Alarm System for the EIC-DIRC Laser Interlock

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October 4, 2023

This note presents the development of the setup to test the Phoebus alarm system using the EIC-DIRC laser interlock printed circuit board (PCB) as a real-time data signal source.

For the development of the Phoebus alarm system [1], a test system has been designed, developed, and implemented. The alarm system has been tested with a host-based EPICS softIOC—generates simulated signals—and a Phoebus software package [2, 3, 4].

The next test is planned to be done with a real-time data signal source—EIC-DIRC laser interlock PCB [5]. In this test, the interlock signals *immediate status* and *latched status* sourced by the laser interlock circuit, Fig. 1, will be monitored. *Immediate status* signal is the instantaneous laser interlock status value that is latched and becomes the *latched status* signal.

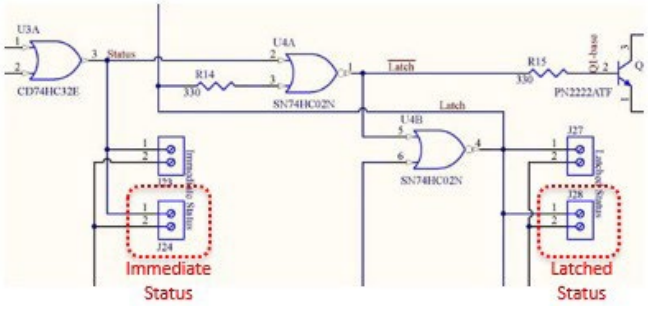

FIG. 1. EIC-DIRC laser interlock PCB signals.

The test setup, Fig. 2, consists of a National Instruments cRIO that monitors the laser interlock status signals, an EPICS softIOC that generates the alarms, and the alarm system software packages that look for alarm conditions.

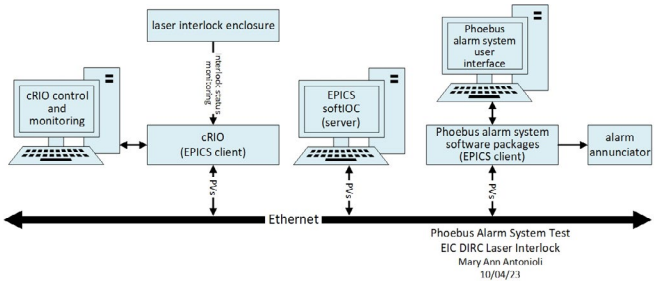

FIG. 2. Phoebus alarm system test with EIC-DIRC laser interlock.

An ADC module within the cRIO chassis, which has controller model #9045, will digitize the status signals. A program developed in LabVIEW and running on the cRIO's Linux real-time operating system reads the digitized laser interlock status data from the ADC. Acting as an EPICS client, the cRIO converts the status data into EPICS process variables (PVs) and writes to the network using EPICS channel access.

An EPICS softIOC application developed for the alarm system test functions as the EPICS server for the system. The softIOC compares the laser interlock status PV values with the pre-programed alarm limits stored within the softIOC. If the PV value equals or exceeds the alarm limits, the softIOC generates an alarm via PV alarm status (HIHI, HIGH, LOW, LOLO) and severity (major, minor).

Code developed for the alarm system software packages specifically for this test with the EIC-DIRC laser interlock will monitor the interlock status PVs for alarm conditions. If the alarm system detects a PV in an alarm state, it latches the PV value at the time of the alarm with a timestamp. The alarm system alerts users via the user interface and the annunciator. The acknowledgement of alarms and the configuration of the alarm settings is accessed via the user interface.

In conclusion, a test of the Phoebus alarm system is being developed. Using the EIC-DIRC laser interlock PCB as a real-time data signal source, this test will check the response of the Phoebus alarm system.

[1] P. Bonneau, et al., *Proposal to Implement Alarm System in Control System Studio Phoebus for the Hall C Neutral Particle Spectrometer*, DSG Note 2021-37, 2021.
[2] P. Bonneau, et al., *Detector Signal Simulator for Testing the Hall C Neutral Particle Spectrometer's Phoebus Alarm System*, DSG Note 2023-23, 2023.
[3] P. Bonneau, et al., *Design and Implementation of Detector Simulator Templates for the Development and Testing of the Hall C Neutral Particle Spectrometer's Phoebus Alarm System*, DSG Note 2023-32, 2023.
[4] P. Bonneau, et al. *Testing of the CS-Studio Phoebus Applications and Alarm System Core Programs*, DSG Note 2023-06, 2023.
[5] T. Lemon, et al., *Design and Features of the EIC-DIRC Laser Lab's Laser Interlock System*, DSG Note 2023-01, 2023.