DSG R&D
Hall B Magnets’ LV Chassis Improvements

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Spare LV Chassis on workbench in EEL 121C with DE0-Nano-SoC installed.
Communications map for Hall B Solenoid. Torus’s communication map is very similar.
Hall B Magnets’ LV Chassis

• Multi-sensor Low Voltage Excitation chassis (“LV Chassis”) provides an excitation voltage/current to sensors to read their measurements.
  – 16 Cernox
  – 16 PT100s
  – 16 strain gauges
  – 4 load cells or Hall sensors

• “Brain” of LV Chassis is a DE0-Nano board with Cyclone IV Field Programmable Gate Array (FPGA).

LV Chassis communication map extracted from previous slide.
DSG’s Proposal - DE0-Nano-SoC

• Replace currently used FPGA board with DE0-Nano-SoC.
  – Altera FPGA board with 40-pin header, allowing direct hardware replacement.

• Has Altera Cyclone V System-on-a-Chip (SoC) with FPGA and hard processor system (HPS).
  – HPS allows development of excitation program that can communicate to PLC.

Progress So Far with DE0-Nano-SoC

• Configured board for network.

• Successfully compiled and deployed Altera’s provided examples.
  – Tests functionality of FPGA, HPS, and FPGA-HPS interface.

• Successfully configured, compiled, and deployed existing LV Chassis FPGA program to board.

• Replicated LV Chassis cRIO’s excitation program in Python.

• Investigated MicroPython for HPS.

• Investigated different Linux distributions for HPS.

• Investigated FPGA-HPS communication configuration.
Successes

• Altera’s examples compiled and deployed to DE0-Nano-SoC.
  – FPGA program to toggle LEDs.
  – HPS program to print “Hello World”.
  – FPGA-HPS program to initiate LED toggling with HPS command.

• Existing LV Chassis FPGA code compiled and deployed.
  – Pin assignments corrected for Cyclone V.
  – Verified using version of LV cRIO program modified to run on desktop with no PLC communication.

• Replicated LV cRIO program in Python.
  – Proof-of-concept that code can be successfully translated to different languages.
Problems Faced

• Network configuration issues.
  – HPS does not have its MAC address assigned by manufacturer, causing board’s MAC to change on reboot.
  – Manually setting and saving MAC address environment variable resolves issue.

• MicroPython and its DE0-Nano-SoC add-on does not compile.
  – Add-on specifically for board is out-of-date and is not compatible with current version of MicroPython.
  – Investigation stopped; excitation program will be re-developed in C.
    ✓ C binaries known to work on HPS as all Altera examples are C-based.
Problems Faced (cont.)

- HPS unable to boot other Linux distribution except for Altera-provided version.
  - Altera-provided version is a basic, terminal-only distribution from 2013.
  - Unsuccessfully attempted to install Debian on HPS.
    - Debian usable on other ARM processor boards (Raspberry Pi, BeagleBoard).
- Unable to compile own program that utilizes FPGA-HPS interface.
  - Took known working FPGA program and tried to add HPS interface and modified program does not compile.
  - May be due to missing step in configuring the interface; investigations will continue.

Data flow chart for attempted FPGA-HPS interface.
Conclusion

• DSG investigating whether LV cRIO can be replaced by using the more advanced DE0-Nano-SoC board in LV Chassis.
  – Gives advantage of all sensor excitation, readout, and communication to PLC is performed in one self-contained package.

• DE0-Nano-SoC has difficulties in programming FPGA-HPS interface.
  – Current investigation still underway.