



# sbRIO-based Upgrade of Hall B Magnets' MSELV Chassis

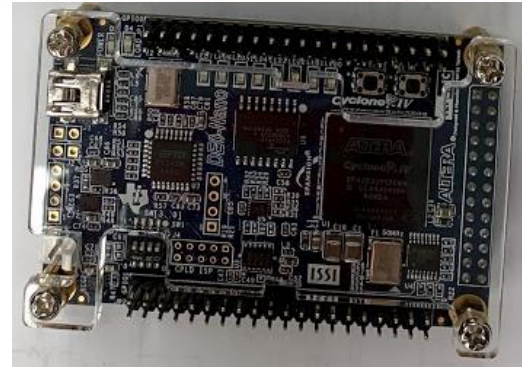
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# Upgrade of MSLEV Chassis

- Present MSLEV Chassis uses Altera Cyclone IV FPGA on a DE0-Nano board
- Tried upgrading MSLEV Chassis with Altera Cyclone V FPGA on a DE0-Nano-SoC board
  - Adds SoC/Linux capabilities
  - Did not work as expected
- Using National Instruments single-board Reconfigurable Input/Output (sbRIO) controller in place of FPGA



DE0-Nano



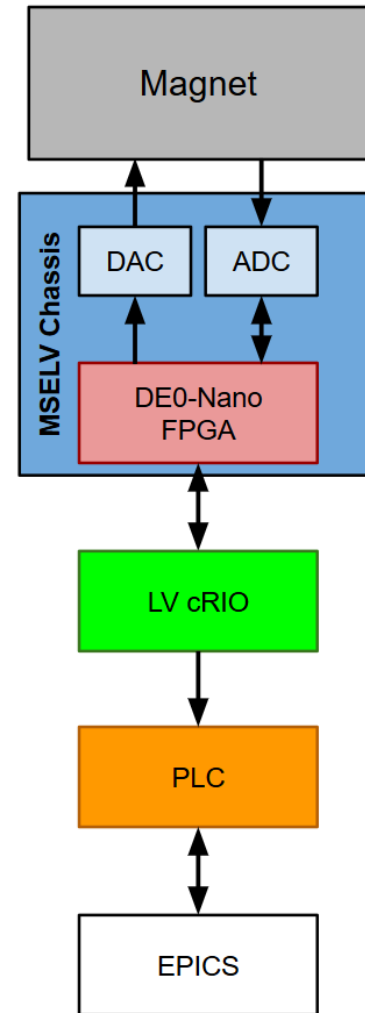
DE0-Nano-SoC



sbRIO

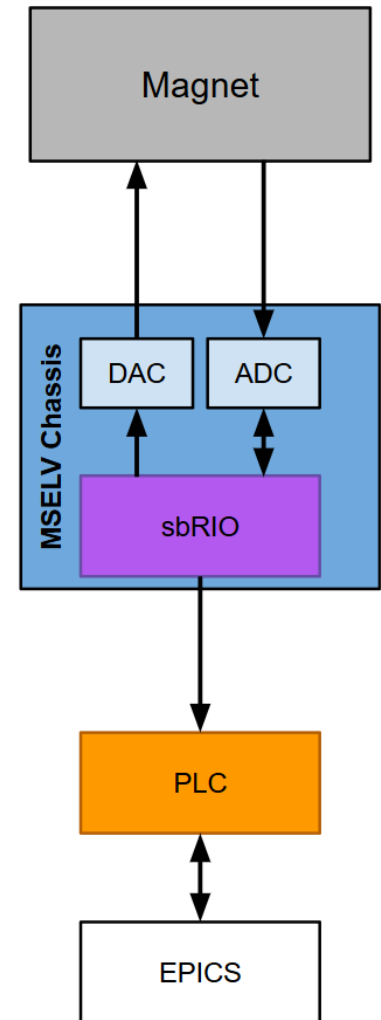
# Present System Configuration

- DE0-Nano FPGA in MSLEV chassis sets DACs and reads ADCs
  - LV cRIO communicates with DE0-Nano FPGA over serial line to set excitation values and read sensors' response
  - Excitation values are written to DACs
  - Sensor responses are measured by MSLEV ADCs
  - LV cRIO converts sensor response to correct units, writes data to PLC, and determines next excitation value



# Proposed System Configuration

- Replace DE0-Nano and LV cRIO with **sbRIO**
  - sbRIO performs all DE0-Nano FPGA's functions in addition to LV cRIO functions
  - Limits points of failure in sensor readout path by removing LV cRIO
  - Gives ability to add additional functions in future
    - Independent EPICS interface
    - Changeable configuration files for sensors

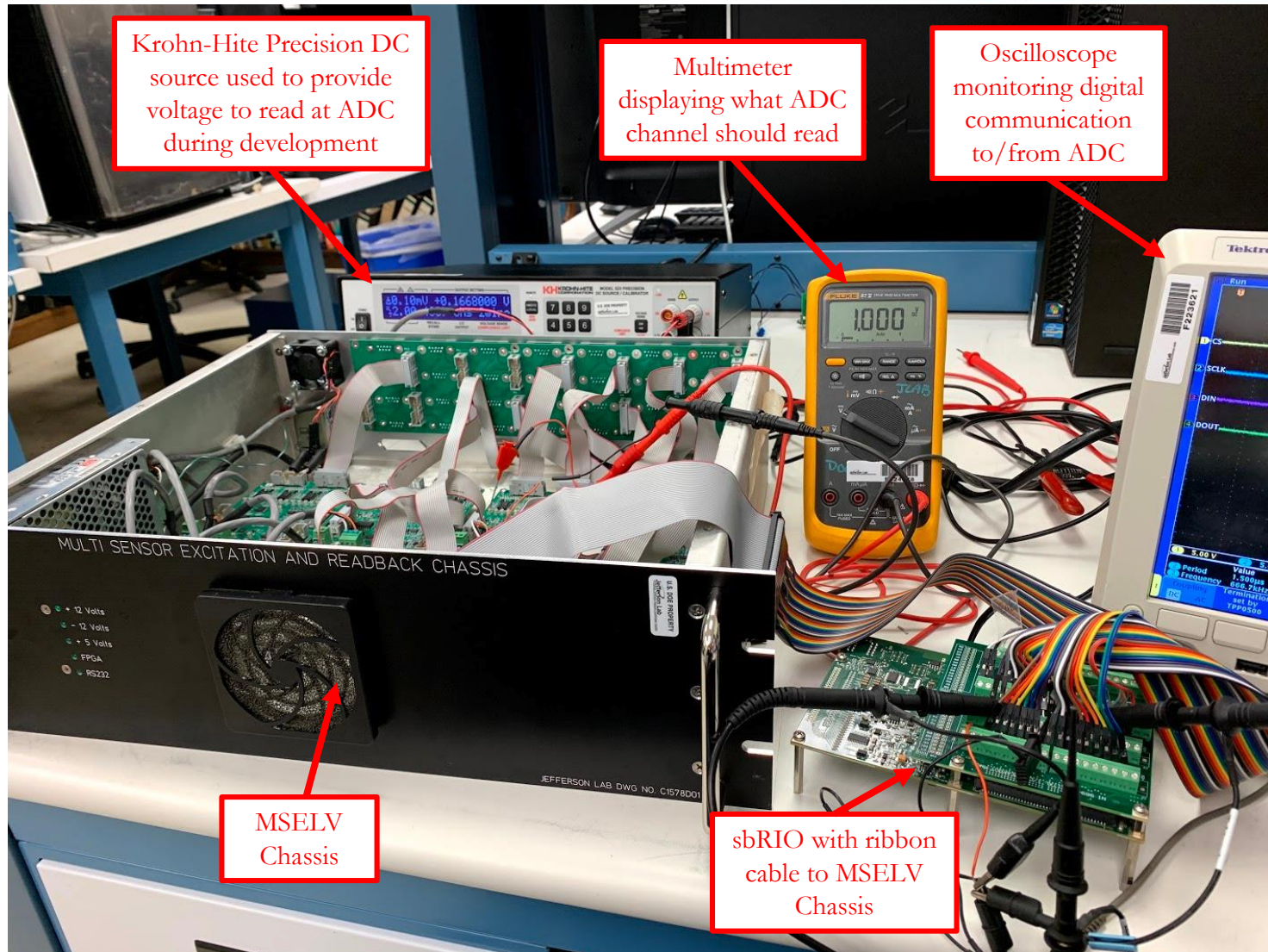


# LV Chassis sbRIO Tasks

1. Develop DAC interface
2. Develop ADC interface
3. Integrate sbRIO FPGA code into existing LV cRIO program in place of serial communication
4. Test MSELV Chassis with sbRIO



# Development Test Station



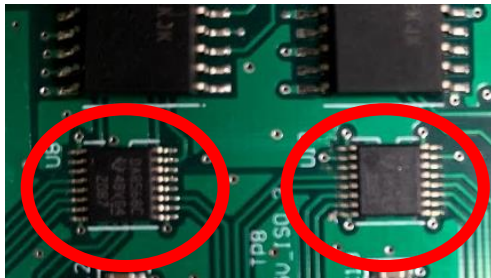
Test station for sbRIO and MSELV Chassis during ADC subVI development

# sbRIO Progress – DACs

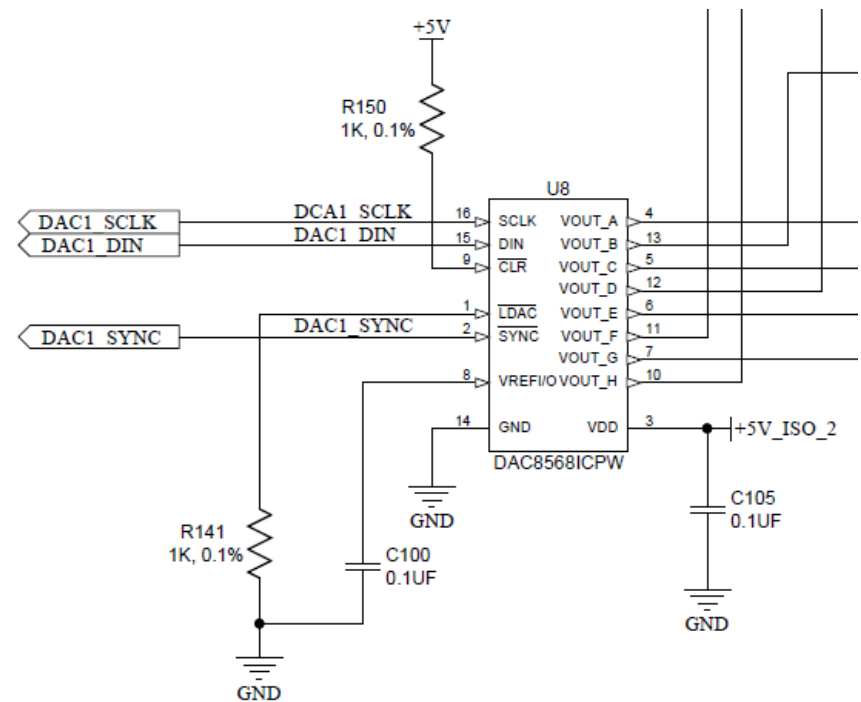
- FPGA interface to DACs

completed

- Generates required sync, clock, and data signals
- Writes signals to digital output in MSELV Chassis



Two DACs, each with eight 16-bit voltage output channels on MSELV Chassis Sensor Readback board



One DAC in MSELV Chassis Sensor Readback board schematic



# DAC Communication

All signals are 0 V (low) – 3.3 V (high)

## SYNC

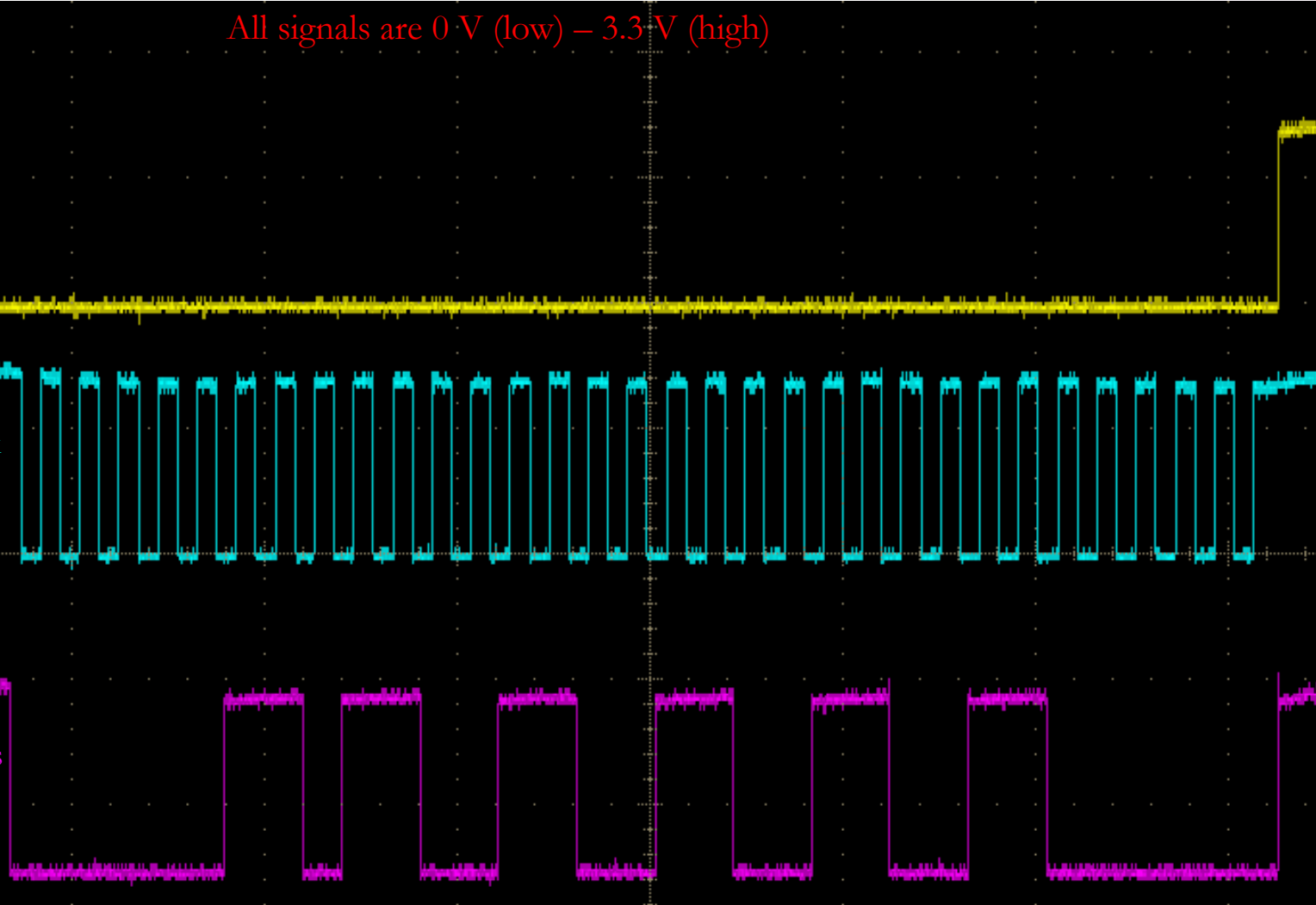
Tells DAC to listen for command.

## CLOCK

Shifts data to DAC's output register on clock falling edge (50 kHz used).

## DATA

Data written to DAC's output register. Contains command to perform, channel address, and data to write.



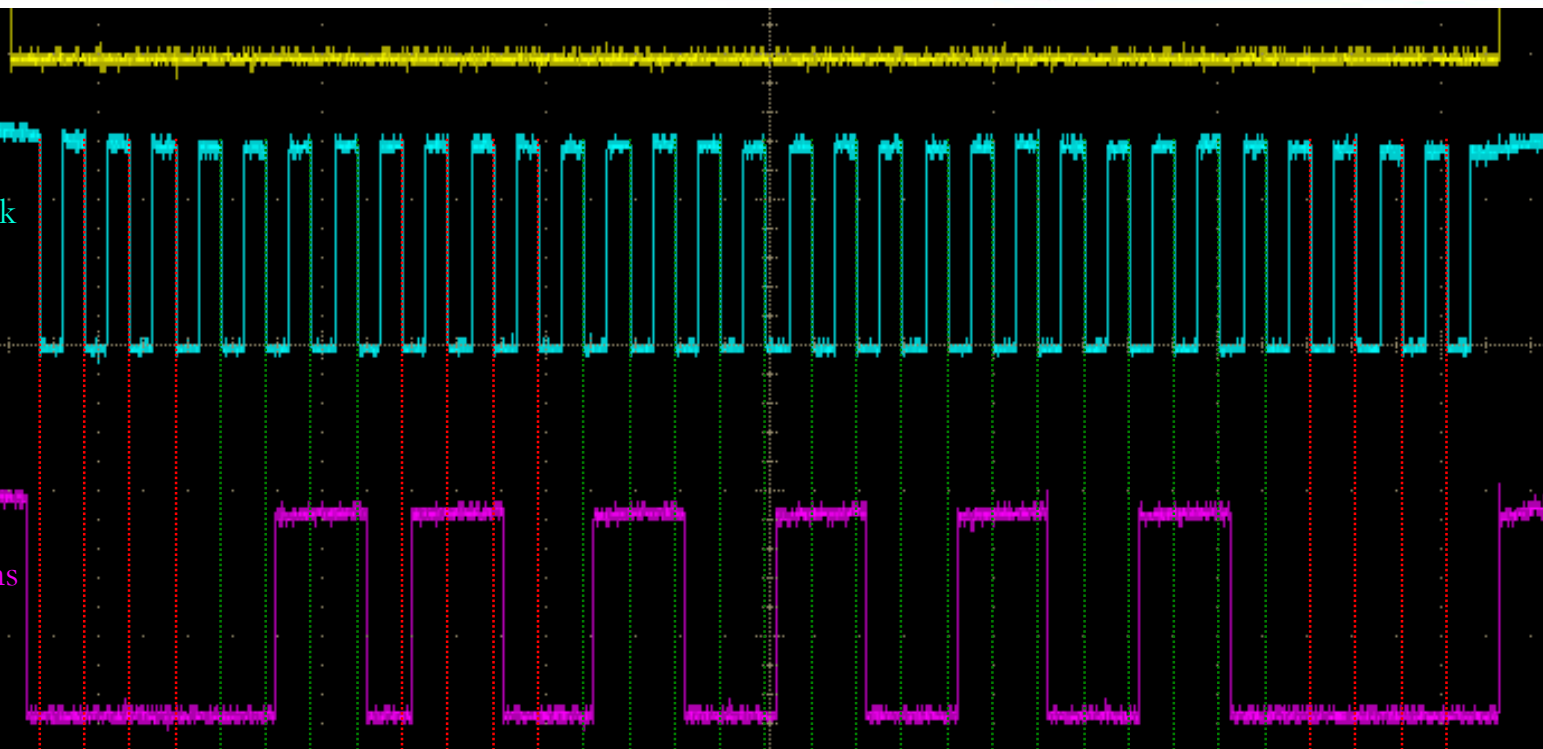
# DAC Communication – Command Breakdown

## CLOCK

Shifts data to DAC's output register on clock falling edge (50 kHz used).

## DATA

Data written to DAC's output register. Contains command to perform, channel address, and data to write.



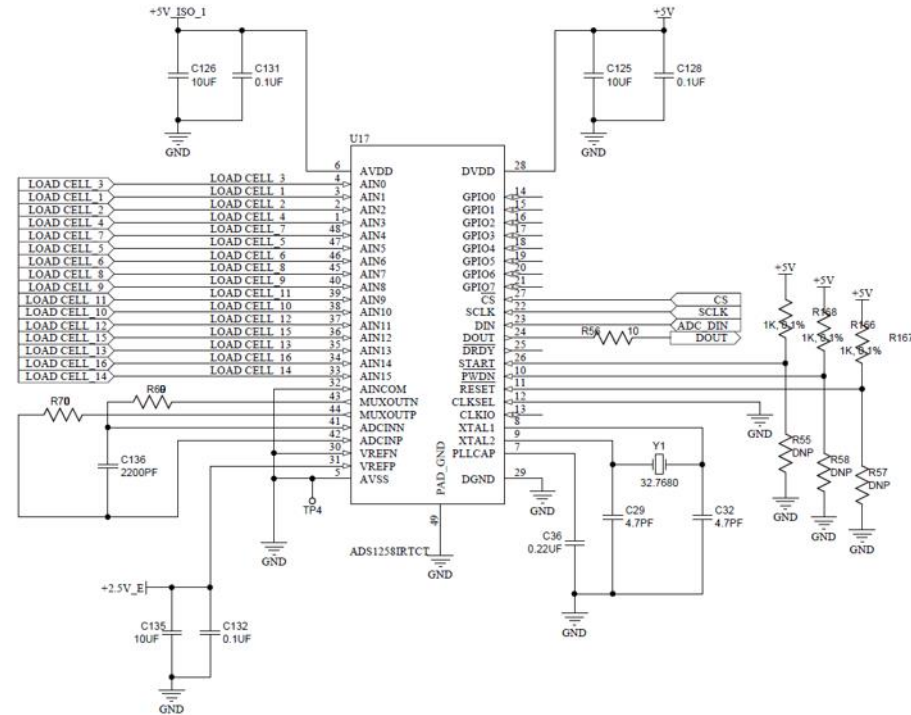
0 0 0 0	0 0 1 1	0 1 1 0	0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0	0 0 0 0
<b>Prefix Bits</b>	<b>Control Bits</b>	<b>Address Bits</b>	<b>Data Bits</b>	<b>Feature Bits</b>
First bit is always zero, other Prefix Bits do not matter.	Set and load DAC channel addressed	0110b = 6  Write to DAC channel G	0110011001100110b = 26214 DAC counts = 2 V  Tells DAC channel to output 2 V.	Used to configure certain features of DAC

# sbRIO Progress - ADCs

- FPGA interface to ADCs completed
  - Generates required sync, clock, and data signals
  - Reads ADC response
    - ADC configured via wiring on PCB for multiplexed channel scan mode

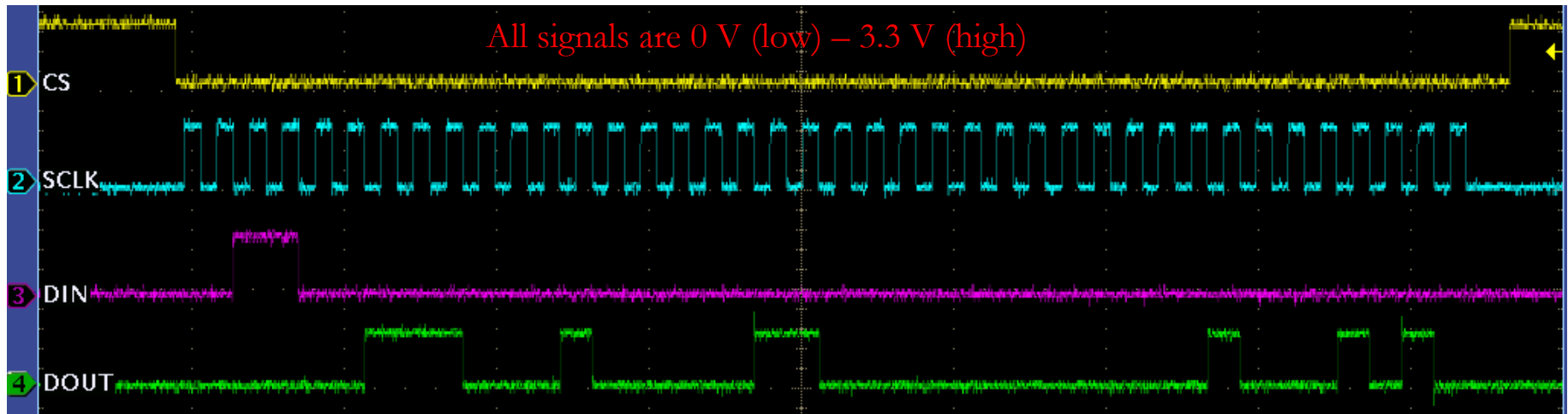


16-channel, 24-bit ADC on MSELV Chassis Sensor Readback board.



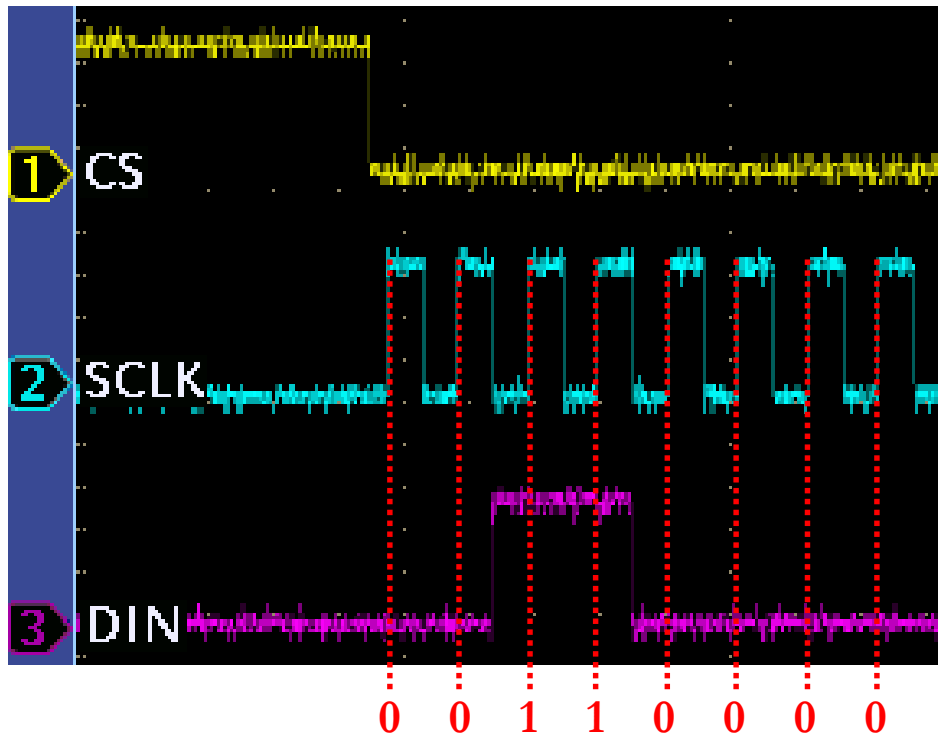
ADC in MSELV Chassis Sensor Readback board schematic. ADC is configured by VREFP and VREFN pin wiring to read 0 V – 2.5 V.

# ADC Communication



- CS
  - “Chip Select”
  - Tells ADC to ready for input/output
- SCLK
  - “Serial Clock”
  - Clock for shifting data to/from ADC
  - ~200 kHz frequency used
  - 40 total clock transitions
- DIN
  - “Data In”
  - 8 bits for command
- DOUT
  - “Data Out”
  - 32 bits for readout
    - First 8: status
    - Remaining 24: ADC measurement

# ADC Communication – Data In

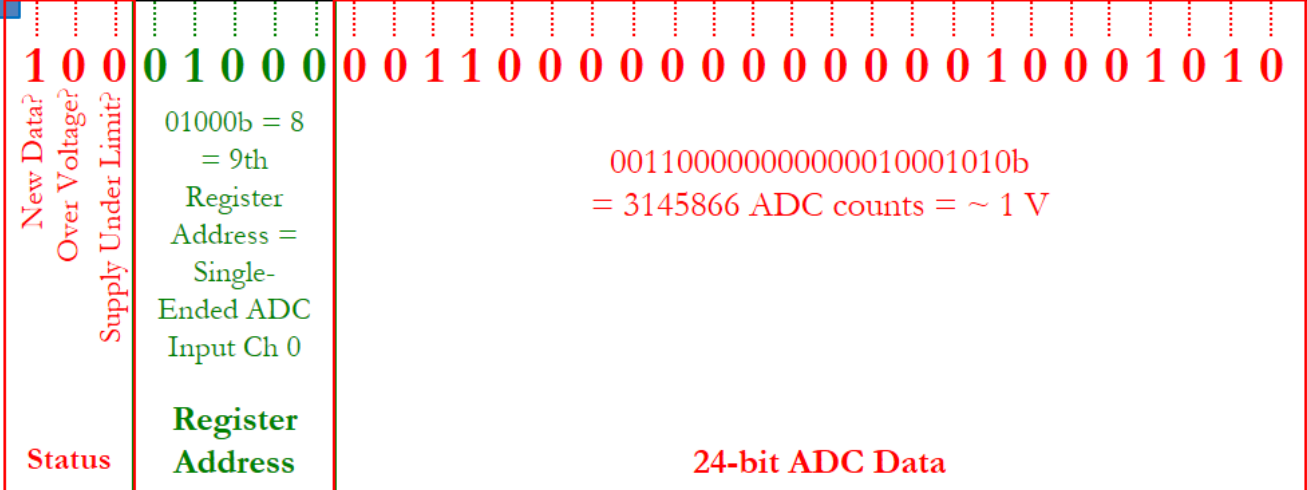
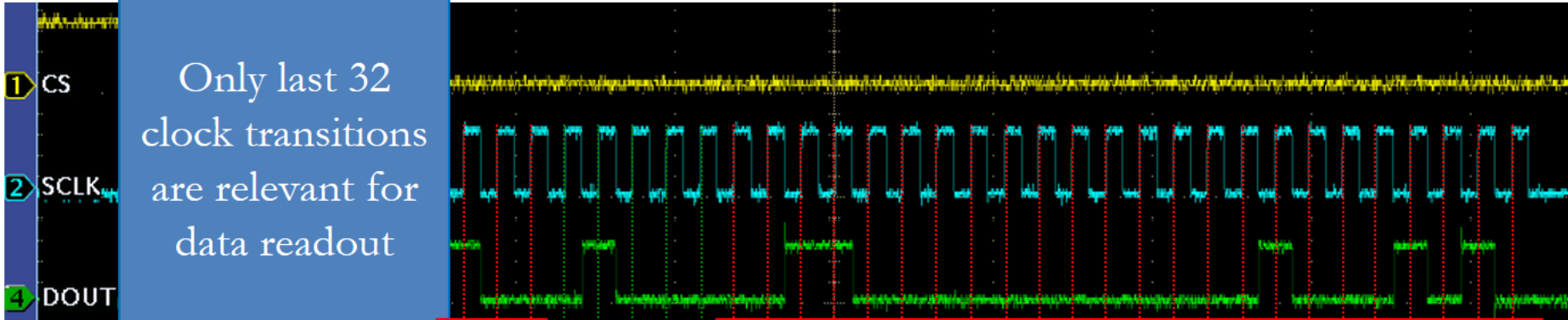


Only first 8 clock transitions are relevant for data input

- “Channel Data Read” command
  - Readout command option available without use of DRDY pin
    - DRDY pin is not connected to anything on PCB
  - Command reads whichever ADC channel has most recently finished converting new data
    - Typically converts all 16 channels in ~300 ms

# ADC Communication – Data Out

Only last 32 clock transitions are relevant for data readout





# sbRIO FPGA–Real Time Interface

- Portion of code that calculates excitation values, converts ADC readings to correct units (temperature, lbf), and communicates to PLC is under development
- Currently mapping sensor input ports to FPGA channels

# Conclusion

- Working to replace DE0-Nano FPGA in MSELV Chassis and LV cRIO with an sbRIO.
- DAC interface subVIs completed.
- ADC interface subVIs completed.
- Program that converts raw ADC data to relevant units (temperature, lbf) in progress.

**Thank You**