Asynchronous Inputs and Flip-Flop Metastability in the CLAS Trigger at CEBAF

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Abstract

The impact of flip-flop metastability on the pipelined trigger for the CLAS detector at CEBAF has been studied. We find that the newest ECL flip-flops (ECLinPS) are much faster than older families (10H) at resolving the metastable condition. This will allow their use in systems with asynchronous inputs without an extra stage of synchronizing flip-flops.

I. INTRODUCTION

The CLAS detector at CEBAF is designed to be run at luminosities exceeding $10^{34}cm^{-2}s^{-1}$, producing an interaction rate of several Megahertz. Specifications for the CLAS data acquisition system call for events to be read out from the detector at a rate above 1 kHz. To achieve this factor of 1000 reduction in rate we have designed a two level trigger system. The LEVEL 1 trigger looks at all prompt signals and processes them through a three-stage pipelined memory lookup within 90 ns. Details of the design of the LEVEL 1 trigger are given in reference 1. The resulting trigger signal initiates data acquisition at the front end electronics of all detectors. The LEVEL 2 trigger (which is still in the design phase) will use information from the drift chambers to find tracks and match them with trigger requirements. Events which pass the LEVEL 2 trigger are then read out and sent to the processing farm for reformatting, partial analysis, and storage.

II. METASTABILITY

A. Why Metastability Occurs

When memories are used to perform logic functions the addresses must be stable during the read access time to guarantee valid data out. The LEVEL 1 trigger must therefore sample and store the input data at discrete times, then apply this data to the address lines. This is done with a set of flip-flops which are clocked at the pipeline speed of the trigger, 67 MHz. Because of the continuous nature of CEBAF's beam, the input signals arrive at these flip-flops at random times, asynchronous to the pipeline clock. This means that some fraction of the time the setup or hold time specifications of the input flip-flops will be violated. All flip-flops have a metastability window around the clock edge which lies somewhere between the setup and hold times. When the data changes during this metastability window a flip-flop takes longer to reach its final output value than the normal propagation delay.

The effect of either metastability depends on the logic following the flip-flop. In the CLAS LEVEL 1 trigger the output of these flip-flops is sent to the address lines of the memories, which need to produce their data for the next set of flip-flops by the next clock cycle. The memories cannot be counted on to begin a valid read cycle until the address data has reached a valid state. This lengthens the effective propagation delay time of the flip-flops. If not accounted for, the memories can retrieve erroneous data, causing a trigger error.

The two ways of dealing with this problem are either to allow extra settling time (above the normal propagation delay) for the metastable event to be resolved, or to add an extra synchronizing stage of flip-flops. The disadvantage of the first solution is that the pipeline clock rate must be reduced, resulting in increased trigger latency, while in the second case the extra clock cycle also adds to the latency of the trigger. In either case some way of quantifying the allowed extra settling time is needed.

B. A Quantitative Treatment of Metastability

Stoll[2] related the Mean Time Between Failures (MTBF) of a digital system with asynchronous inputs to the metastable behaviour using the equation:

$$MTBF = 1/(2*f_c*f_d*T_P*10^{-(\Delta t)/\tau}) \quad (1)$$

where:

f_c	is the clock frequency
f_d	is the data frequency.
T_P	is the normal propagation delay
T_D	is the minimum delay after a clock that constitutes a failure
Δt	is the excess delay (T_D-T_P)
τ	is the flip-flop resolution time constant.

Equation 1 characterizes the MTBF as a function of the flip-flop properties (T_P, and τ), the system design parameters (f_c and f_d), and the amount of additional time, above the propagation delay, allowed for the flip flop to reach its final value (Δt). This equation may be turned around to allow computation of the Δt needed to obtain a certain MTBF:

$$\Delta t = \tau \log (MTBF*2*f_c*f_d*T_P) \quad (2)$$

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The difficulty in using these equations comes from the fact that while the propagation delays for flip-flops are given in data books, the resolution time constant is almost never revealed. Motorola has recently released an application note[3] which reports measurements of τ for several different flip flops.

C. Metastability effects in the CLAS trigger

The LEVEL 1 trigger requires a multiple input D-type flip-flop. We therefore compared a 10E151 with a 10H186. The 10H186 is not shown in the table above, but it should have characteristics not very different from the 10H131[4].

The computational procedure is as follows. The pipeline clock frequency of the LEVEL 1 trigger is 67 MHz. There are 384 inputs into the LEVEL 1 trigger; each of these is expected to have a data frequency of 25 kHz, which yields an aggregate data frequency of 9.6 MHz. Equation 2 is then used to predict the extra settling time Δt needed for a given flip-flop, in order to have a 1000 s MTBF. This MTBF figure will yield a trigger error rate of less than 1 in 1,000,000. The total settling time T_D is computed by adding the propagation delay to Δt. This figure, which we call T_D1000, yields the total time which must be allowed after the clock for the input flip-flops to settle, in order to get this error rate. Another way of saying it is that T_D1000 is the metastable pulse width which should be equaled or exceeded by no more than one event during 1000 s of running with the CLAS detector. The results of these calculations are shown in Table 1.

Type	τ	Δt	T_D1000
10H186	~718 ps	6.9 ns	9.9 ns
10E151	185 ps	1.7 ns	2.5 ns

Table 1. Excess delay time (Δt), and the total delay time needed to yield a 1000 s MTBF (T_D1000).

These calculations indicate that use of the 10H186 at the inputs to the pipeline would require the addition of an additional stage of synchronizing flip-flops. The 15 ns period between successive clockings would be enough to insure that the input data to the second flip-flop would have reached its final value before the setup time, and therefore the data out would reach its final value within T_P (3 ns). This would add 15 ns to the latency of the trigger.

By contrast if the 10E151 is used in the first stage of the trigger, only 2.5 ns needs to be allotted for the data to stabilize, less than the propagation delay of the 10H186 with synchronous inputs. This allows 12.5 ns for the memory logic and setup time of the next flip-flop.

III. MEASUREMENTS

To verify these calculations a series of observations of metastable events was undertaken. The idea was not to repeat the measurements done by reference 3, but to see if a simple measurement could be done that would quickly allow a rough determination that the theoretical calculations are correct, and that would also allow comparisons of T_D1000 between different flip-flops, if τ for some of them were not known. Metastability events of type 1 can be observed using digital scopes with sophisticated triggers, and it was hoped that this would allow just such a measurement.

Two controlled impedance test boards were built, one to test the 10E151, and one for the 10H186. Two pulse generators provided the stimulus, one running at 100 MHz for the clock, the other running at 25 MHz (not synchronously) for the data. With these input frequencies, a MTBF of 256 s corresponds with the 1000 s MTBF in the CLAS detector. A Tektronix TDS 640 digital scope was used in sample mode with a pulse-width trigger to observe the metastable events.

The measurement procedure was to set the pulse width and voltage requirements to trigger on the 10-15 widest pulses in fifteen minutes. Each time the scope triggered on an event, we measured the time duration from the clock until the data had returned from the indeterminate region. This yields a direct measurement of T_D for that particular event, after correcting for propagation delays on the test boards (0.7 ns for the 10H186 and 0.6 ns for the 10E151's).

As mentioned above, 256 s in the test setup is equivalent to 1000 s in the CLAS detector. Therefore we would expect to see metastable events of the width of T_D1000 or greater at the rate of one every 256 s, or between three and four events over the fifteen minute run. The width of the third largest metastable event occurring during the fifteen minute run was chosen to be representative of T_D1000, that is, the largest metastable event occurring at a rate of 1 every 1000 s in the CLAS detector.

These measurements were made for the Motorola 10H186 and 10E151, as well as the Synergy 10E151. One interesting result that was observed was that positive metastable events in the Motorola 10E151 are not large enough in voltage to make the transition to the indeterminate region (> - 1.48 V). In this case measurements of T_D were made to the highest point of the pulse, but it should be kept in mind that the pulse never actually was in the transition region. The results of our measurements are shown in Table 2, and the scope pictures of the negative pulse T_D1000 events are shown in figures 1 through 3.

This data shows several interesting results. First, our measurement of T_D1000 for the Motorola 10E151 compares reasonably well with what was calculated in Table 2 using the published value of τ. Second, the Motorola version of the 10E151 has much better metastable performance than the Synergy version of the same chip. Third, while our measurement of T_D1000 for the 10H186 is smaller than that expected from a calculation using the value of τ from the 10H131, it is still worse than either of the 10E151 chips.

Chip	Pulse dir.	Total # evts	T_D range	2nd largest T_D	3rd largest T_D (T_D1000)
M H186	+	7	5.9-6.2	6.1	6.1
M H186	-	6	5.2-6.7	6.3	6.0
M E151	+	18	1.3-2.0	2.0	2.0
M E151	-	20	2.4-2.8	2.8	2.7
S E151	+	10	3.2-3.8	3.3	3.3
S E151	-	12	3.9-4.4	4.4	4.3

Table 2. A comparison of the measured TD values for the Motorola 10H186 and 10E151, and the Synergy 10E151. The last column is interpreted as being representative of the width of the 1 in 1000 s metastability expected in the CLAS trigger.

IV. CONCLUSIONS

We have calculated T_D1000, the metastable pulse width which should be equaled or exceeded by no more than one event during 1000 s of running with the CLAS detector, for both the 10H186 and the 10E151 using the formulation first given by Stoll. These results indicate that for use in systems with asynchronous inputs, the newer ECLinPS family chip resolves the metastable condition much faster. Its performance is so good that an extra set of synchronizing flip-flops can often be avoided. We have also determined a simple way of making rough measurements of the size of these events, and have used this to compare one flip-flop against another. Our measured results are in line with the calculations. And finally we find that not all vendors' chips of the same type have the same metastable performance, and that in the 10E151 chip in particular the Motorola version outperforms the Synergy version.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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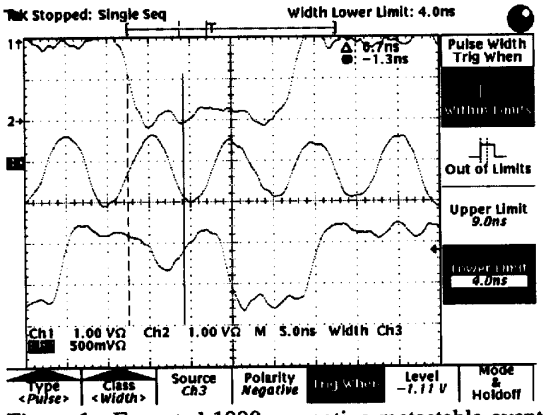

Figure 1. Expected 1000 s negative metastable event using the Motorola 10H186.

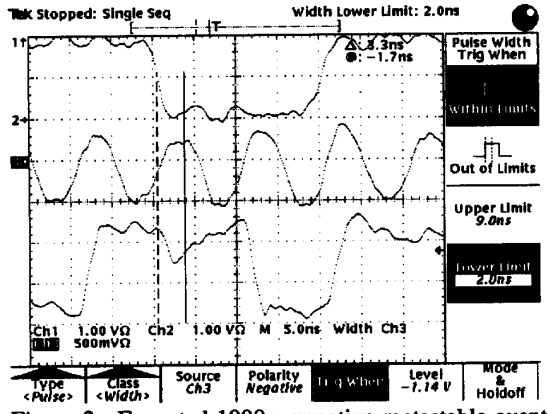

Figure 2. Expected 1000 s negative metastable event using the Motorola 10E151.

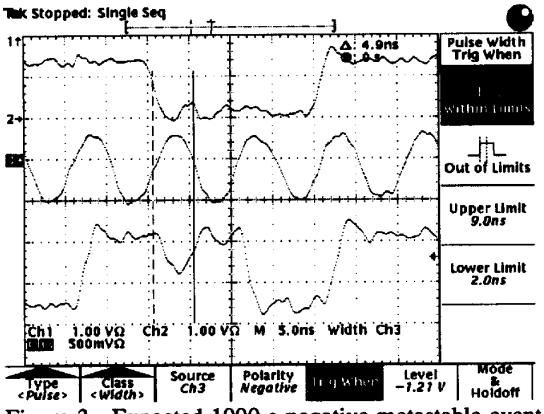

Figure 3. Expected 1000 s negative metastable event using the Synergy 10E151