Experimental Nuclear Physics Division

Fast Electronics & Data Acquisition
‘FEDAQ’

Electronics
Status and Upgrade Opportunities
for
Flash ADC and 12GeV Trigger Hardware

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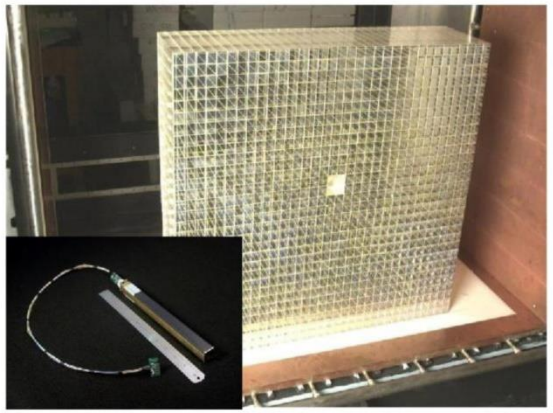
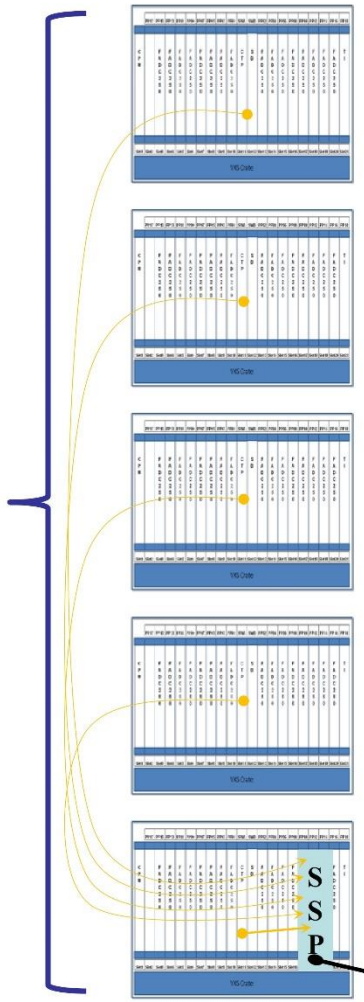
NPS Collaboration Meeting
Jefferson Lab
14-November-2013

Pipeline DAQ/Trigger for NPS (Low Q^2)

31 x 36 2D Array
1116 - PMT Channels (R4125)
Coaxial output to FADC250



PrimEx PbWO crystals



Trigger from Calorimeter
Distributed to other Detector DAQ crates

- **256 channels/crate**
- **5 VXS crates needed**
- **Need Crate Trigger Processors**
- **One VXS crate would need a SubSystem Processor**

- **SSP will need to combine clusters across 256 channel boundaries for final trigger**
- Experiment trigger would be generated from the SSP and distributed to the other detector DAQ crates.

- Many details not shown but this type of Cluster finding trigger will require significant hardware cost commitment.
- Good news is that a good deal of firmware effort has been completed for the HPS cluster functions, so in principle these firmware features can be reused for NPS.

Use VTP rather than CTP

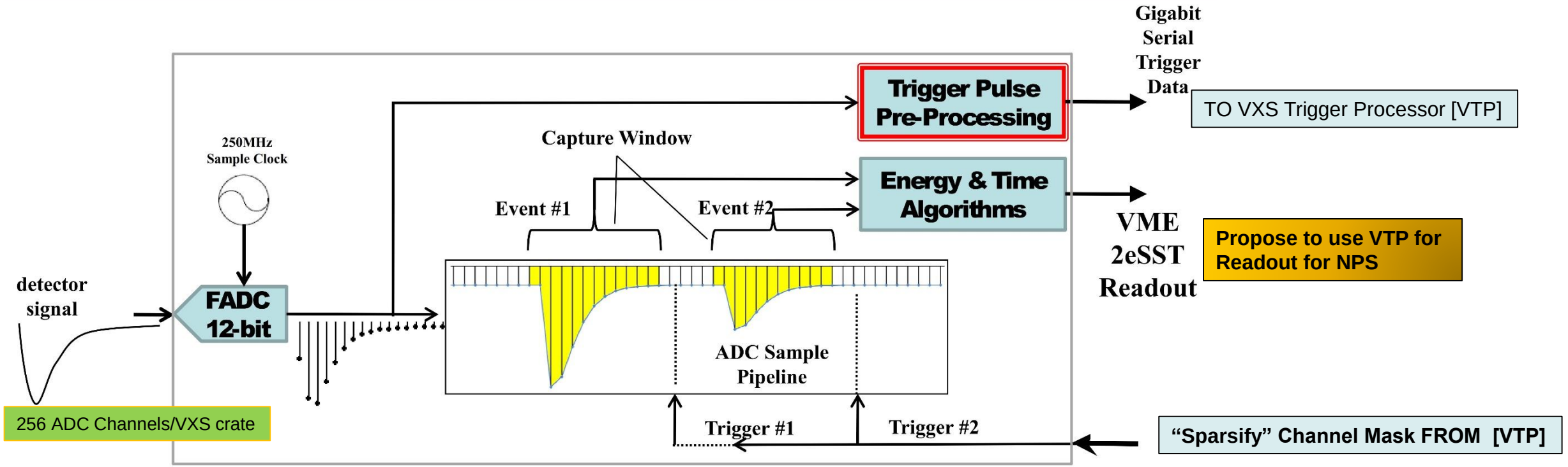
VTP replaces SSP

Flash-250Msps modules need to be secured with NPS group by FY22 start.

Modules accounted:
Trigger Interface –TI
Signal Distribution –SD

VXS crates – On site

Pipeline Method of Signal Capture



- ADC buffer is 8uS
- FADC250 "Mode10" algorithm needs testing – H. Dong, E. Jastrzembski
- Firmware for handling Channel Mask to inhibit channels from readout ["Sparsify"] NOT started, but method is understood.

VTP (VXS Trigger Processor)

- Designed for creating triggers from VXS payload modules (FADC250, DCRB, VETROC) - lives in the switch slot of the VXS crate

- 10 to 20Gbps links to each VXS payload slot

- 4x QSFP+ modules running at 34Gbps to interconnect crates and share trigger information: for NPS these will be used to share FADC hits between crates so the trigger clustering logic can perform correctly even when clusters use hits not in the local crate

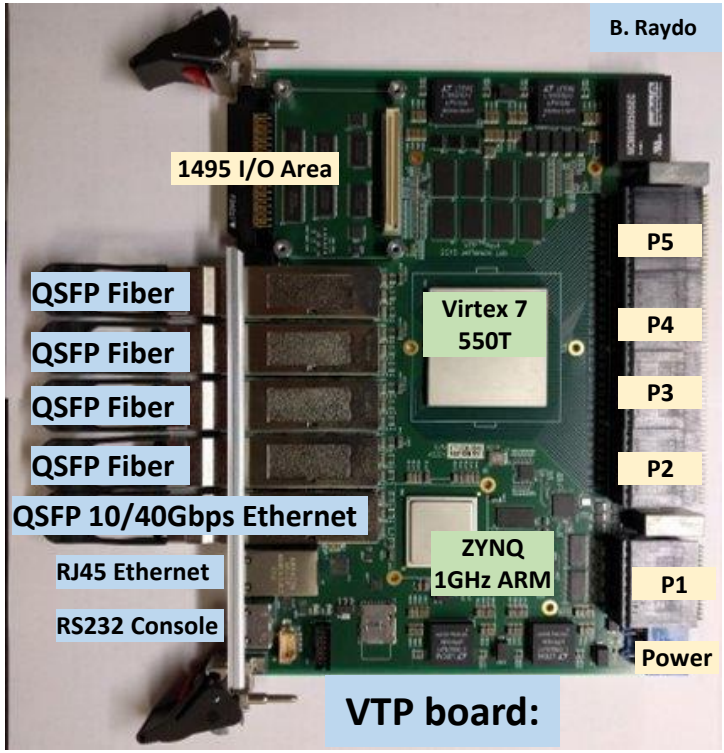
- 1x 1Gbps copper ethernet, 32bit 1GHz ARM CPU running Centos 7 Linux. Can run CODA ROC capable of 100kHz readout rate with data <100MB/s

These features have been used for CLAS12 and Hall A Compton

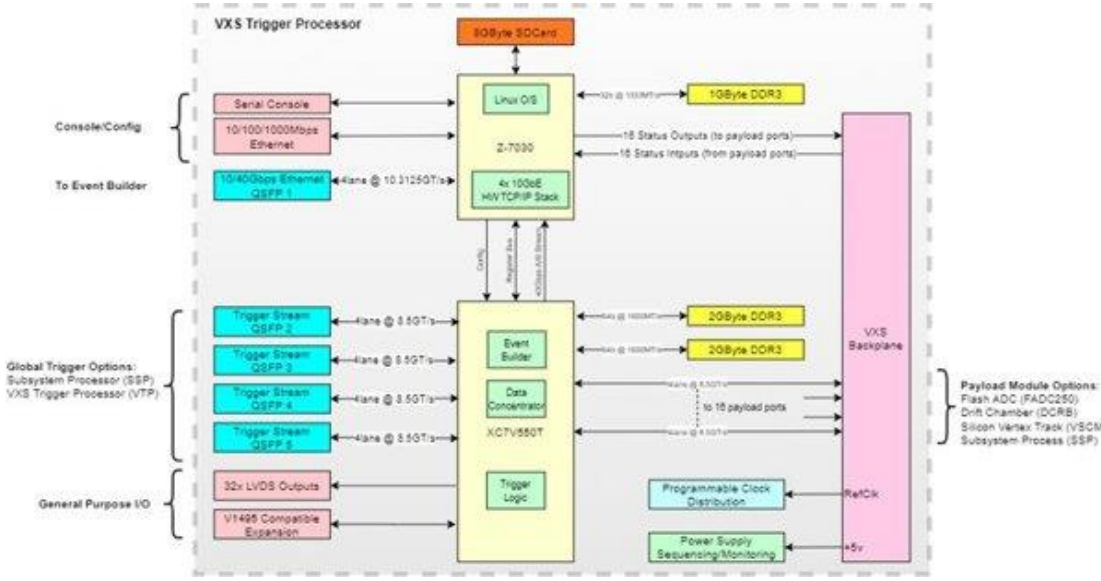
- 1x QSFP+ module running at 40Gbps. Can also be used as 4x 10Gbps Ethernet links

- 4GByte of DDR3 memory (100Gbps bandwidth) that can be used for data buffering (not used in trigger applications at the moment)

These additional features were used by the Jlab Streaming Readout beam tests in 2020



VTP H/W block diagram:



VTP – upgrade to VME readout

- VME readout of FADC250 is limited by 2eSST 200MB/s (with overhead it's ~150MB/s) and the CPU Ethernet link (typically 1Gbps, but can be upgraded to 10Gbps)

- Instead, by: Increasing the FADC -> VTP trigger link from 10Gbps to 12.5Gbps we can send 200MB/s from each FADC (in a crate, all 16 FADC would send at 200MB/s in parallel).

- To start with we plan to use only 1x 10GbE links from the VTP (4 are available), so this becomes the main bottleneck. We've been able to transmit close to 9Gbps from the VTP using a single TCP socket to a server.

- Much of the CODA ROC would run on the VTP ARM CPU (as it currently does today). The front-end data movement and TCP/IP stack will be fully hardware accelerated allowing near saturation of the ethernet links.

- Will be completely compatible with CODA event builders - intended to be completely transparent to the user.

- Given the number of VXS modules at Jlab this will provide a way for this hardware to continue to be useful in higher data rate experiments in the future.

VTP ROC/readout

- The VTP ROC will support event building of VXS based front-end data (FADC250 initially, but others can follow: VETROC, DCRB, SSP, MPD)

- A standard C readout list will still run on the CPU (the VTP ARM CPU) and is modifable by users.

- Users can still generate asynchronous and synchronous events using the C readout list.

- The firmware utilization in the VTP is small for this, so the bulk of resources are still available for trigger applications that will run in parallel to this ROC firmware

- Firmware development is nearly completed and integration/testing will begin by DAQ folks in the next few weeks to iron out issues and measure the performance increase