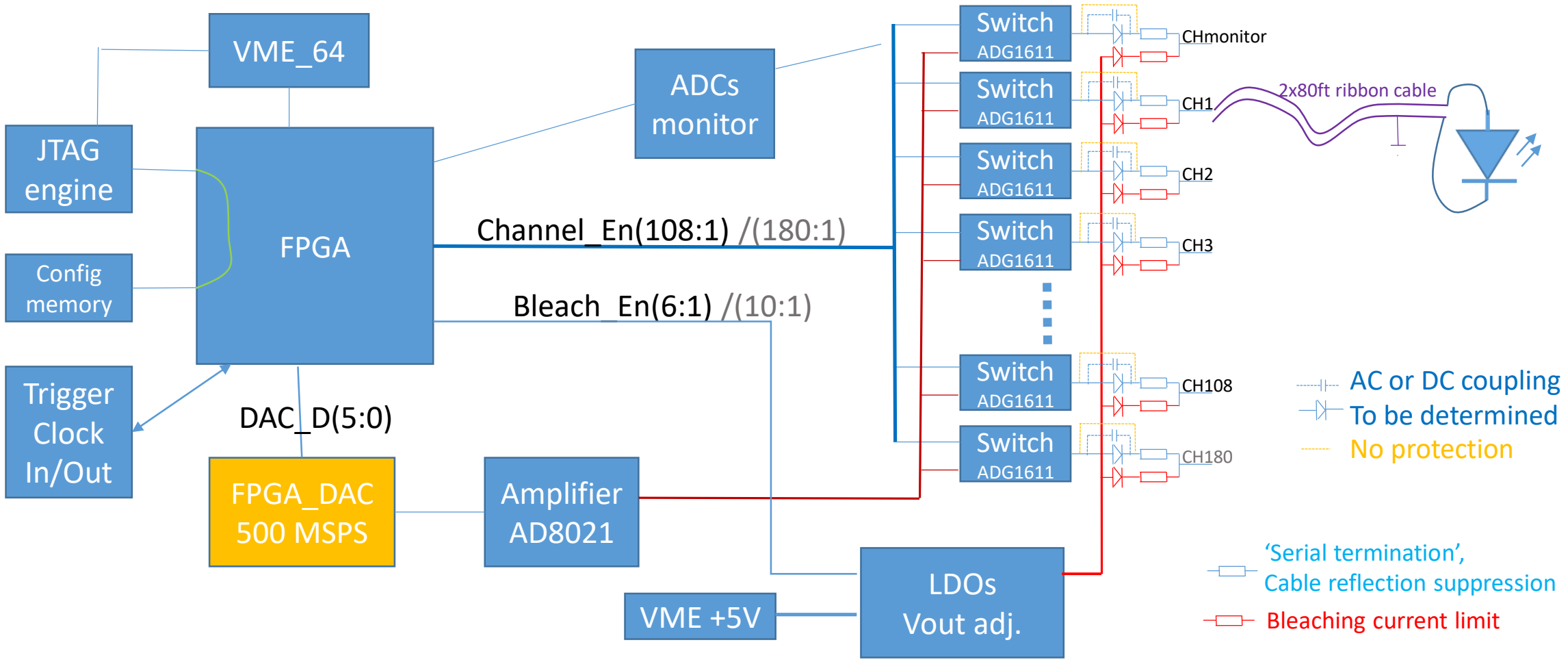
VME LED Driver (VLD) design

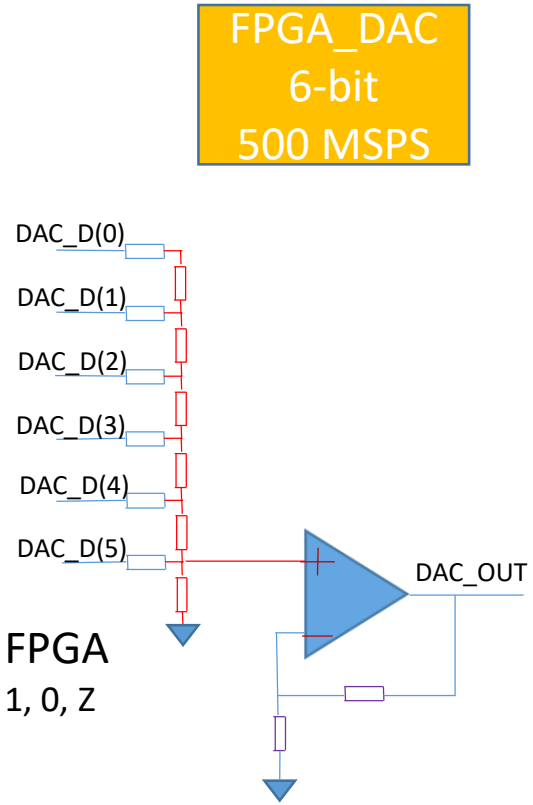
1080 (30x36) LEDs, through long ribbon cables.

- Calibration: individually controllable, up to 110 mA, ~ns pulses
- Bleaching: All ON, 35 mA, many hours

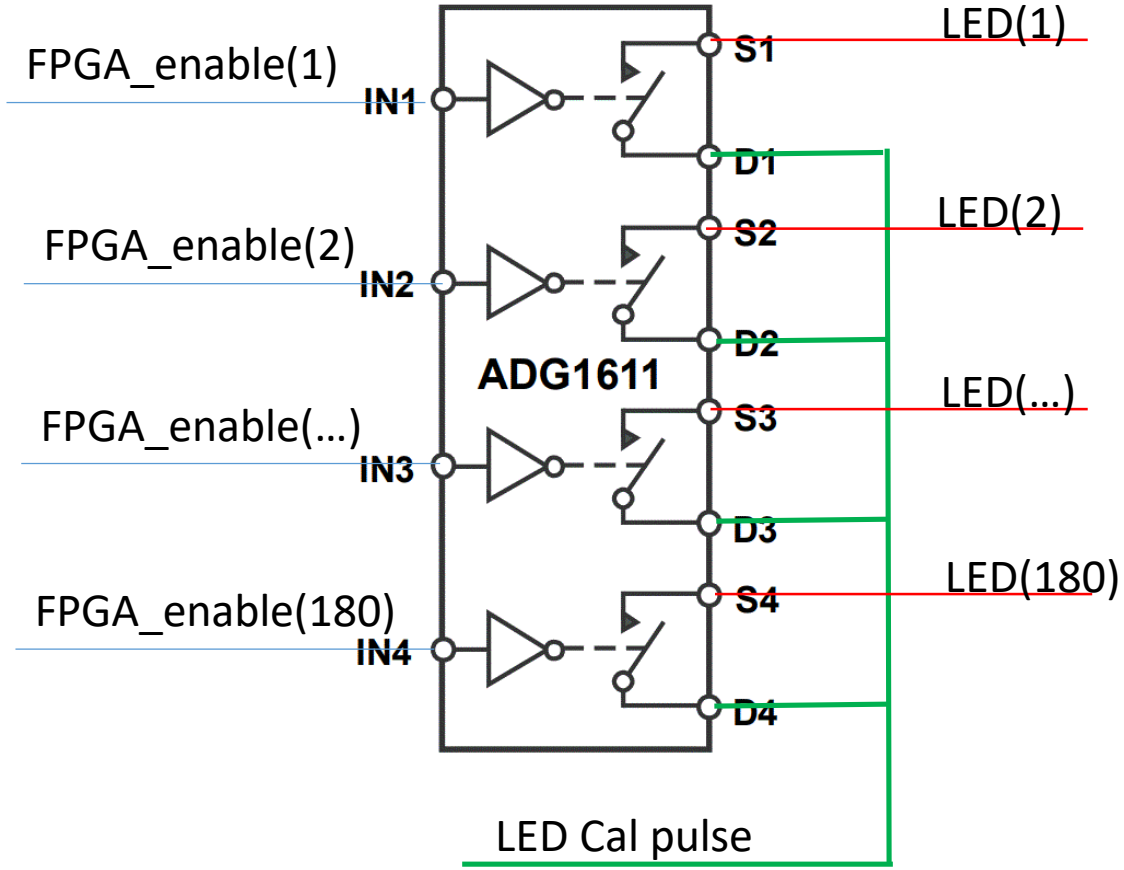
Design in progress



VLD design



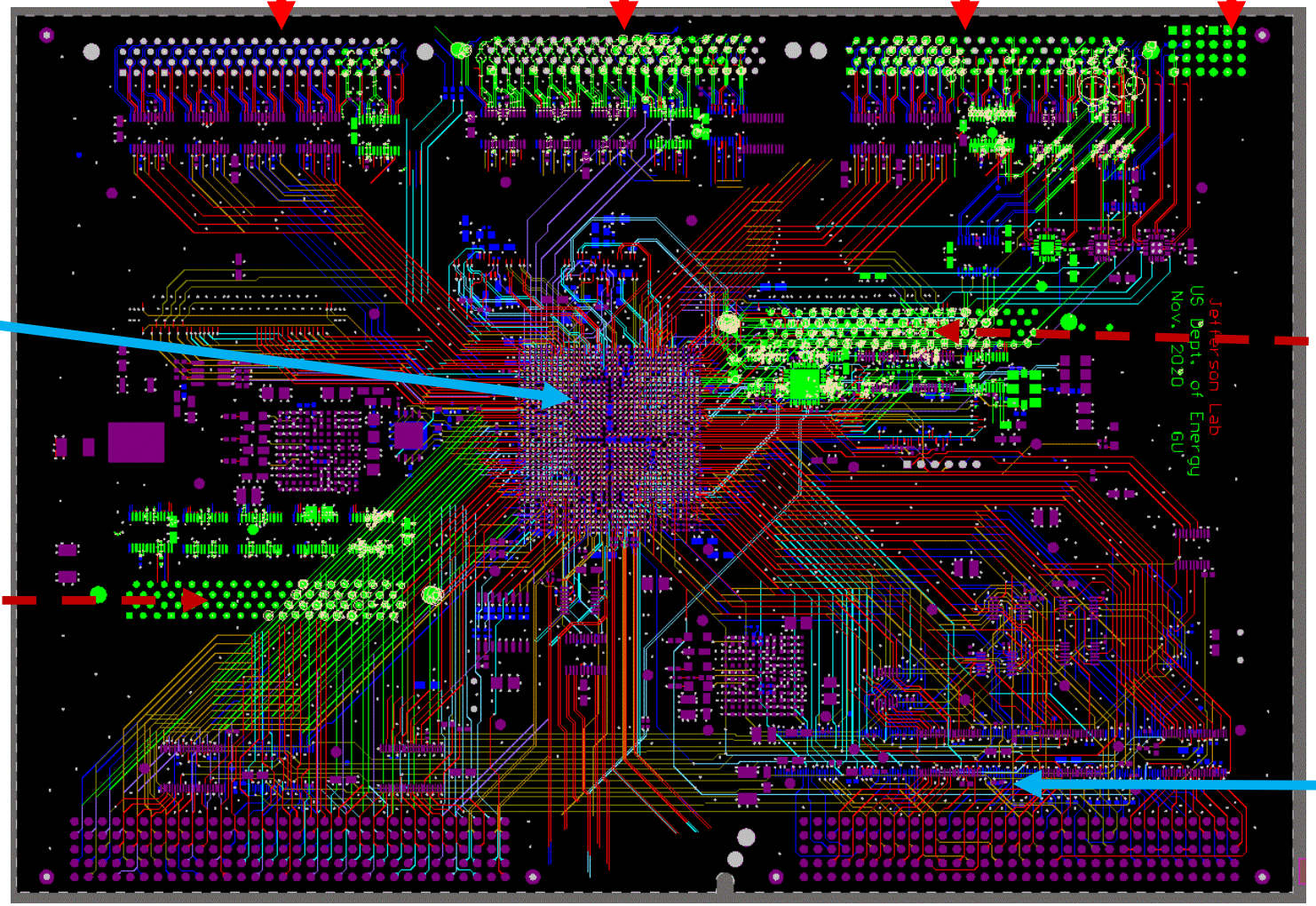
DAC_D: width adjustable with steps of 2ns
Amplitude: 3.3V, 0V, or high impedance (each bit)



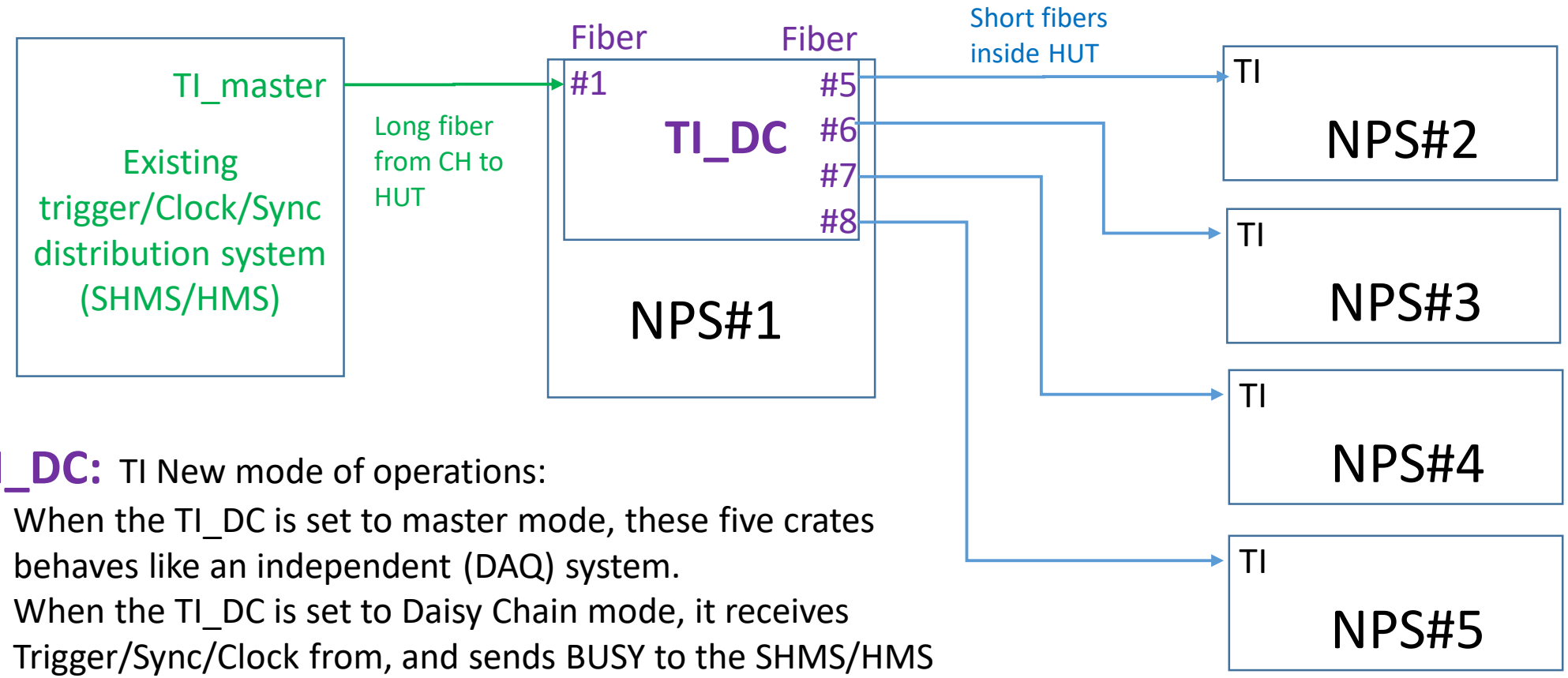
ADG1611:
1 Ohm typical on resistance
+3.3V enable control
+12V single supply.

VLD PCB

1080 channels:
* 10 VLDs: the front panel
* 6 VLDs: the front panel and on-board



Trigger Interface for NPS



TI_DC: TI New mode of operations:

- When the TI_DC is set to master mode, these five crates behaves like an independent (DAQ) system.
- When the TI_DC is set to Daisy Chain mode, it receives Trigger/Sync/Clock from, and sends BUSY to the SHMS/HMS master TI via fiber#1 (as a salve TI); fans out the Trigger/Sync/Clock to, and accepts BUSY from fiber#5, #6, #7, and #8 as a TD (or master TI).

TI_DC FPGA firmware is being developed/tested

Minimum fiber route (addition), minimum existing (SHMS/HMS) trigger interface change.